UM4616

30V Complementary Enhancement Mode MOSFET

DESCRIPTION

The UM4616 is the complementary logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology to provide excellent $R_{DS(ON)}$.

This device is suitable for use as a load switch or in PWM and gate charge for most of the synchronous buck converter applications

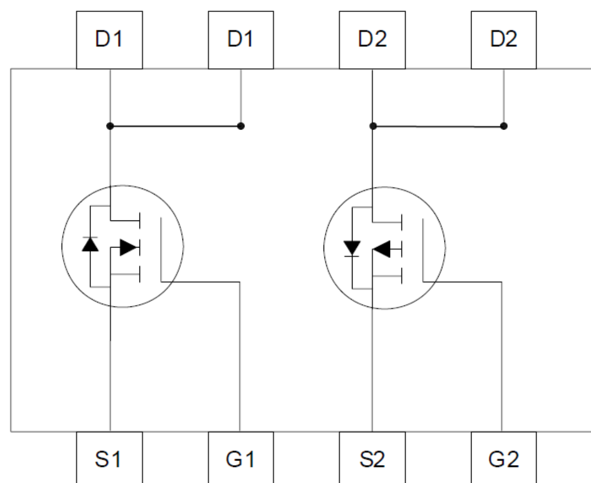
FEATURE

- ***30V/10A, $R_{DS(ON)}$=14mΩ @V_{GS}=10V N_CH***
- ***-30V/-9.7A, $R_{DS(ON)}$=20mΩ @V_{GS}=-10V P_CH***
- ***30V/10A, $R_{DS(ON)}$=22mΩ @V_{GS}=4.5V N_CH***
- ***-30V/-7.0A, $R_{DS(ON)}$=35mΩ @V_{GS}=-4.5V P_CH***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOP8 package design

APPLICATIONS

- High Frequency Point-of-Load Synchronous
- Networking DC-DC Power System
- Load Switch

PIN CONFIGURATION



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PART NUMBER INFORMATION

UM4616A-BB C	A= Package Code S: SOP BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

ORDERING INFROMATION

Part Number	Package Code	Package	Shipping
UM4616S-TR	S	SOP8	3000EA / T&R

※ Year Code : 0~9

※ Week Code : A~Z

※ G : Green Product. This product is RoHS compliant.

ABSOLUTE MAXIMUM RATINGS *(T_A = 25℃ Unless otherwise noted)*

Symbol	Parameter		N-Channel	P-Channel	Unit
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		±20	±20	V
I_D	Continuous Drain Current (T_A=25℃)	V_{GS}=10V	9	-8	A
	Continuous Drain Current (T_A=70℃)		7.2	-6.4	A
I_{DM}	Pulsed Drain Current		40	-40	A
P_D	Power Dissipation	T_A=25℃	2	2	W
		T_A=70℃	1.3	1.3	
T_J	Operation Junction Temperature		-55~150	-55~150	℃
T_{STG}	Storage Temperature Range		-55~150	-55~150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

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N Channel ELECTRICAL CHARACTERISTICS (T_A=25℃ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.4	2	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0			1	uA
		V_{DS}=30V, V_{GS}=0 T_J=55℃			30	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=10A		12	14	mΩ
		V_{GS}=4.5V, I_D=10A		16.5	22	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=10A		20		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.74	1.0	V
I_S	Body-Diode Continuous Current				2.6	A
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=15V		7.65	9.95	nC
Q_{gs}	Gate-Source Charge	V_{GS}=5V		2.82	3.67	
Q_{gd}	Gate-Drain Charge	I_D=10A		2.49	3.24	
C_{iss}	Input Capacitance	V_{DS}=15V		886		pF
C_{oss}	Output Capacitance	V_{GS}=0V		151		
C_{rss}	Reverse Transfer Capacitance	f=1MHz		75.77		
$T_{d(on)}$	Turn-On Time	V_{DS}=15V		13.92	27.84	nS
T_r		V_{GS}=10V		2.64	5.28	
$T_{d(off)}$	Turn-Off Time	R_G=6Ω		31.4	62.8	
T_f		R_L=15Ω		3.28	6.56	

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

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P Channel ELECTRICAL CHARACTERISTICS (T_A=25℃ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.0	-1.2	-2	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0			-1	uA
		V_{DS}=-30V, V_{GS}=0 T_J=55℃			-30	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-9.7A		17.1	20	mΩ
		V_{GS}=-4.5V, I_D=-7A		20.7	35	
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-8A		21.7		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.74	-1.0	V
I_S	Body-Diode Continuous Current				-2.1	A
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=-15V V_{GS}=-10V I_D=-8.0A		33.82	43.97	nC
Q_{gs}	Gate-Source Charge			4.93	6.41	
Q_{gd}	Gate-Drain Charge			5.2	6.76	
C_{iss}	Input Capacitance	V_{DS}=-15V V_{GS}=0V f=1MHz		1973	2200	pF
C_{oss}	Output Capacitance			491		
C_{rss}	Reverse Transfer Capacitance			231	325	
$T_{d(on)}$	Turn-On Time	V_{DS}=-15V V_{GS}=-10V R_G=6Ω R_L=15Ω		15.44	30.88	nS
T_r				5.04	10.08	
$T_{d(off)}$	Turn-Off Time			71.04	142.08	
T_f				16.8	33.6	

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N Channel TYPICAL CHARACTERISTICS (25℃ Unless Note)

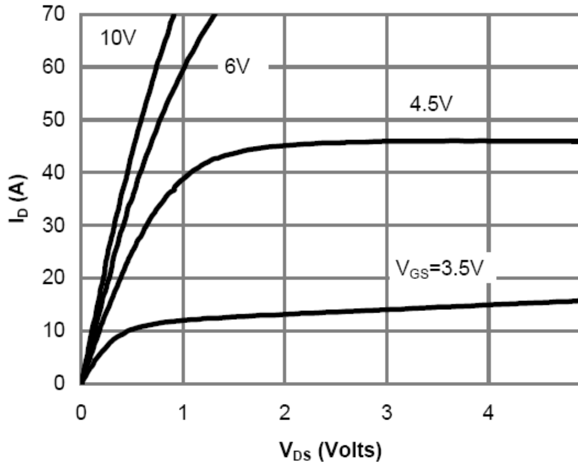

Fig 1: On-Region Characteristics

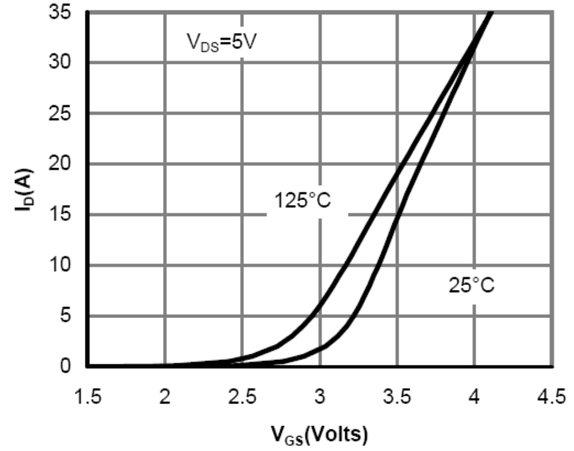

Figure 2: Transfer Characteristics

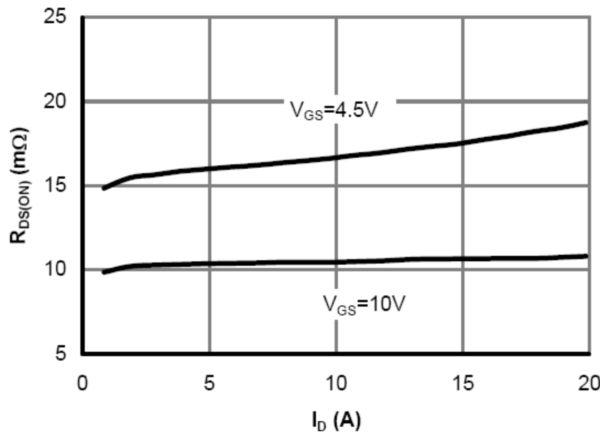

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

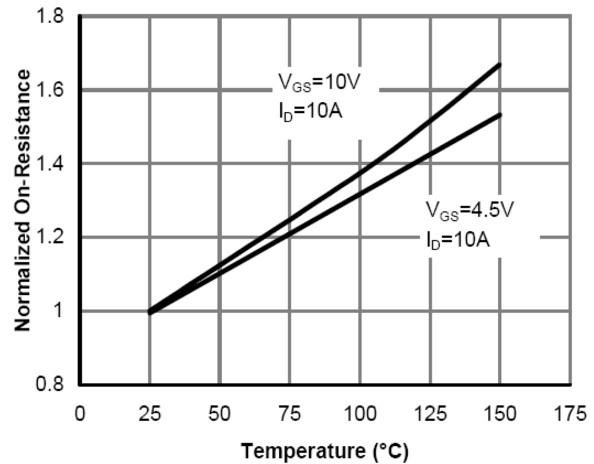

Figure 4: On-Resistance vs. Junction Temperature

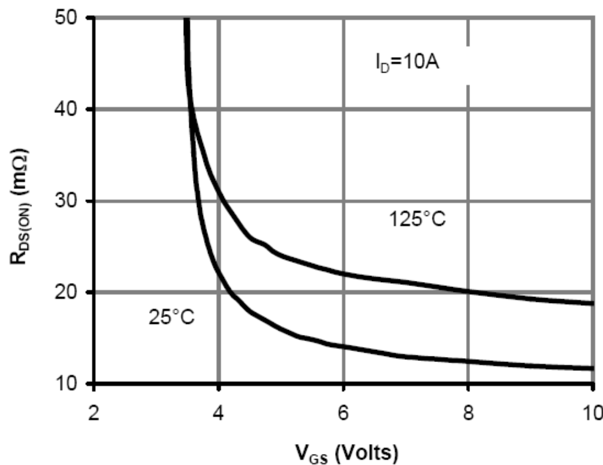

Figure 5: On-Resistance vs. Gate-Source Voltage

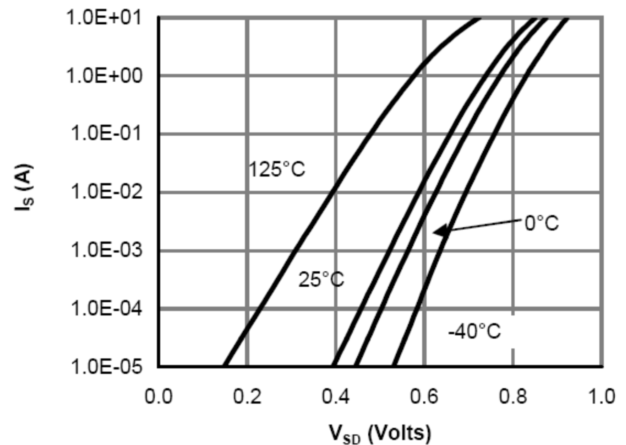

Figure 6: Body-Diode Characteristics

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N Channel TYPICAL CHARACTERISTICS *(continuous)*

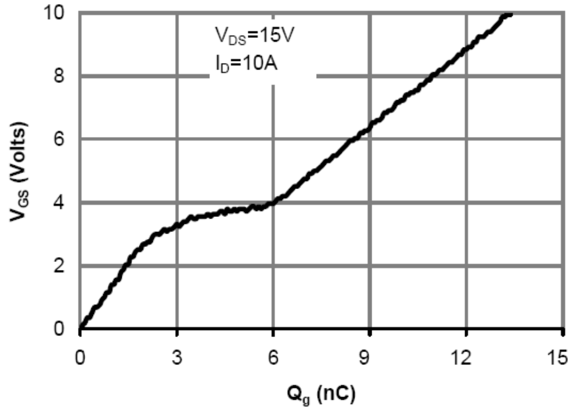

Figure 7: Gate-Charge Characteristics

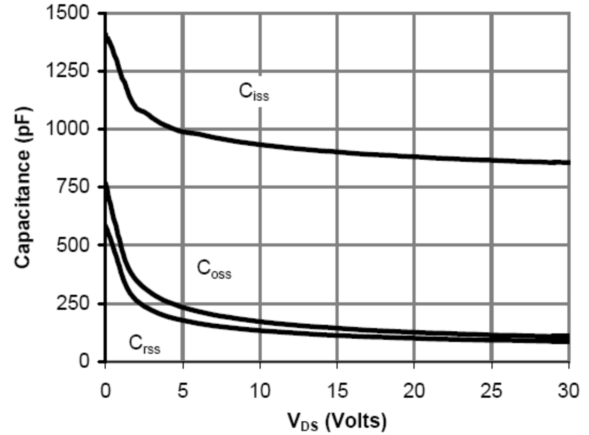

Figure 8: Capacitance Characteristics

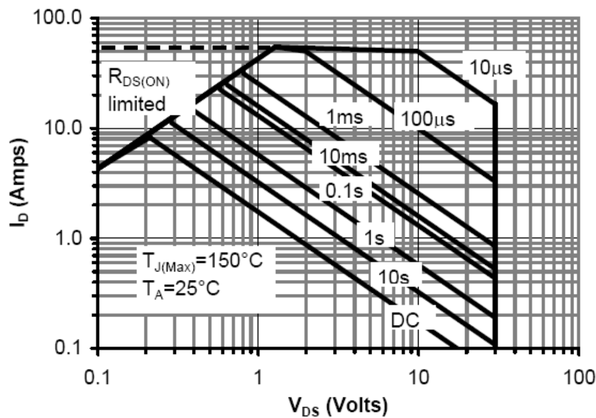

Figure 9: Maximum Forward Biased Safe Operating Area

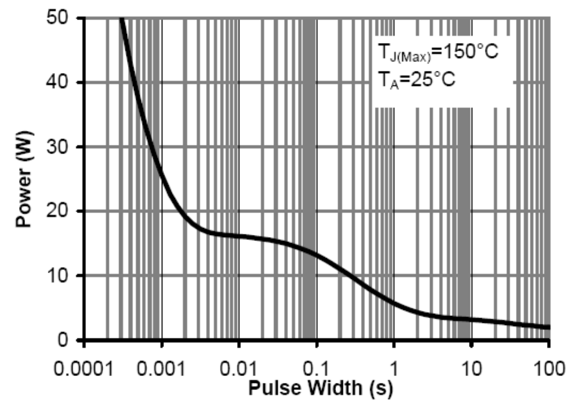

Figure 10: Single Pulse Power Rating Junction-to-Ambient

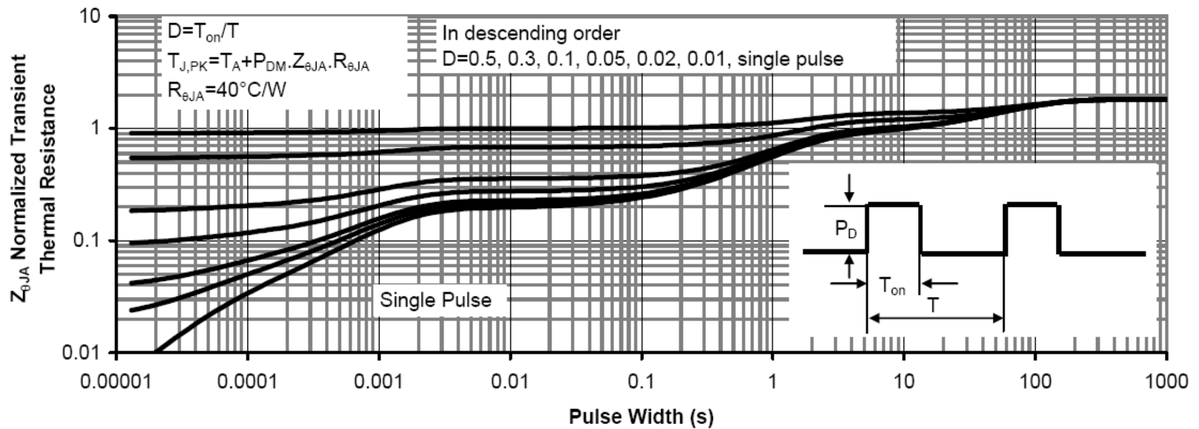

Figure 11: Normalized Maximum Transient Thermal Impedance

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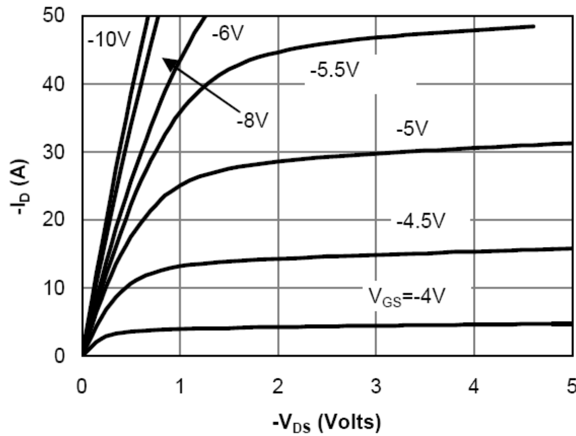
■ *P Channel TYPICAL CHARACTERISTICS (25℃ Unless Note)*



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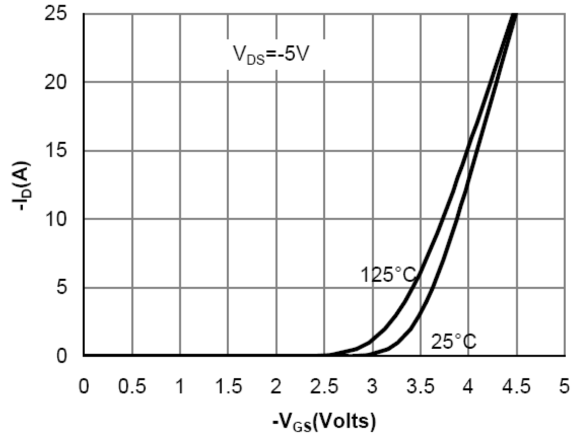

Figure 2: Transfer Characteristics

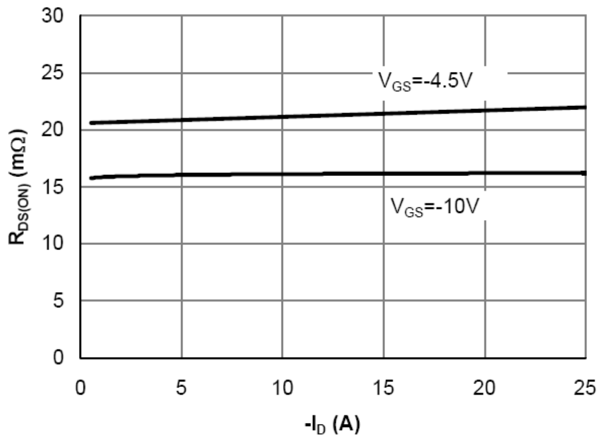

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

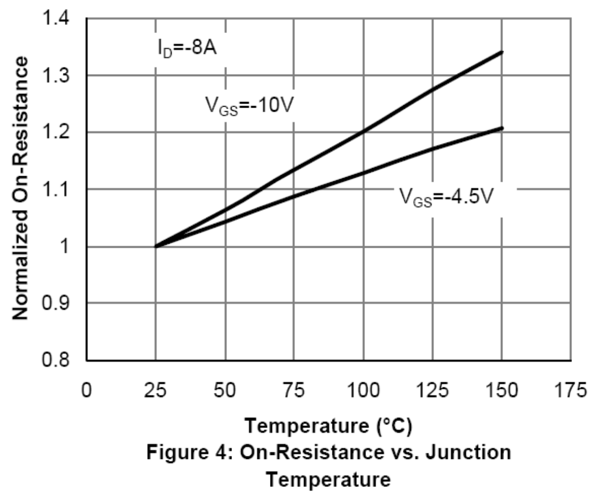

Figure 4: On-Resistance vs. Junction Temperature

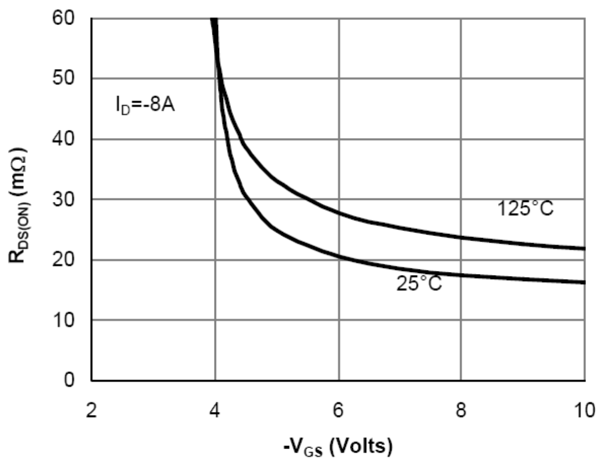

Figure 5: On-Resistance vs. Gate-Source Voltage

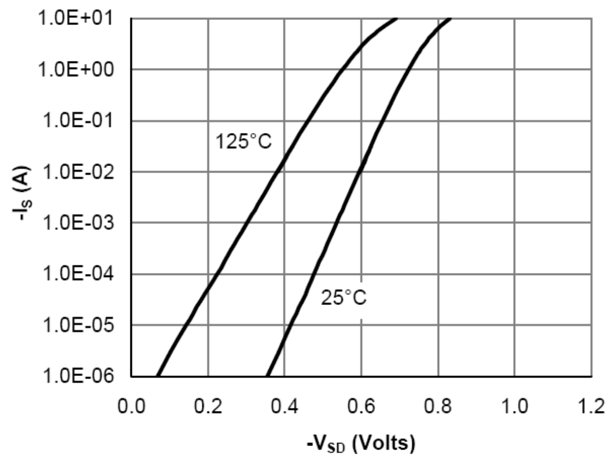

Figure 6: Body-Diode Characteristics

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■ *P Channel TYPICAL CHARACTERISTICS (continuous)*

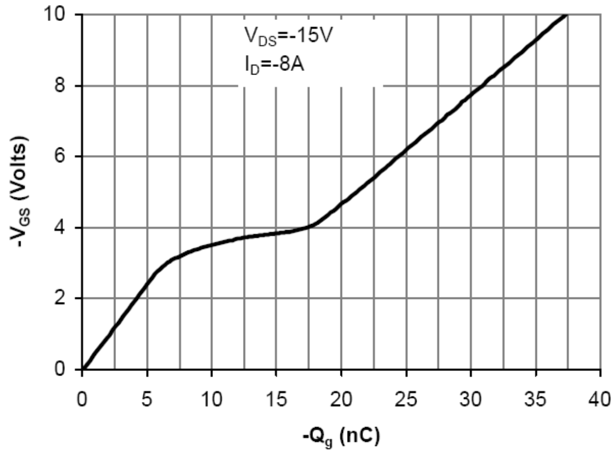
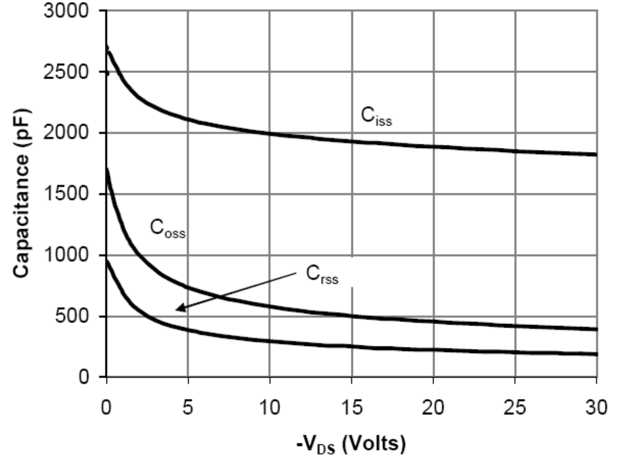


Figure 7: Gate-Charge Characteristics



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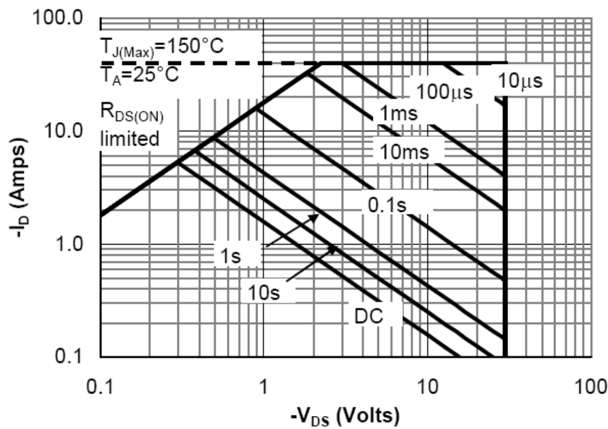

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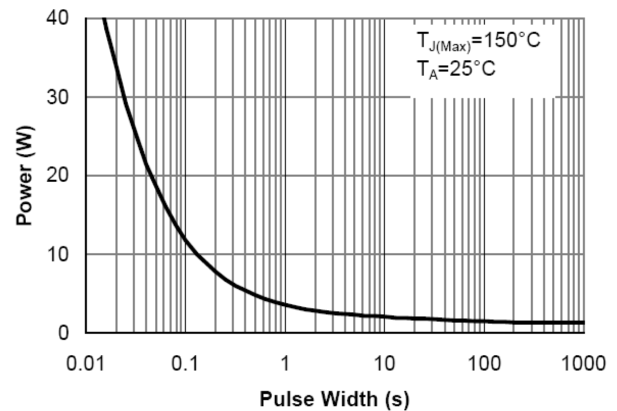

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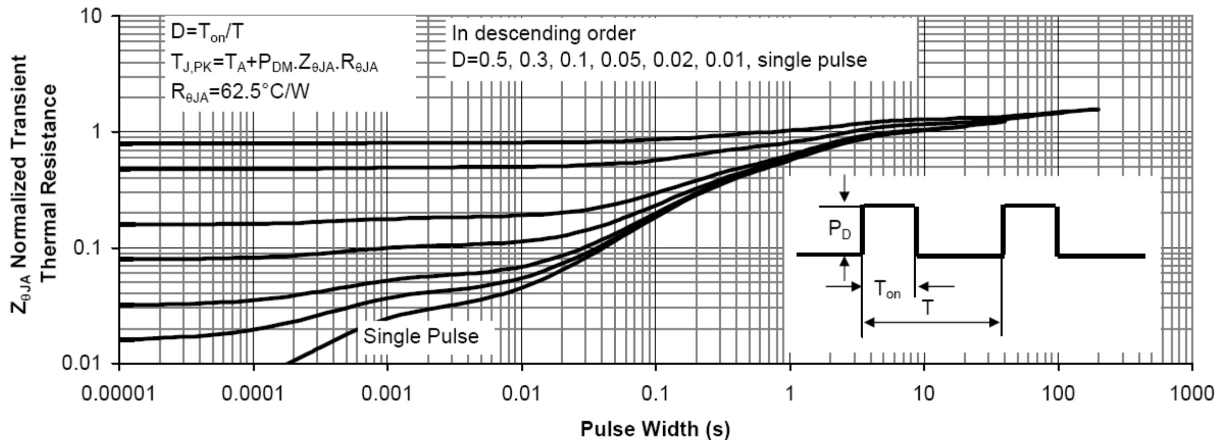

Figure 11: Normalized Maximum Transient Thermal Impedance

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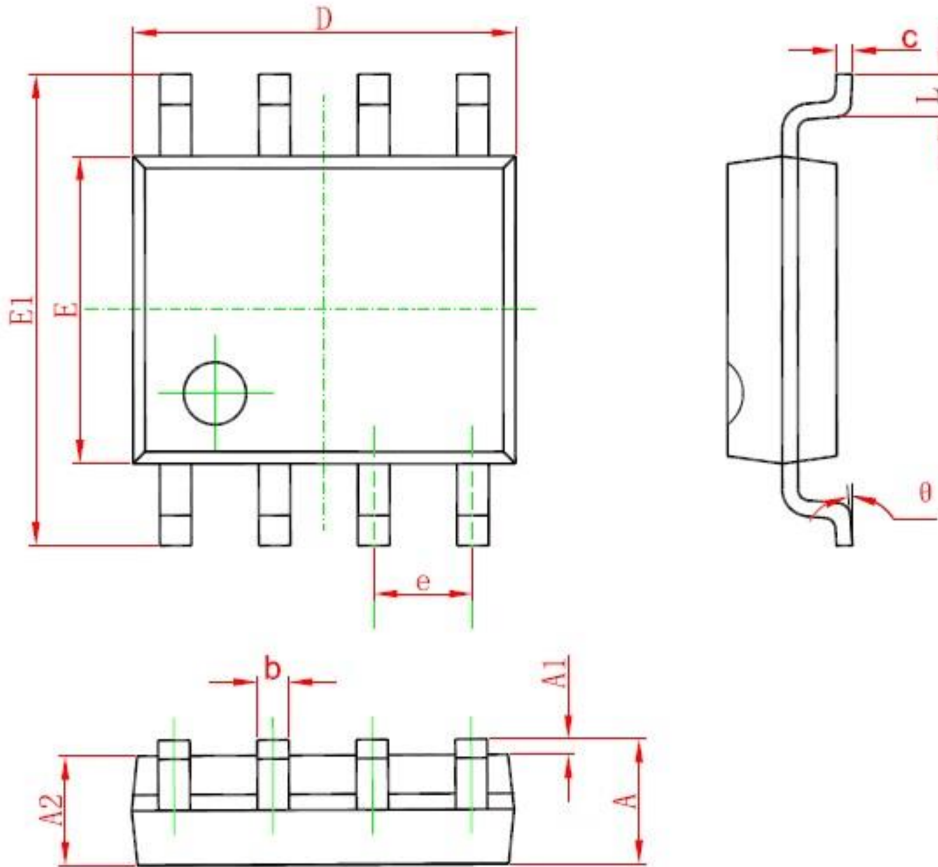
SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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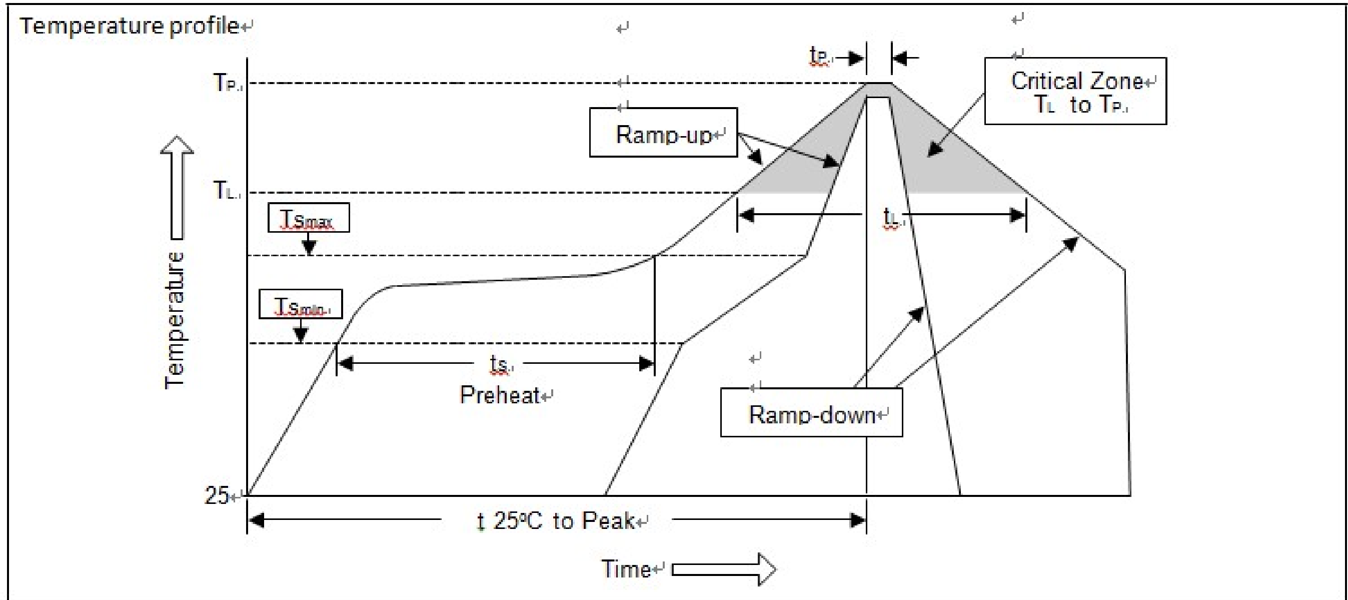
SOLDERING METHODS FOR UNIVERCHIP

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

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Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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