Dual Line ESD Protection Diode Array

UM5062 *QFN3 1.4×1.1*

General Description

The UM5062 ESD protection diode is designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and PDA's. It features large cross-sectional area junctions for conducting high transient currents, offers desirable electrical characteristics for board level protection, such as fast response time, lower operating voltage, lower clamping voltage and no device degradation when compared to MLVs.
The UM5062 ESD protection diode protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events. The UM5062 is available in a QFN3 1.4mm×1.1mm package with working voltages of 5 volt.
It gives designer the flexibility to protect one or two unidirectional line in applications where arrays are not practical. Additionally, it may be "sprinkled" around the board in applications where board space is at a premium. It may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Applications

- Cell Phone Handsets and Accessories
- Microprocessor Based Equipment
  Personal Digital Assistants (PDA's)
- Notebooks, Desktops and Servers
- Portable Instrumentation
- Cordless Phones
- Digital Cameras
- Peripherals
- MP3 Players

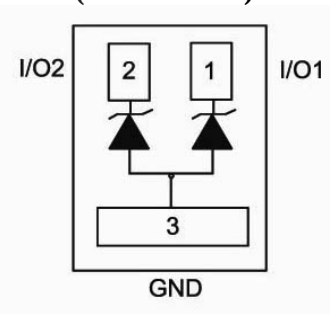
Features

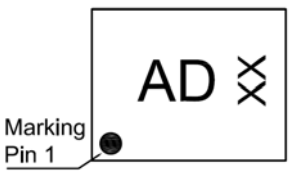
- Transient Protection for Data & Power Lines to IEC 61000-4-2 (ESD) ±15kV (Air), ±8kV (Contact)
- Small Package for Use in Portable Electronics
- Suitable Replacement for MLV's in ESD Protection Applications
- Protect One or Two I/O Lines
- Low Clamping Voltage
- Stand-off Voltages: 5V
- Low Leakage Current
- Solid-State Silicon-Avalanche Technology

Pin Configurations

Top View

(Bottom View)





XX: Week Code
UM5062
QFN3 1.4×1.1

Ordering Information

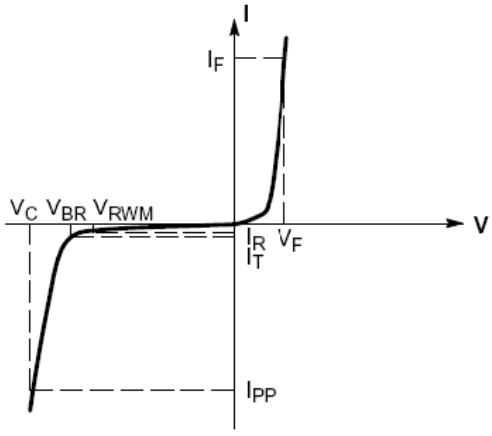
Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5062	5.0V	QFN3 1.4×1.1	2	AD	3000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

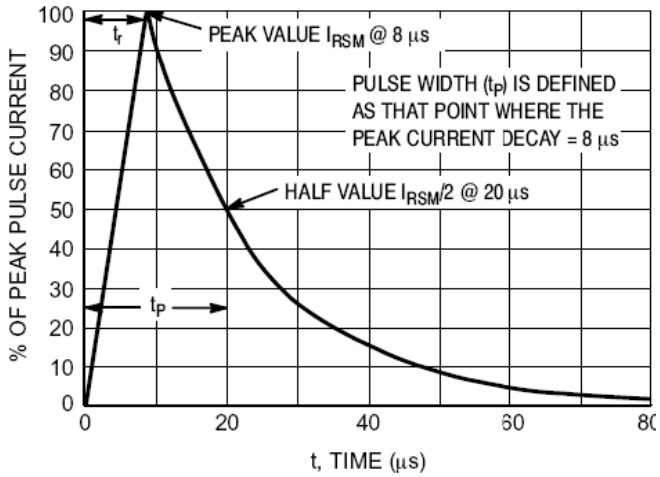
Rating	Symbol	Value	Unit
Peak Pulse Power (t_P=8/20μs)	P_{PK}	140	Watts
Maximum Peak Pulse Current (t_P=8/20μs)	I_{PP}	11	Amps
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Symbol Definition

Parameter	Symbol
Maximum Reverse Peak Pulse Current	I_{PP}
Clamping Voltage @ I_{PP}	V_C
Working Peak Reverse Voltage	V_{RWM}
Maximum Reverse Leakage Current @ V_{RWM}	I_R
Breakdown Voltage @ I_T	V_{BR}
Test Current	I_t
Forward Current	I_F
Forward Voltage @ I_F	V_F
Peak Power Dissipation	P_{PK}
Max. Capacitance @ V_R=0V, f=1MHz	C



Uni-Directional TVS



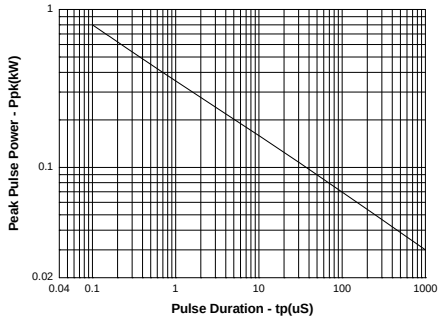
Electrical Characteristics

(T=25°C, Device for 5.0V Reverse Stand-off Voltage)

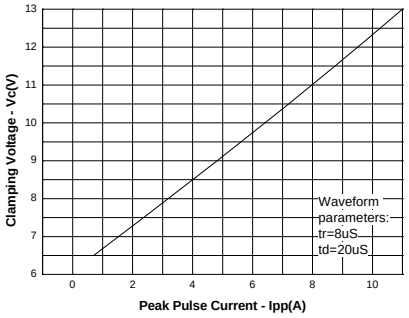
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	6	6.8	7.2	V
Reverse Leakage Current	I_R	V_{RWM}=5V, T=25°C			0.1	μA
Clamping Voltage	V_C	I_{PP}=5A, t_P=8/20μs			9.1	V
		I_{PP}=11A, t_P=8/20μs			13	
Forward Voltage	V_F	I_F=10mA		0.8		V
Junction Capacitance	C_J	V_R=0V, f=1MHz		40	55	pF
Junction Capacitance	C_J	V_R=2.5V, f=1MHz		30	40	pF

Typical Operating Characteristics

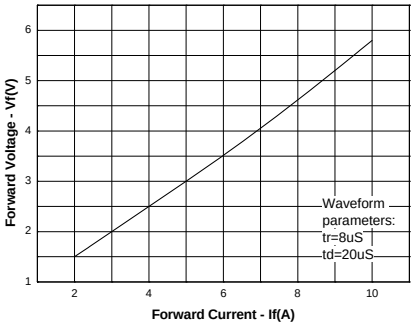
Non-Repetitive Peak Pulse Power vs. Pulse Time



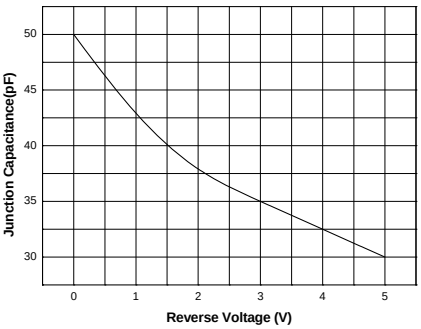
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Junction Capacitance vs. Reverse Voltage



Applications Information

Device Connection Options

UM5062 ESD protection diode is designed to protect one or two I/O lines. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode band should be placed towards the line that is to be protected.

Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
7. Keep parallel signal paths to a minimum.
8. Avoid running protection conductors in parallel with unprotected conductor.
9. Minimize all printed-circuit board conductive loops including power and ground loops.
10. Avoid using shared transient return paths to a common ground point.

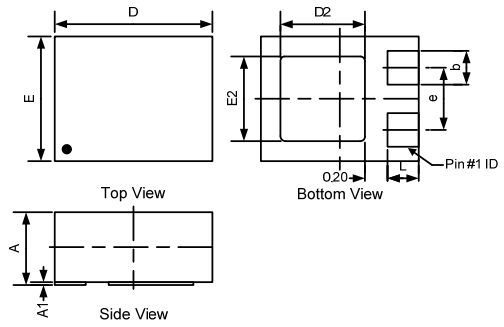
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Package Information

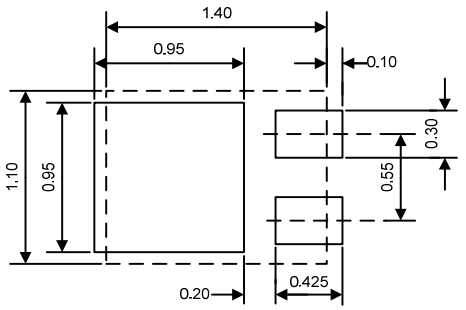
UM5062 QFN3 1.4×1.1

Outline Drawing



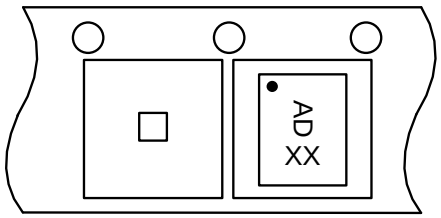
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.47	0.50	0.53	0.019	0.020	0.021
A1	0.00	0.02	0.05	0.000	0.0008	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.35	1.40	1.475	0.053	0.055	0.058
D2	0.65	0.75	0.85	0.026	0.030	0.033
E	1.05	1.10	1.175	0.041	0.043	0.046
E2	0.65	0.75	0.85	0.026	0.030	0.033
e	0.55TYP			0.022TYP		
L	0.225	0.275	0.325	0.009	0.011	0.013

Land Pattern



NOTES:
1. Compound dimension: 1.40×1.10:
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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