UM6104-1

1K × 4 CMOS SRAM

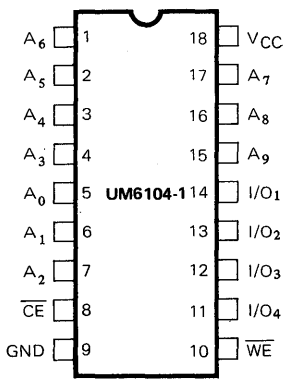
Features

- 2.5V minimum operating voltage
- Low power standby
- Low power operation
- Chip access time: 2.0 μs
- Data retention: 2.0V min.
- Three-state outputs
- On-chip address register
- Synchronous circuitry
- Standard 18 pin DIP package
- No clock required (complete static circuit)

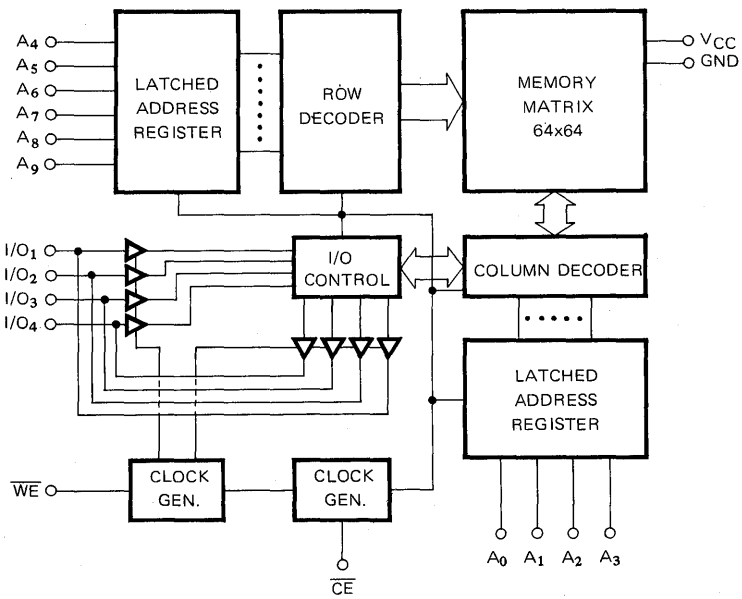
General Description

The UM6104-1 is a nonclocked CMOS static RAM organized as 1024 words by 4-bits. Since 1Kx4 CMOS static RAM is usually used in low voltage or low power consumption situation, such as telephonic equipments and portable equipments, UMC creates a new product version, UM6104-1 to serve these requirements. UM6104-1 dissipates very little current at the data retention mode and is suitable for use in non-volatile RAM applications with battery backup.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Ambient temperature under bias, T_A . . . . . −10 to +80°C
Storage temperature, T_{ST} . . . . . − 55 to +125°C
Input voltage, V_{IN} . . . . . −0.3 to V_{CC} +0.3V
Output voltage, V_{OUT} . . . . . −0.3 to V_{CC} +0.3V
Maximum power supply voltage, V_{CC} max. . . . . +7.0V

*Comments

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

D.C. Electrical Characteristics

(T_A = 0 to 70°C, GND = 0V, V_{CC} = 2.5 to 5.5V unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
V_{CC}	Supply Voltage		2.5	3.0	5.5	V
V_{IL}	Input Low Voltage		−0.3	–	0.4	V
V_{IH}	Input High Voltage		2.2	–	V_{CC} +0.3	V
I_{CCSB}	Standby Supply Current	$\overline{CE}$ = V_{CC}, I_{OUT} = 0mA V_{IN} = GND or V_{CC}			3.0	μA
I_{CCOP}	Operation Supply Current	f = 400 KHz, I_{OUT} = 0mA V_{IH} = V_{CC} V_{IL} = GND			5.0	mA
I_{CCDR}	Data Retention Supply Current	V_{CC} = $\overline{CE}$ = 1.5V I_{OUT} = 0mA V_{IN} = GND or V_{CC}			1.0	μA
V_{CCDR}	Data Retention Supply Voltage	$\overline{CE}$ = high	1.5			V
I_{LI}	Input Leakage Current	GND V_{IN} V_{CC}	−1.0	–	1.0	μA
I_{LO}	Output Leakage Current	GND V_{OUT} V_{CC}	−1.0	–	1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4			V

Capacitance

(T_A = 25°C f = 400 KHz)

Symbol	Parameter	Test Conditions	Limits		Unit
			Typ.	Max.	
C_{IN}	Input Capacitance	All pins except pin under		7	pF
C_{OUT}	Output Capacitance	test tied to AC ground		10	pF

Note:
This parameter is periodically sampled and is not 100% tested.

A.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 2.5 to 5.5V)

Symbol		Parameter	Limits		Units
Conventional	Standard		Min.	Max.	
t_{CA}	T_{ELQV}	Chip enable access time		2.0	μs
t_{COE}	T_{ELQX}	Chip enable output enable time		100	ns
t_{COZ}	T_{EHQZ}	Chip enable output disable time		500	ns
t_{WOZ}	T_{WLQZ}	Write enable output disable time		500	ns
$t_{\overline{CE}}$	T_{ELEH}**	Chip enable pulse negative width	2.0		μs
t_{CE}	T_{EHEL}	Chip enable pulse positive width	500		ns
t_{AS}	T_{AVEL}	Address setup time	100		ns
t_{AH}	T_{ELAX}	Address hold time	0		ns
t_{RS}	T_{WHEL}	Read setup time	0		ns
t_{RH}	T_{EHWL}	Read hold time	0		ns
t_{RD}	T_{ELWL}	Read enable time	2.0		μs
t_{WS}	T_{WLEL}	Write setup time	−100		ns
t_{WD}	T_{ELWH}	Write enable time	2.0		μs
t_{DS}	T_{DVEH}	Input data setup time	1.5		μs
t_{DH}	T_{EHDX}	Input data hold time	0		ns
t_{OH}	T_{EHQX} / T_{WLQX}	Output data hold time	0		ns
t_{C}*	T_{ELEL}	Read or write cycle time	2.5		μs

Notes:

*: $T_{ELEL} = T_{ELEH} + T_{EHEL} + T_R + T_F$

**: For Read Modify Write cycle, $T_{ELEH} = T_{ELWL} + T_{WLEH} + T_F$

AC Test Conditions

Input pulse levels: 0.6V to 2.4V

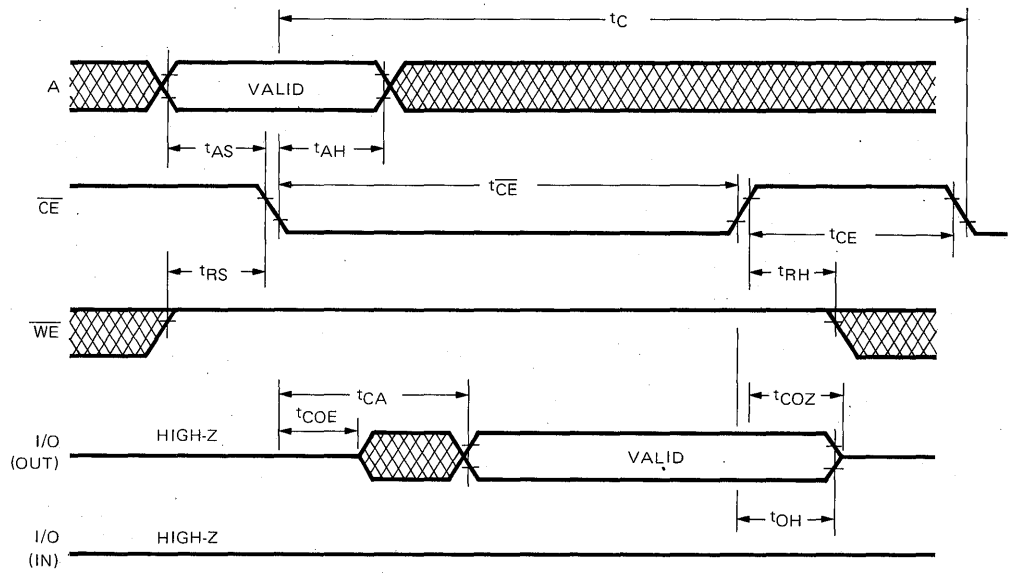
Input pulse rise & fall times (T_R & T_F): 10 ns

Timing measurement levels: input: V_{IL} = 0.8V V_{IH} = 2.2V

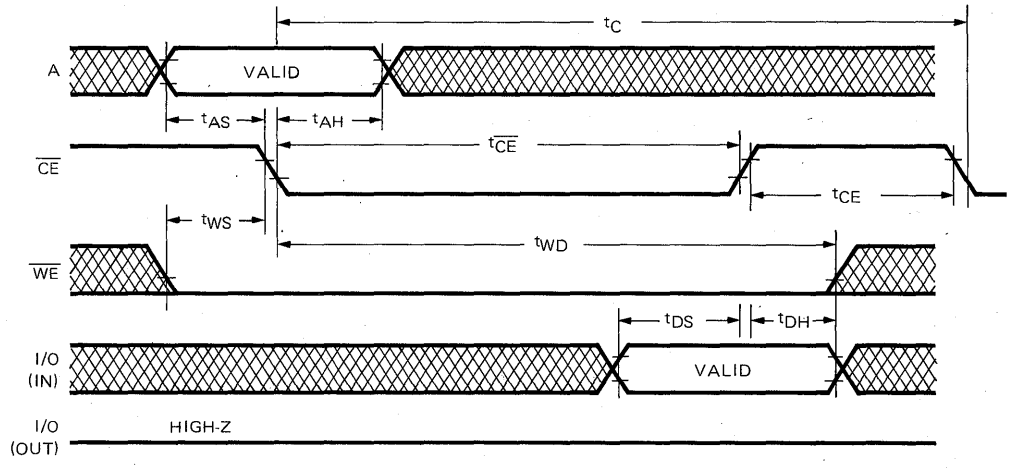
output: V_{OL} = 0.6V V_{OH} = 2.4V

Output load: 1 TTL GATE and C_L = 100 pF

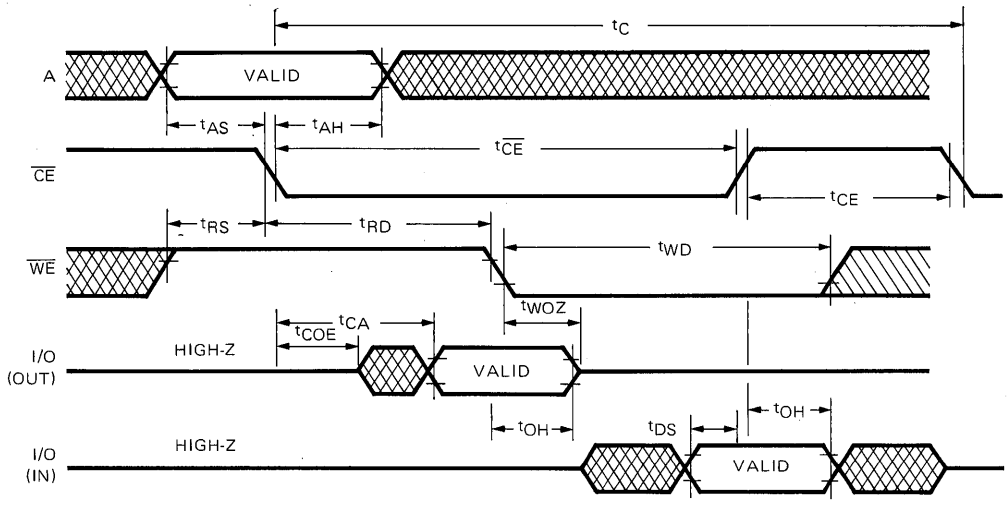
READ CYCLE TIMING DIAGRAM



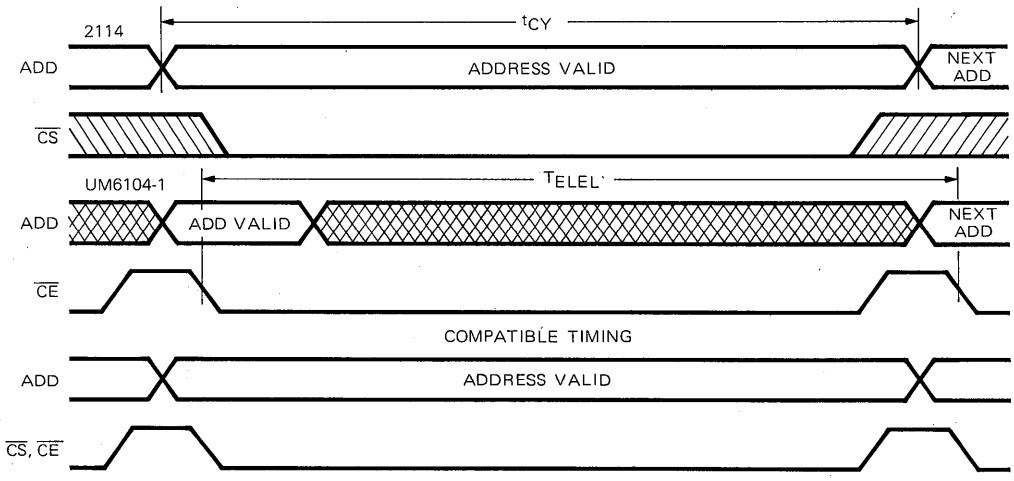
WRITE CYCLE TIMING DIAGRAM



READ MODIFY WRITE CYCLE TIMING DIAGRAM



2114 COMPATIBILITY



2114 – REQUIRES THE ADDRESS TO REMAIN VALID THROUGHOUT THE CYCLE.

UM6104-1 – REQUIRES VALID ADDRESS FOR ONLY A SMALL PORTION OF THE CYCLE, BUT REQUIRES $\overline{CE}$ t_C FALL TO INITIATE EACH CYCLE.

SRAM