UM6104

1K × 4 CMOS SRAM

Features

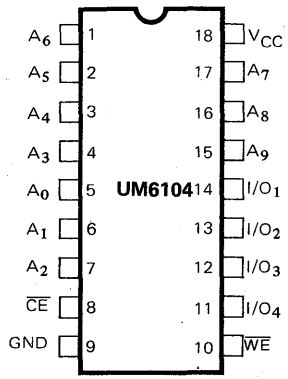
- Single + 5V power supply
- Low power standby
- Low power operation
- Fast Access time . . . . . 120/150/200/250 ns max.
- Data retention . . . . . 2.0V min.
- Three-state outputs
- On-chip address register
- Synchronous circuitry
- Standard 18 pin DIP package
- TTL compatible input/output

General Description

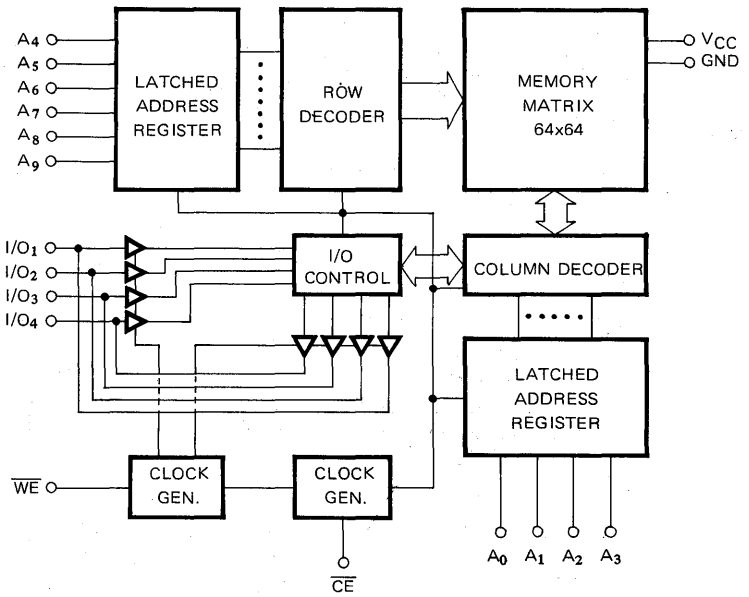
The UM6104 is a 1024x4 fully static CMOS RAM. The device utilizes synchronous circuitry to achieve performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Ambient temperature under bias, T_A . . . . −10 to +80°C
Storage temperature, T_{ST} . . . . . −55 to +125°C
Input voltage, V_{IN} . . . . . −0.3 to V_{CC} +0.3V
Output voltage V_{OUT} . . . . . −0.3 to V_{CC} +0.3V
Maximum power supply voltage, V_{CC} max. . . . . +7.0V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

D.C. Electrical Characteristics

(T_A = 0 to 70°C, GND = 0V, V_{CC} = 4.5 to 5.5V unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IL}	Input low voltage		−0.3	–	0.8	V
V_{IH}	Input high voltage		2.4	–	V_{CC} +0.3	V
I_{CCSB}	Standby supply current	$\overline{CE}$ = V_{CC}, I_{OUT} = 0mA V_{IN} = GND or V_{CC}			10	μA
I_{CCOP}	Operation supply current	f = 1 MHZ, I_{OUT} = 0 mA V_{IH} = V_{CC} V_{IL} = GND			7	mA
I_{CCDR}	Data retention supply current	V_{CC} = $\overline{CE}$ = 3V I_{OUT} = 0mA V_{IN} = GND or V_{CC}			5	μA
V_{CCDR}	Data retention supply voltage	$\overline{CE}$ = high	2.0			V
I_{LI}	Input leakage current	GND V_{IN} V_{CC}	−1.0	–	1.0	μA
I_{LO}	Output leakage current	GND V_{OUT} V_{CC}	−1.0	–	1.0	μA
V_{OL}	Output low voltage	I_{OL} = 3.2mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = −1.0mA	2.4			V

Capacitance

(T_A = 25°C f = 1.0 MHz)

Symbol	Parameter	Test Conditions	Limits		Unit
			Typ.	Max.	
C_{IN}	Input capacitance	All pins except pin under		7	pF
C_{OUT}	Output capacitance	test tied to AC ground		10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. Electrical Characteristics

(T_A = 0 to 70°C, V_{CC} = 4.5 to 5.5V)

Symbol		Parameter	UM6104		UM6104-2		UM6104-3		UM6104-4		Unit
Conventional	Standard		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CA}	T_{ELQV}	Chip enable access time		250		200		150		120	ns
t_{COE}	T_{ELQX}	Chip enable output enable time		50	20		20		10		ns
t_{COZ}	T_{EHOZ}	Chip enable output disable time		80		80		60		50	ns
t_{WOZ}	T_{WLQZ}	Write enable output disable time		80		80		60		50	ns
t_{CE}	T_{ELEH}**	Chip enable pulse engative width	250		200		150		120		ns
t_{CE}	T_{EHEL}	Chip enable pulse positive width	100		80		70		50		ns
t_{AS}	T_{AVEL}	Address setup time	20		20		20		20		ns
t_{AH}	T_{ELAX}	Address hold time	100		80		60		40		ns
t_{RS}	T_{WHEL}	Read setup time	0		0		0		0		ns
t_{RH}	T_{EHWL}	Read hold time	0		0		0		0		ns
t_{RD}	T_{ELWL}	Read enable time	250		200		150		120		ns
t_{WS}	T_{WLEL}	Write setup time	–20		–20		–20		–20		ns
t_{WD}	T_{ELWH}	Write enable time	250		200		150		120		ns
t_{DS}	T_{DVEH}	Input data setup time	200		150		100		70		ns
t_{DH}	T_{EHDX}	Input data hold time	0		0		0		0		ns
t_{OH}	T_{EHQX} / T_{WLQX}	Output data hold time	0		0		0		0		ns
t_{C}*	T_{ELEL}	Read or Write cycle time	350		280		220		170		ns

Notes:

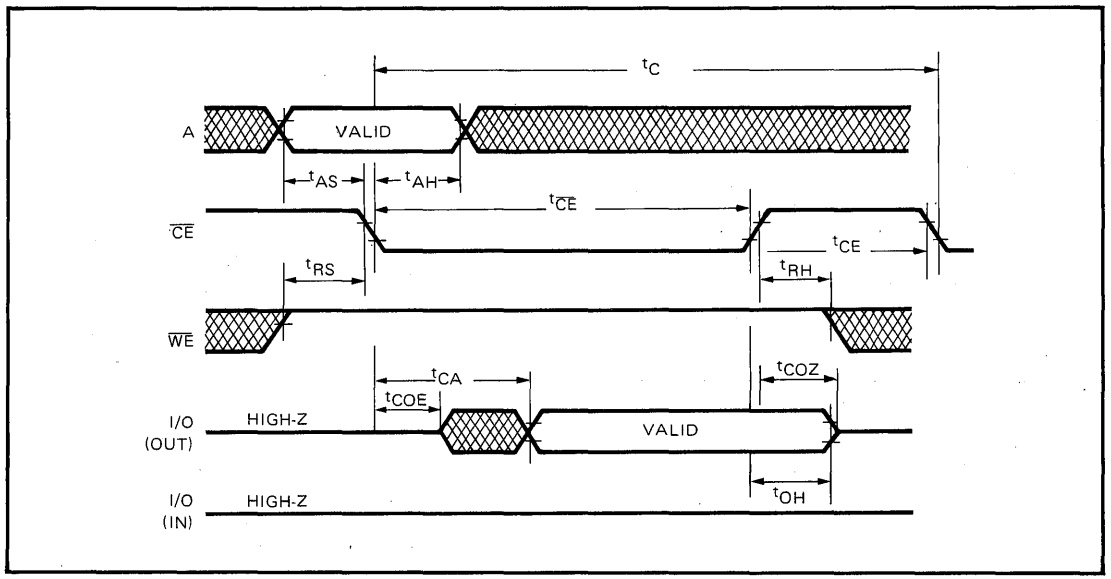
*: $T_{ELEL} = T_{ELEH} + T_{EHEL} + T_R + T_F$

**: For Read Modify Write cycle, $T_{ELEH} = T_{ELWL} + T_{WLEH} + T_F$

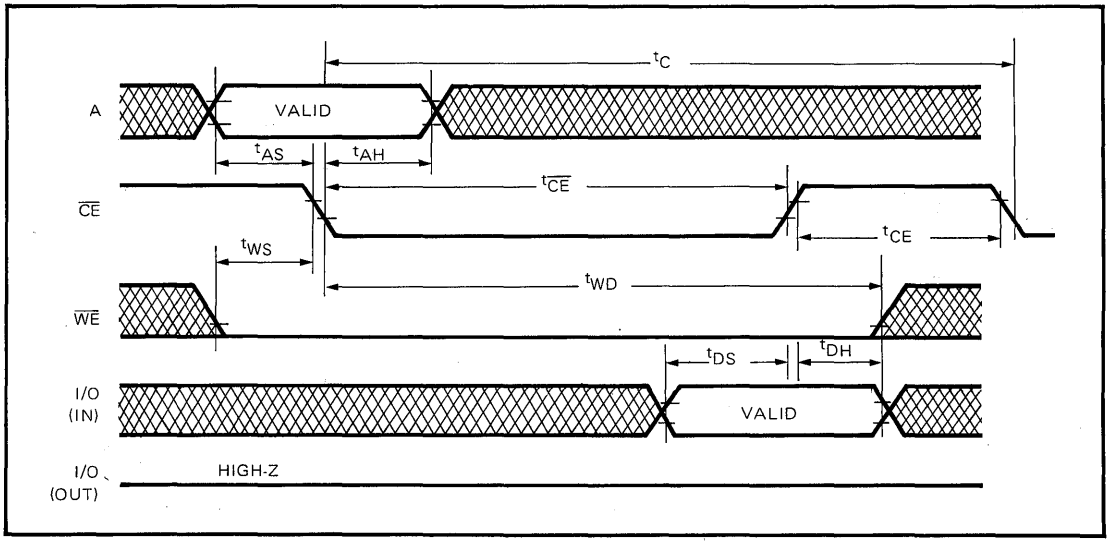
A. C. Test Conditions

Input pulse levels: 0.6V to 2.4V
Input pulse rise & fall times (T_R & T_F): 10 ns
Timing measurement levels: input: V_{IL} = 0.8V V_{IH} = 2.2V
output: V_{OL} = 0.6V V_{OH} = 2.4V
output load: 1 TTL GATE and C_L = 100pF

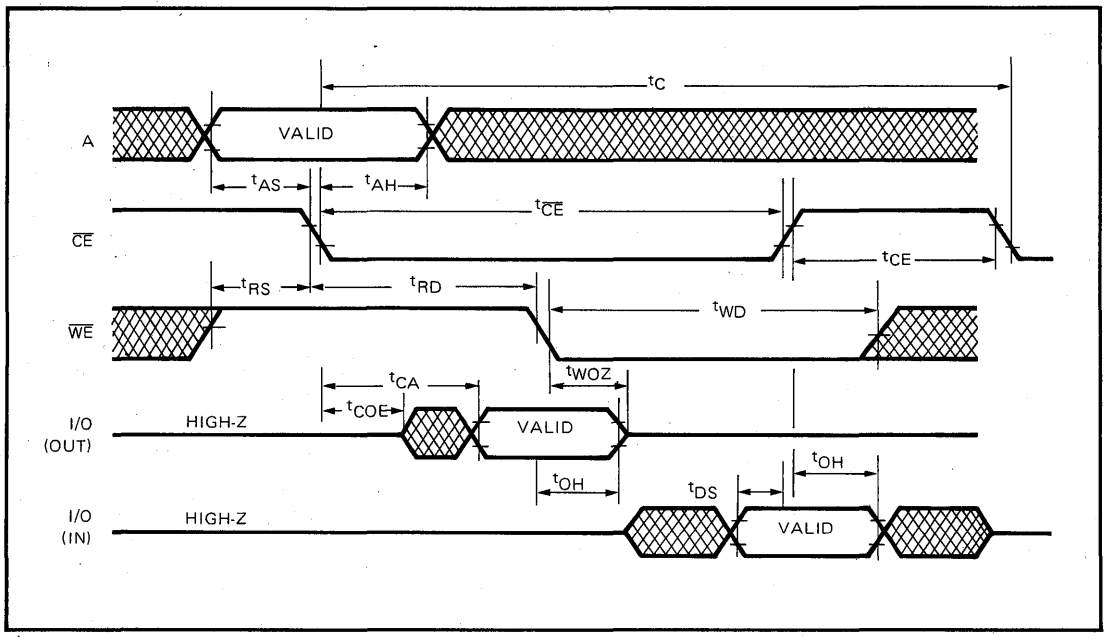
Read Cycle Timing Diagram



Write Cycle Timing Diagram



Read Modify Write Cycle Timing Diagram



Ordering Information

Part Number	Access Time (Max.)	Package
UM6104	250 ns	Plastic
UM6104–2	200 ns	Plastic
UM6104–3	150 ns	Plastic
UM6104–4	120 ns	Plastic
UM6104J	250 ns	CERDIP
UM6104J–2	200 ns	CERDIP
UM6104J–3	150 ns	CERDIP
UM6104J–4	120 ns	CERDIP