UM6114

1K × 4 CMOS SRAM

Features

- High speed—45/55/70/90 ns (max.)
- Low power dissipation:
  50mW (Typ.) operating
  5μW (Typ.) standby
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0—5.5V

General Description

The UM6114 is a 4,096 bit high speed and low power static random access memory organized as 1,024 words by 4 bits using CMOS technology, and operates from a single 5-volt supply.

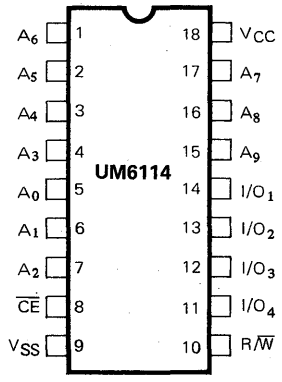
The UM6114 is compatible with the industry produced NMOS 2148 type 4K RAM, yet offers a more than 90% reduction in power of their NMOS equivalents.

The UM6114 is a fully CMOS RAM, therefore it is suited for use in low power applications where battery operation and battery back up for nonvolatility are required.

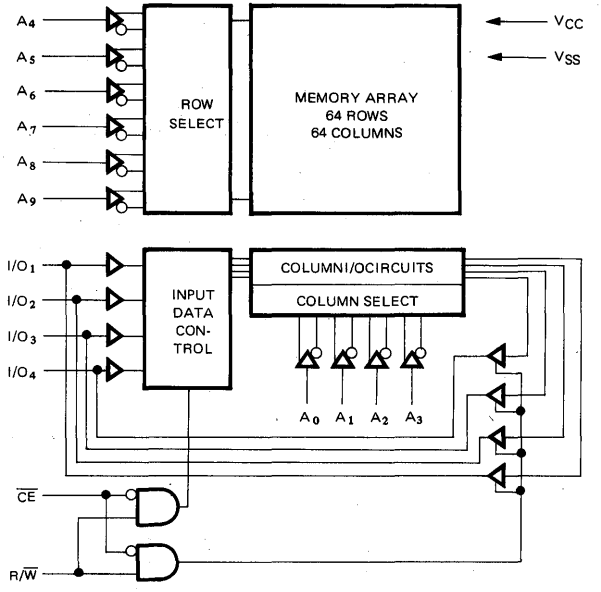
The UM6114 is guaranteed for data retention at a power supply as low as 2 volts. The UM6114 is directly TTL compatible in all inputs and outputs.

The UM6114 is offered in both standard 18 pin plastic and cerdip packages, 0.3 inches in width.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage V_{CC} -V_{SS} . . . . . −0.3V to 7V
Input Voltage V_{IN} . . . . . −0.3V to 7V
Input/Output Voltage Applied $V_{I/O}$ −0.3V to V_{CC} +0.3V
Temp Under Bias T_{BIAS} Ceramic. . . . . −55°C to 125°C
Temp Under Bias T_{BIAS} Plastic. . . . . −10°C to 85°C
Storage Temperature T_{STG} Ceramic . . −65°C to +150°C
Storage Temperature T_{STG} Plastic . . . . −40°C to +125°C
Power Dissipation P_T 1.0W
DC Output Current I_{OUT} 50mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Pin Names

A_0–A_9	ADDRESS
I/O_1–I/O_4	DATA INPUT/OUTPUT
CE	CHIP ENABLE INPUT
R/$\overline{W}$	READ WRITE CONTROL INPUT
V_{CC}/V_{SS}	POWER SUPPLY TERMINALS

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

SRAM

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC} +0.3	V
V_{IL}	Input Low Voltage	−.3	–	+0.8	V
C_L	Output Load	–	–	30	pF
TTL	Output Load	–	–	1	–

D.C. Electrical Characteristics over the operating range

Symbol	Parameter	Test Conditions	6114-3			6114-2			6114-1			6114			Units
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	–	–	±10	–	–	±10	–	–	±10	–	–	±10	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	–	–	±10	–	–	±10	–	–	±10	–	–	±10	μA
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	–	15	30	–	15	30	–	15	30	–	20	40	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	–	10	–	–	10	–	–	10	–	–	10	–	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle =100%	–	–	50	–	–	50	–	–	50	–	–	50	mA
I_{SB}	Standby Power Current	$\overline{CE}$ = V_{IH}	–	5	10	–	5	10	–	5	10	–	5	10	mA
I_{SB1}		$\overline{CE}$ ≥ V_{CC}−0.2V, V_{IN} ≥ V_{CC}−0.2V or V_{IN} ≤ 0.2V	–	1	20	–	1	20	–	1	20	–	1	200	μA
V_{OL}	Output Low Voltage	I_{OL} = 2.4 mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V

*V_{CC} = 5V, T_A = 25°C

Truth Table

Mode	$\overline{CE}$	$\overline{R/W}$	I/O Operation
Standby	H	X	High Z
Read	L	H	D_{OUT}
Write	L	L	D_{IN}

Capacitance*

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} =0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ =0V	10	pF

* This parameter is periodically sampled and not 100% tested.

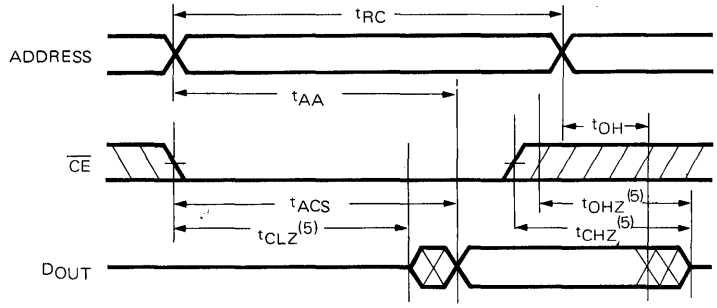
A.C. Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate and C_L = 30pF (Including scope and jig)

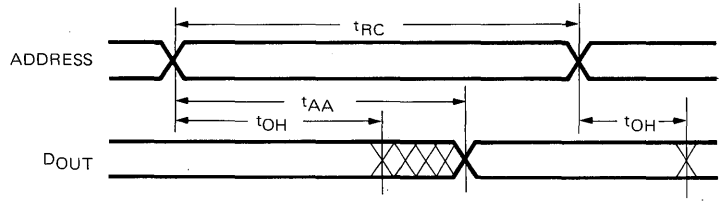
A.C. Electrical Characteristics over the operating range

Symbol	Parameter	6114-3 Min.	6114-3 Max.	6114-2 Min.	6114-2 Max.	6114-1 Min.	6114-1 Max.	6114 Min.	6114 Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	45	–	55	–	70	–	90	–	ns
t_{AA}	Address Access Time	–	45	–	55	–	70	–	90	ns
t_{ACS}	Chip Enable Access Time	–	45	–	55	–	70	–	90	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Enable to Output in High Z	0	30	0	30	0	35	0	40	ns
t_{OHZ}	Output Disable to Output in High Z	0	25	0	30	0	35	0	40	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	45	–	55	–	70	–	90	–	ns
t_{CW}	Chip Enable to End of Write	40	–	40	–	45	–	55	–	ns
t_{AW}	Address Valid to End of Write	40	–	50	–	60	–	80	–	ns
t_{AS}	Address Set-up Time	5	–	5	–	10	–	10	–	ns
t_{WP}	Write Pulse Width	40	–	45	–	45	–	55	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Write to Output in High Z	0	25	0	25	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap	25	–	25	–	30	–	30	–	ns
t_{DH}	Data Hold from Write Time	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	0	–	ns

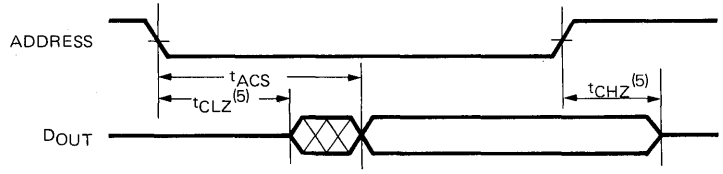
Timing Waveforms of Read Cycle No. 1[1]



READ CYCLE 2[1,2,]

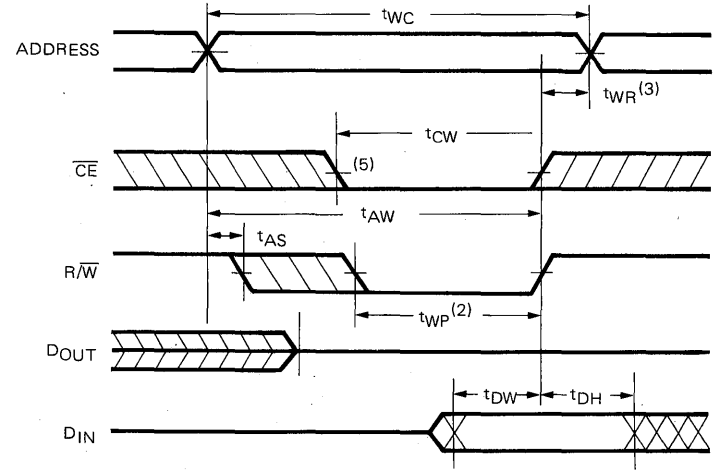


READ CYCLE 3[1,3]

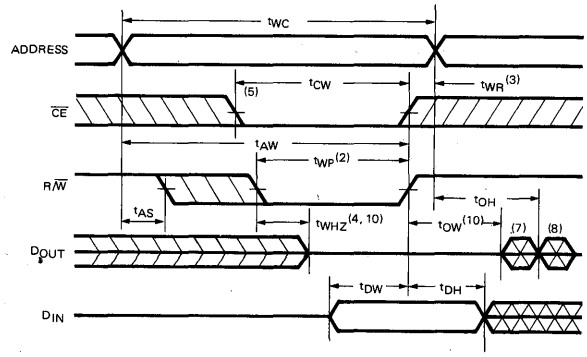


Notes:
1. R/W is High for Read Cycle.
2. Device is continuously selected, $\overline{CE} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Timing Waveforms of Write Cycle 1[1]



WRITE CYCLE 2[1]



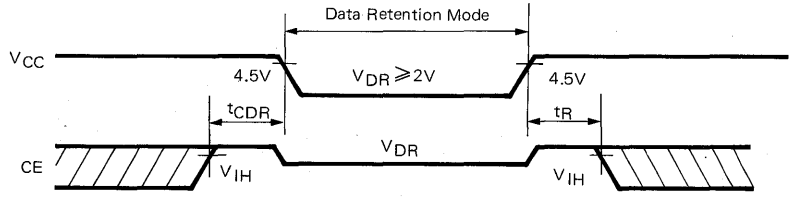
Notes:
1. R/W must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low CE and a low R/W.
3. tWR is measured form the earlier of CE or R/W going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the CE low transition occures simultaneously with the R/W low transitions or after the R/W transition, outputs remain in a high impedance state.
7. Dout is the same phase of write data of this write cycle.
8. Dout is the read data of next address.
9. If CE is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Data Retention Characteristics over the operating temperature range

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
V_{DR}	V_{CC} for Retention Data	$\overline{CE} = V_{CC}$	2.0	–	–	V
I_{CCDR}	Data Retention Current	$V_{IN} = 0V$ or V_{CC}	–	2	20	μA
t_{CDR}	Chip Deselect to Data Retention Time	$V_{CC} = 2.0V$, $\overline{CE} = V_{CC}$	0	–	–	ns
t_R	Operation Recovery Time	$V_{IN} = 0V$ or V_{CC}	t_{RC}[2]	–	–	ns

1. $V_{CC} = 2V$, $T_A = +25°C$
2. I_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



Ordering Information

Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)	Package Type
UM6114	90 ns	30 mA	10 mA	Plastic
UM6114-1	70 ns	30 mA	10 mA	Plastic
UM6114-2	55 ns	30 mA	10 mA	Plastic
UM6114-3	45 ns	40 mA	10 mA	Plastic
UM6114J	90 ns	30 mA	10 mA	CERDIP
UM6114J-1	70 ns	30 mA	10 mA	CERDIP
UM6114J-2	55 ns	30 mA	10 mA	CERDIP
UM6114J-3	45 ns	40 mA	10 mA	CERDIP