UMC

UM6116-5

2K × 8 High Speed CMOS SRAM

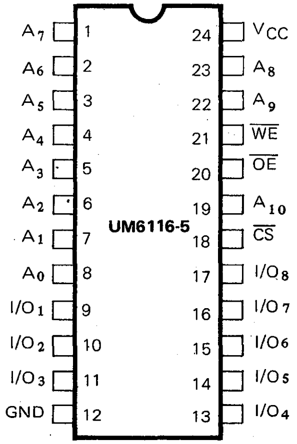
Features

- Single 5V supply and high density 24 pin package
- High speed: Fast access time 55ns (max.)
- Low power standby and Low power operation — Standby: 5μW (typ.), Operation: 250mW (typ.)
- Completely static RAM: No clock or timing strobe required
- Directly TTL compatible: All input and output
- Pin compatible with standard 16K EPROM/Mask ROM
- Equal access and cycle time

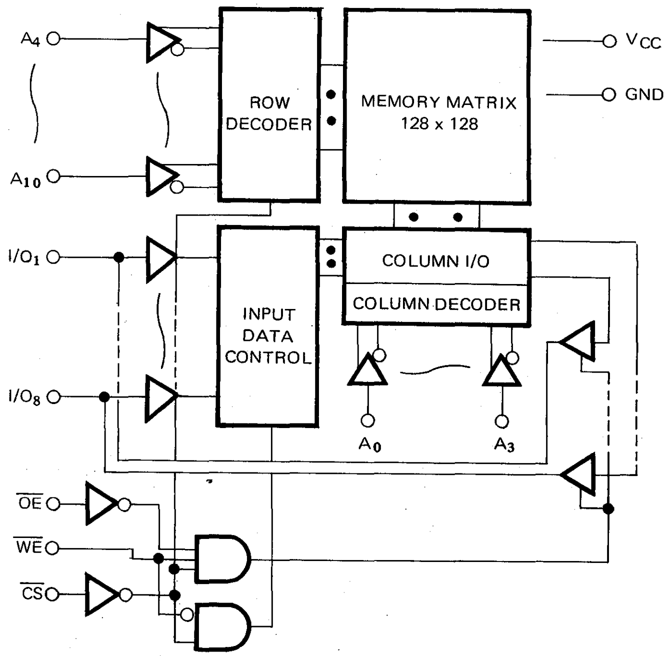
General Description

The UM6116 is a 16,384-bit static random access memory organized as 2048 words by 8 bits and operates from a signle 5 volt supply. It is built with UMC's high performance CMOS process. Six-transistor full CMOS memory cell provides low standby current and high-reliability. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The UM6116 is moulded in a standard 24-pin 600mil-DIP.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Voltage on Any Pin Relative to GND, V_T . −0.3V to +7.0V
Operating Temperature, T_{opr} . . . . 0°C to +70°C
Storage Temperature (Plastic), T_{stg}. . . . −55°C to +125°C
Temperature Under Bias, T_{bias} . . . . −10°C to +85°C
Power Dissipation, P_T 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin
H	x	x	Standby	I_{SB}, I_{SBT}	High Z
L	L	H	Read	I_{CC}	Dout
L	H	H	Read	I_{CC}	High Z
L	x	L	Write	I_{CC}	Din

D.C. and Operating Characteristics

(V_{CC} = 5V ± 5%, GND = 0V, T_A = 0 to +70° C)

Item	Symbol	Test Conditions	6116-5			Units
			Min.	Typ.*	Max.	
Input Leakage Current	I_{LI}	V_{CC}=5.5V, V_{IN}=GND to V_{CC}	–	–	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	–	50	100	mA
	I_{CC1}	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	–	45	–	mA
Dynamic Operating Current	I_{CC2}	Min. cycle, duty=100%	–	–	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–	5	10	mA
	I_{SB1}	$\overline{CS} \geqslant V_{CC}$-0.2V, $V_{IN} \geqslant V_{CC}$ -0.2V or $V_{IN} \leqslant$0.2V	–	1	50	μA
Output Voltage	V_{OL}	I_{OL} = 4mA	–	–	0.4	V
	V_{OH}	I_{OH} = -1.0mA	2.4	–	–	V
Input Voltage	V_{IH}		2.2	3.5	5.8	V
	V_{IL}		-0.3	–	+0.8	V

*V_{CC} = 5V, T_A = 25°C

A.C. Characteristics (V_{CC} = 5V ± 5%, T_A = 0 to +70°C)

A.C. Test Conditions

Input Pulse Levels: 0V to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 30pF (including scope and jig)

READ CYCLE

Item	Symbol	6116-5		Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	55	–	ns
Address Access Time	t_{AA}	–	55	ns
Chip Select Access Time	t_{ACS}	–	55	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	–	ns
Output Enable to Output Valid	t_{OE}	–	35	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	ns
Chip Disable to Output in High Z	t_{OHZ}	0	25	ns
Output Hold from Address Change	t_{OH}	5	–	ns

WRITE CYCLE

Item	Symbol	6116-5		Unit
		Min.	Max.	
Write Cycle Time	t_{WC}	55	–	ns
Chip Selection to End of Write	t_{CW}	40	–	ns
Address Valid to End of Write	t_{AW}	50	–	ns
Address Set Up Time	t_{AS}	5	–	ns
Write Pulse Width	t_{WP}	40	–	ns
Write Recovery Time	t_{WR}	5	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	25	ns
Write to Output in High Z	t_{WHZ}	0	25	ns
Data to Write Time Overlap	t_{DW}	25	–	ns
Data Hold from Write Time	t_{DH}	5	–	ns
Output Active from End of Write	t_{OW}	0	–	ns

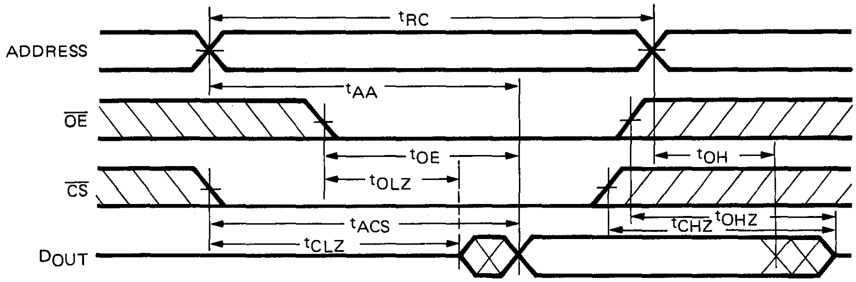
Capacitance* (f = 1MHz, T_A = 25° C)

Item	Symbol	Test Conditions	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF

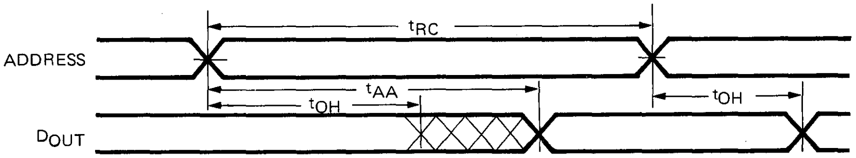
*This parameter is sampled and not 100% tested.

Timing Waveform

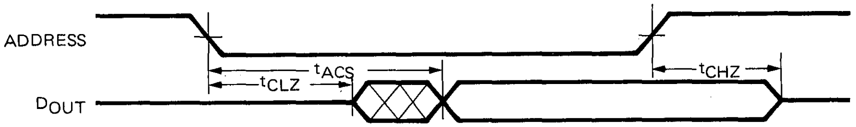
READ CYCLE (1)[1][5]



READ CYCLE (2)[1][2][4]

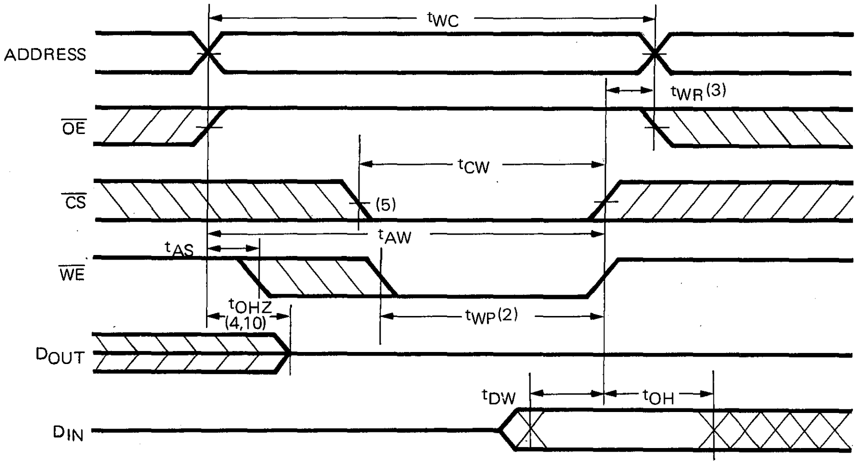


READ CYCLE (3)[1][3][4][5]

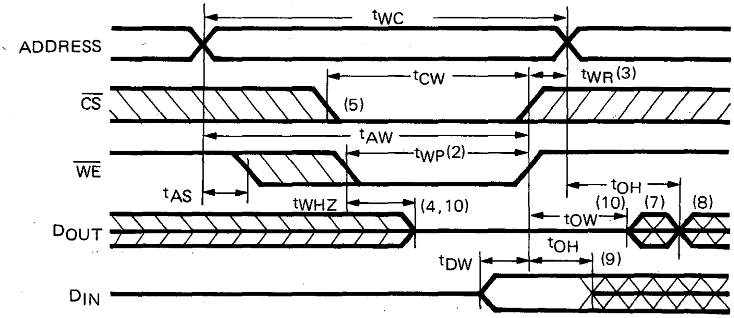


Notes:
1. WE is High for Read Cycle.
2. Device is continuously selected, CS = V_{IL}.
3. Address Valid prior to or coincident with CS transition Low.
4. OE = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE (1)



WRITE CYCLE (2)$^{(1)(6)}$



Notes:

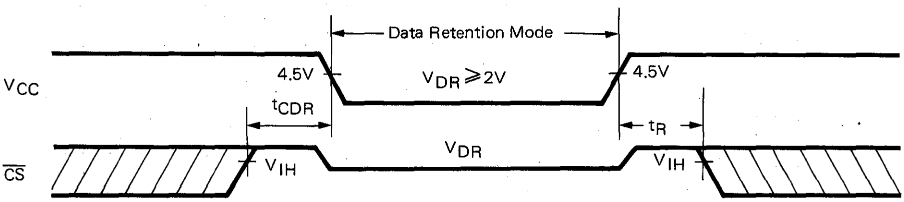
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Data Retention Characteristics over the operating temperature range

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{DR}	V_{CC} for Retention Data	$\overline{CS} = V_{CC}$	2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{IN} = 0V or V_{CC}	–	2	20	μA
t_{CDR}	Chip Deselect to Data Retention Time	V_{CC} = 2.0V, CS = V_{CC}	0	–	–	ns
t_R	Operation Recovery Time	V_{IN} = 0V or V_{CC}	t_{RC} (2)	–	–	ns

1. V_{CC} = 2V, T_A = +25° C
2. I_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



Ordering Information

Part Number	Access Time (Max.)	Package
UM6116-5	55 ns	Plastic
UM6116J-5	55 ns	CERDIP