UMC

T-46-23-12

UMC

# UM61166 Series

PRELIMINARY

## 4K×16 CMOS CACHE RAM

### Features

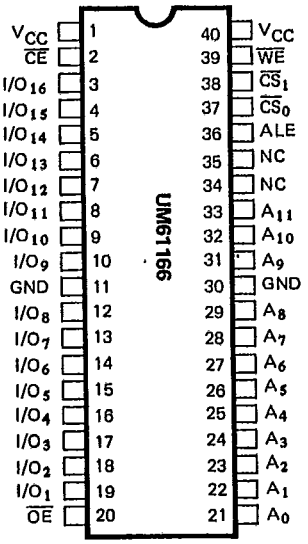
- Single +5V power supply
- Access times: 25/35/45/55 ns (max.)
- Supports high speed 80386 (33/25/20/16 MHz) with fast output enable access times (10/13/15/18 ns)
- Current: Operating: 240 mA (max.)
  Standby: 15 mA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: all inputs and outputs
- Common I/O using three-state output
- Direct interface with Intel cache controller 82385 or IDT 79R3000 RISC CPU or C & T cache controller 82C307
- Supports 80386 pipelined bus cycles with built-in high speed address latch
- Separate enables for upper and lower bytes
- Available in 40 pin DIP or 44 pin PLCC packages

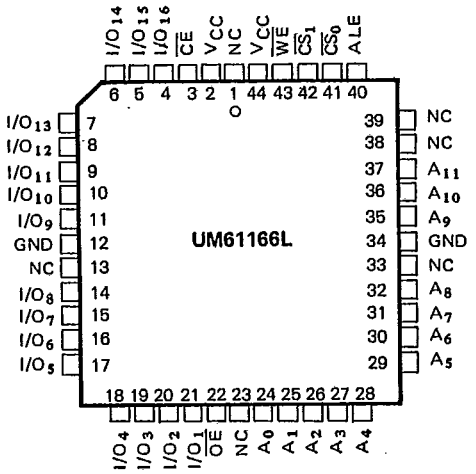
### General Description

The UM61166 is a high performance CMOS static RAM designed to be used as data cache RAM for 80386/82385 and other cache systems operating at speeds up to 33 MHz. Thanks to innovative design techniques, only four UM61166 chips are needed to implement a full 32KB cache without additional address latches or data transceivers for 80386/82385. Fabricated in reliable CMOS double metal process, UM61166 offers a significant reduction in board real estate, power consumption and capacitive loading.

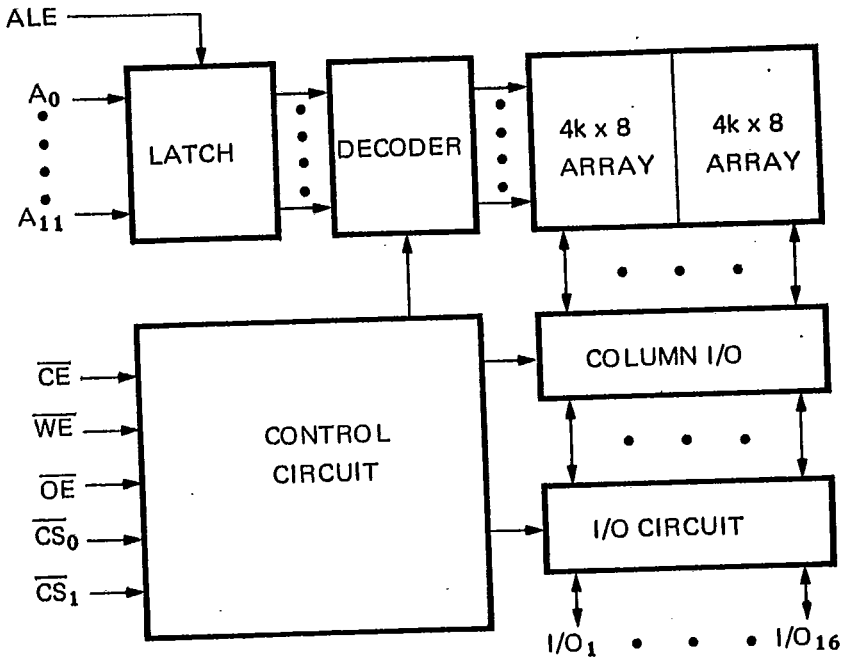
All inputs and outputs of UM61166 are TTL-compatible, and the device operates from a standard 5V supply, simplifying system design. The UM61166 is offered in a 40 pin plastic DIP, or a 44 pin plastic leaded chip carrier, providing high board level packing density.

### Pin Configuration



Block Diagram



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### Pin Description

| Designation | Description |
|---|---|
| ALE | Address Latch Enable |
| $A_0 - A_{11}$ | Address Input |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{CS_1}$ | Chip Select (Higher Byte Enable) |
| $\overline{CS_0}$ | Chip Select (Lower Byte Enable) |
| NC | No Connection |
| $I/O_1 - I/O_{16}$ | Data Input/Output |
| $V_{CC}$ | Power Supply (+5V) |
| GND | Ground |

### Recommended DC Operating Conditions

($T_A$ = 0°C to 70°C)

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.5 | V |
| GND | Ground | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage | −0.5 | +0.8 | V |
| $C_L$ | Output Load | — | 30 | pF |
| TTL | Output Load | — | 1 | — |

### Absolute Maximum Ratings *

$V_{CC}$ to GND ..... −0.5V to +7.0V
IN, IN/OUT Volt to GND ..... −0.5V to $V_{CC}$
Operating Temperature, $T_{opr}$ ..... 0°C to +70°C
Storage Temperature, $T_{stg}$ ..... −65°C to +150°C
Temperature Under Bias, $T_{bias}$ ..... −65°C to + 135°C
Power Dissipation, $P_T$ ..... 1.5W
Soldering Temp. & Time ..... 260°C, 10 sec

### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Electrical Characteristics ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ± 10%, GND = 0V)

| Symbol | Parameter | UM61166-25 | | UM61166-35 | | UM61166-45 | | UM61166-55 | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $\|I_{LI}\|$ | Input Leakage Current | — | 10 | — | 10 | — | 10 | — | 10 | μA | $V_{IN}$ = GND to $V_{CC}$ |
| $\|I_{LO}\|$ | Output Leakage Current | — | 10 | — | 10 | — | 10 | — | 10 | μA | $V_{IN}$ = GND to $V_{CC}$ Output Disabled |
| $I_{CC}$ | Active Power Supply Current | — | 130 | — | 130 | — | 130 | — | 130 | mA | $\overline{CE}$ = $V_{IL}$, $I_{I/O}$ = 0 mA |
| $I_{CC1}$ | Dynamic Operating Current | — | 240 | — | 240 | — | 240 | — | 240 | mA | $\overline{CE}$ = $V_{IL}$, $I_{I/O}$ = 0 mA Min Cycle, Duty = 100% |
| $I_{SB}$ | Standby Power Supply Current | — | 70 | — | 70 | — | 70 | — | 70 | mA | $\overline{CE}$ = $V_{IH}$, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | UM61166-25 Min. | UM61166-25 Max. | UM61166-35 Min. | UM61166-35 Max. | UM61166-45 Min. | UM61166-45 Max. | UM61166-55 Min. | UM61166-55 Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{SB1}$ | Standby Power Supply Current | – | 15 | – | 15 | – | 15 | – | 15 | mA | $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ |
| $I_{OS}$ | Output Short Circuit Current (1) | – | –150 | – | –150 | – | –150 | – | –150 | mA | $V_{I/O}$ = GND |
| $V_{OL}$ | Output Low Voltage | – | 0.5 | – | 0.5 | – | 0.5 | – | 0.5 | V | $I_{OL}$ = 8.0 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | – | 2.4 | – | 2.4 | – | 2.4 | – | V | $I_{OH}$ = –4.0 mA |

Note:

1. Not more than 1 output should be shorted at any time. Duration of output short circuit should not exceed 30 seconds.

## Truth Table

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{CS_1}$ | $\overline{CS_0}$ | I/O Operation | $V_{CC}$ Current |
|---|---|---|---|---|---|---|---|
| Standby | H | X | X | X | X | High Z | $I_{SB}$, $I_{SB1}$ |
| Output Disable | L | X | X | H | H | High Z | $I_{CC}$, $I_{CC1}$ |
| Output Disable | L | H | H | X | X | High Z | $I_{CC}$, $I_{CC1}$ |
| Read Upper Byte | L | L | H | L | H | $D_{OUT}$ | $I_{CC}$, $I_{CC1}$ |
| Read Lower Byte | L | L | H | H | L | $D_{OUT}$ | $I_{CC}$, $I_{CC1}$ |
| Read Word | L | L | H | L | L | $D_{OUT}$ | $I_{CC}$, $I_{CC1}$ |
| Write Upper Byte | L | X | L | L | H | $D_{IN}$ | $I_{CC}$, $I_{CC1}$ |
| Write Lower Byte | L | X | L | H | L | $D_{IN}$ | $I_{CC}$, $I_{CC1}$ |
| Write Word | L | X | L | L | L | $D_{IN}$ | $I_{CC}$, $I_{CC1}$ |

Notes: L: Low, H: High, X: Don't Care

Cache RAM

## Capacitance ($T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V)

| Symbol | Parameter | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| $C_{IN}$* | Input Capacitance | | 12 | pF | $V_{IN}$ = 0V |
| $C_{I/O}$* | Input/Output Capacitance | | 12 | pF | $V_{I/O}$ = 0V |

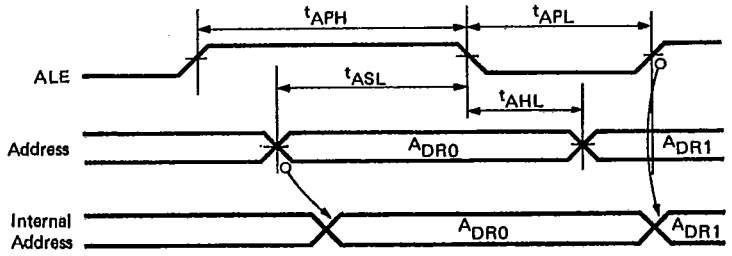
*This parameter is sampled and not 100% tested.

**AC Characteristics** ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ± 10%)

| Symbol | Parameter | UM61166-25 Min. | UM61166-25 Max. | UM61166-35 Min. | UM61166-35 Max. | UM61166-45 Min. | UM61166-45 Max. | UM61166-55 Min. | UM61166-55 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| **Address Latch** | | | | | | | | | | |
| $t_{APH}$ | ALE Pulse Width High | 10 | – | 10 | – | 12 | – | 15 | – | ns |
| $t_{APL}$ | ALE Pulse Width Low | 10 | – | 10 | – | 12 | – | 15 | – | ns |
| $t_{ASL}$ | Address Set-up To Latch Low | 5 | – | 5 | – | 5 | – | 5 | – | ns |
| $t_{AHL}$ | Address Hold from Latch Low | 4 | – | 5 | – | 5 | – | 5 | – | ns |
| **Read Cycle** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 25 | – | 35 | – | 45 | – | 55 | – | ns |
| $t_{AA}$ | Address Access Time | – | 25 | – | 35 | – | 45 | – | 55 | ns |
| $t_{ACE}$ | $\overline{CE}$ Access Time | – | 25 | – | 35 | – | 45 | – | 55 | ns |
| $t_{ACS}$ | Chip Select Access Time | – | 13 | – | 15 | – | 20 | – | 25 | ns |
| $t_{OE}$ | $\overline{OE}$ to Output Valid | – | 10 | – | 13 | – | 15 | – | 18 | ns |
| $t_{CLZ}$ | Chip Selection to Output in Low Z | 3 | – | 3 | – | 3 | – | 3 | – | ns |
| $t_{OLZ}$ | $\overline{OE}$ to Output in Low Z | 2 | – | 2 | – | 2 | – | 2 | – | ns |
| $t_{CHZ}$ | Chip Deselection to Output in High Z | – | 20 | – | 25 | – | 30 | – | 35 | ns |
| $t_{OHZ}$ | Output Disable to Output in High Z | – | 4 | – | 9 | – | 13 | – | 15 | ns |
| $t_{LZ}$ | $\overline{CE}$ to Output in Low Z | 3 | – | 3 | – | 3 | – | 3 | – | ns |
| $t_{HZ}$ | Chip Disable to Output in High Z | – | 20 | – | 25 | – | 30 | – | 35 | ns |
| $t_{OH}$ | Output Hold from Address Change | 3 | – | 3 | – | 3 | – | 3 | – | ns |
| **Write Cycle** | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 25 | – | 35 | – | 45 | – | 55 | – | ns |
| $t_{CW}$ | $\overline{CE}$ to End of Write | 20 | – | 25 | – | 30 | – | 40 | – | ns |
| $t_{AW}$ | Address Valid to End of Write | 25 | – | 35 | – | 45 | – | 55 | – | ns |
| $t_{AS}$ | Address Set-up Time | 0 | – | 0 | – | 0 | – | 0 | – | ns |
| $t_{WP}$ | Write Pulse Width | 17 | – | 25 | – | 30 | – | 40 | – | ns |
| $t_{WR}$ | Write Recovery Time | 0 | – | 0 | – | 0 | – | 0 | – | ns |
| $t_{WHZ}$ | Write Enable to Output in High Z | – | 13 | – | 15 | – | 20 | – | 25 | ns |
| $t_{WLZ}$ | Write Disable to Output in Low Z | 5 | – | 5 | – | 5 | – | 5 | – | ns |
| $t_{DW}$ | Data to Write Time Overlap | 11 | – | 13 | – | 15 | – | 18 | – | ns |
| $t_{DH}$ | Data Hold from End of Write | 0 | – | 0 | – | 0 | – | 0 | – | ns |
| $t_{BW}$ | Chip Select to Write Set-up Time | 20 | – | 25 | – | 30 | – | 40 | – | ns |

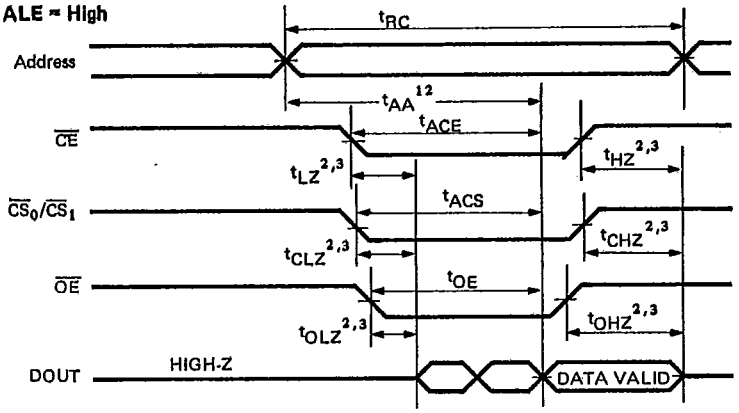
## Timing Waveforms

### Address Latch (1)

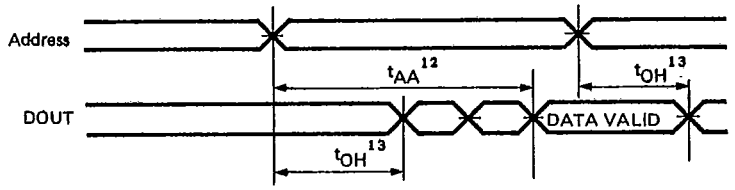



Note: 1. Address Latch must be used together with Read Cycle and Write Cycle or keep ALE high in no address latch mode.

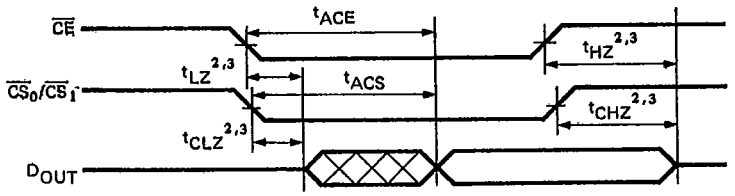
### Read Cycle 1 (1,4) with ALE = High




### Read Cycle 2 (1,4,5,6,7) with ALE = High



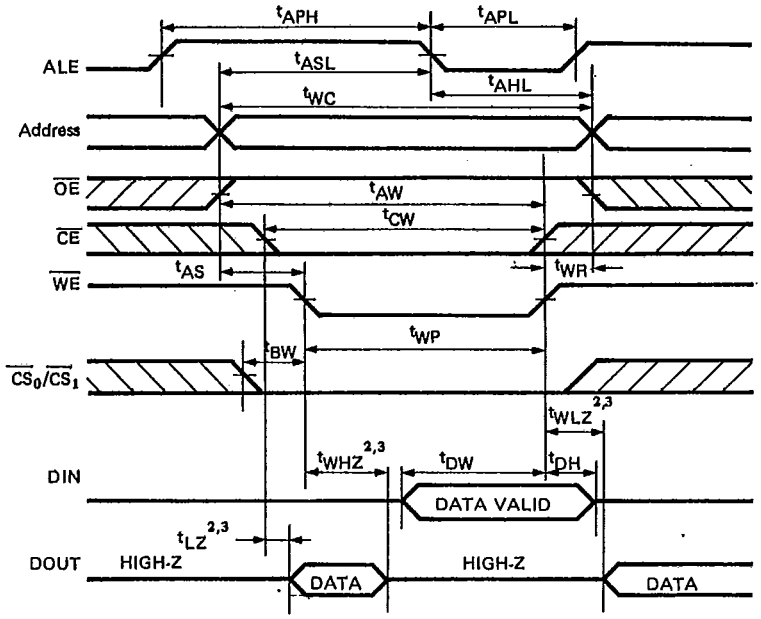

### Read Cycle 3 (1,4,7) with ALE = High



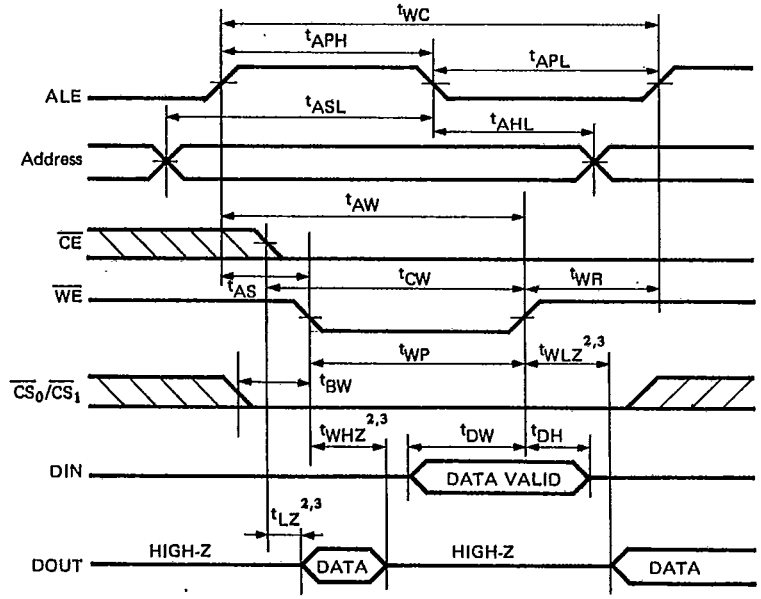

Cache RAM

## Timing Waveforms (Continued)

**Write Cycle 1** (8,9,10,11)




**Write Cycle 2** (7,8,9,11)



Notes:

1. All read cycle timings are referenced from the valid address to the first transitioning address.
2. The parameter is tested with the load in Figure 2. The transition is measured at ± 200mV from steady state voltages.
3. This parameter is not 100% tested.
4. $\overline{WE}$ is high for the read cycle.
5. $\overline{CE}$ is Low.
6. $\overline{CS_0}/\overline{CS_1}$ is Low.
7. $\overline{OE}$ is Low.
8. A write occurs during the overlap of a low $\overline{CE}$, a low $\overline{CS_0}$ and/or $\overline{CS_1}$, and a low $\overline{WE}$.
9. $\overline{WE}$ must be high during address transistion.
10. If $\overline{OE}$ is high, I/O pins remain in a high impedance state.
11. $\overline{CE}$ must remain static during the write cycle, when $\overline{WE}$ is low. The write cycle can only be controlled by the $\overline{WE}$ pulse.
12. The parameter $t_{AA}$ is measured either from the first low to high transition of ALE after the read address has become valid, or from the stabilization of the read address during the period when ALE is high.
13. The parameter $t_{OH}$ is measured either from the first low to high transition of ALE after the address change, or from the address change during the period when ALE is high.

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | See Fig. 1 and 2 |

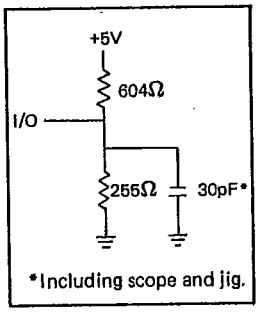



**Figure 1. Output Load**

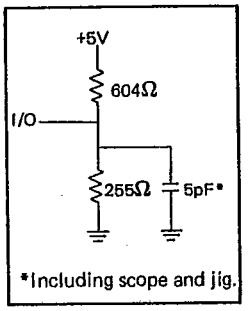



**Figure 2. Output Load for $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{WHZ}$, $t_{WLZ}$, $t_{HZ}$ and $t_{LZ}$.**

Cache RAM

## Ordering Information

| Part No. | Access Time (ns) | Operating Current Max.(mA) | Standby Current Max.(mA) | Package |
|---|---|---|---|---|
| UM61166-25 | 25 | 240 | 15 | 40L DIP |
| UM61166L-25 | 25 | 240 | 15 | 44L PLCC |
| UM61166-35 | 35 | 240 | 15 | 40L DIP |
| UM61166L-35 | 35 | 240 | 15 | 44L PLCC |
| UM61166-45 | 45 | 240 | 15 | 40L DIP |
| UM61166L-45 | 45 | 240 | 15 | 44L PLCC |
| UM61166-55 | 55 | 240 | 15 | 40L DIP |
| UM61166L-55 | 55 | 240 | 15 | 44L PLCC |