UM6164

8K × 8 High Speed CMOS SRAM

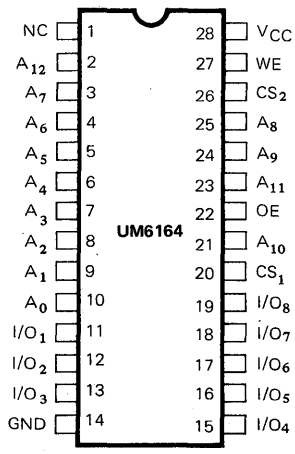
Features

- High-speed – 45/55/70ns (Max.)
- Low power dissipation
  300mW (Typ.) Operating
  100μW (Typ.) standby
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0–5.5V

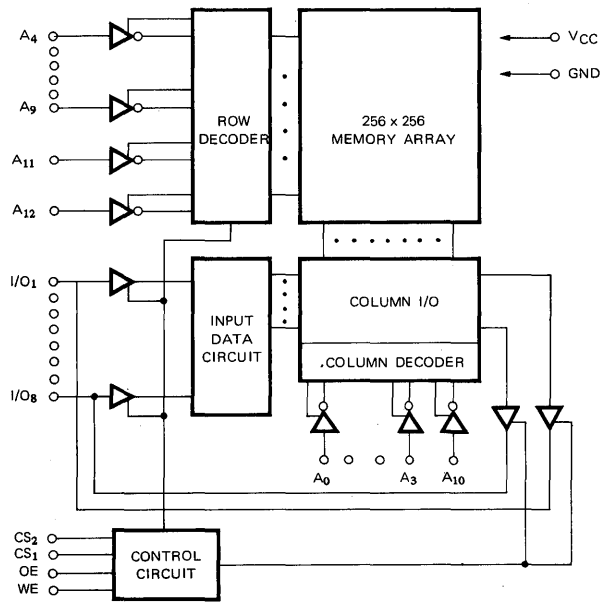
General Description

The UM6164 is a 65,536-bit static random access memory organized as 8192 words by 8 bits and operates from a single 5 volt supply. It is built with UMC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The UM6164 is moulded in a standard 28-pin, 600 mil-DIP.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Terminal Voltage with Respect to
GND (V_{TERM}) . . . . . −0.5V to +7.0V
Temperature Under Bias (T_{BIAS}) . . . . . −10°C to +125°C
Storage Temperature (T_{STG}) . . . . . −40° C to +150°C
Power Dissipation (P_T) 1.0W
DC Output Current (I_{OUT}) . . . . . 20 mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Pin Names

A_0–A_{12}	Address	WE	Write Enable
I/O_1–I/O_8	Data Input/Output	OE	Output Enable
CS_1	Chip Select One	CS_2	Chip Select Two
V_{CC}	Power	GND	Ground

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

D.C. Electrical Characteristics

(V_{CC} = 5V ±10%, GND = 0V, T_A = 0 to 70°C)

Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Units
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}	–	–	5	μA
I_{LO}	Output Leakage Current	$CS_1 = V_{IH}$ or $CS_2 = V_{IL}$ or OE = V_{IH}, $V_{I/O}$ = GND to V_{CC}	–	–	5	μA
I_{CC}	Operating Power Supply Current	$CS_1 = V_{IL}$, $CS_2 = V_{IH}$, $I_{I/O}$ = 0mA	–	50	100	mA
I_{CC1}	Average Operating Current	Min, Duty Cycle = 100%, $CS_1 = V_{IL}$, $CS_2 = V_{IH}$	–	60	120	mA
I_{SB}	Standby Power Supply Current	$CS_1 = V_{IH}$ or $CS_2 = V_{IL}$, $I_{I/O}$ = 0mA	–	5	10	mA
I_{SB1}[2]		$CS_1 \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	–	.02	2	mA
I_{SB2}[2]		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	–	.02	2	mA
V_{OL}	Output Voltage	I_{OL} = 2.1 mA	–	–	0.4	V
V_{OH}		I_{OH} = −1.0mA	2.4	–	–	V

1. Typical limits are at V_{CC} = 5.0V, T_A = 25° C and specified loading.
2. V_{IL} min = −0.3V

Recommended D.C. Operating Conditions

(T_A = 0 to +70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
G_{ND}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5	0	0.8	V

Capacitance (1)

(T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note: This parameter is sampled and not 100% tested.

A.C. Test Conditions

Parameter	Conditions
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output	1.5V
Timing Reference Level	
Output Load	1 TTL Gate and C_L = 30pF (including scope and jig)

SRAM

A.C. Electrical Characteristic

(over the operating range)

Symbol	Parameter		UM6164-2		UM6164-1		UM6164		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Read Cycle Time		45	–	55	–	70	–	
t_{AA}	Address Access Time		–	45	–	55	–	70	ns
t_{ACS1}	Chip Select Access Time	CS_1	–	45	–	55	–	70	ns
t_{ACS2}		CS_2	–	45	–	55	–	70	ns
t_{OE}	Output Enable to Output Valid		–	30	–	35	–	50	ns
t_{CLZ1}	Chip Selection to Output in Low Z	CS_1	5	–	5	–	5	–	ns
t_{CLZ2}		CS_2	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z		5	–	5	–	5	–	ns
t_{CHZ1}	Chip Deselection to Output in High Z	CS_1	0	25	0	30	0	35	ns
t_{CHZ2}		CS_2	0	25	0	30	0	35	ns
t_{OHZ}	Output Disable to Output in High Z		0	25	0	30	0	35	ns
t_{OH}	Output Hold from Address Change		5	–	5	–	5	–	ns
WRITE CYCLE									
t_{WC}	Write Cycle Time		45	–	55	–	70	–	ns
t_{CW}	Chip Selection to End of Write		35	–	40	–	45	–	ns
t_{AS}	Address Setup Time		5	–	5	–	5	–	ns
t_{AW}	Address Valid to End of Write		40	–	50	–	65	–	ns
t_{WP}	Write Pulse Width		35	–	40	–	45	–	ns
t_{WR1}	Write Recovery Time	CS_1, WE	5	–	5	–	5	–	ns
t_{WR2}		CS_2	5	–	10	–	10	–	ns
t_{WHZ}	Write to Output in High Z		0	20	0	25	0	30	ns
t_{DW}	Data to Write Time Overlap		20	–	25	–	30	–	ns
t_{DH}	Data Hold from Write Time		5	–	5	–	5	–	ns
t_{OHZ}	OE to Output in High Z		0	25	0	25	0	25	ns
t_{OW}	Output Active from End of Write		5	–	5	–	5	–	ns

Note:

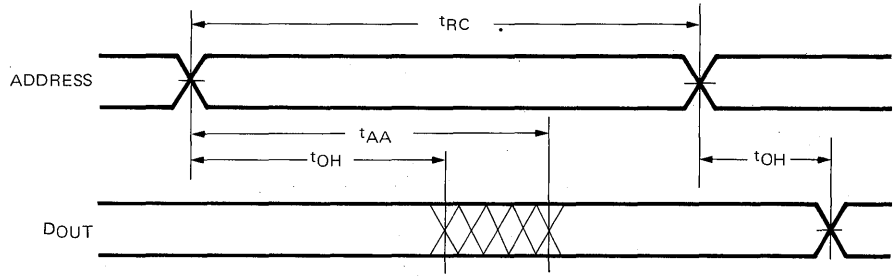
t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Truth Table

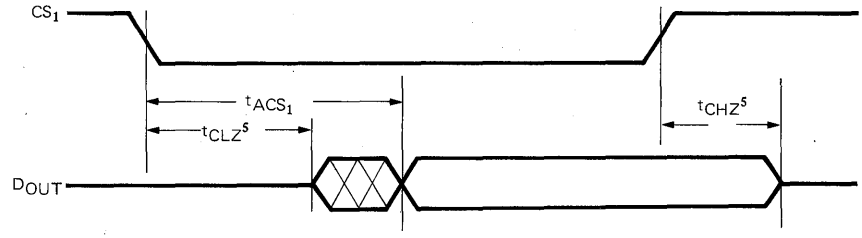
Mode	WE	CS_1	CS_2	OE	I/O Operation	V_{CC} Current	Notes
Not Selected (Power Down)	X	H	X	X	High Z	I_{SB}, I_{SB1}	
	X	X	L	X	High Z	I_{SB}, I_{SB2}	
Output Disabled	H	L	H	H	High Z	I_{CC}, I_{CC1}	
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}	
Write	L	L	H	H	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 1
	L	L	H	L	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 2

Timing Waveforms

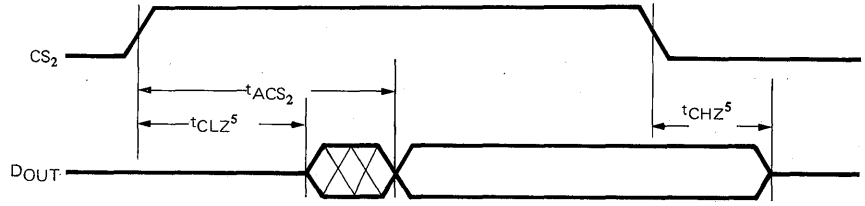
READ CYCLE[1, 2, 4]



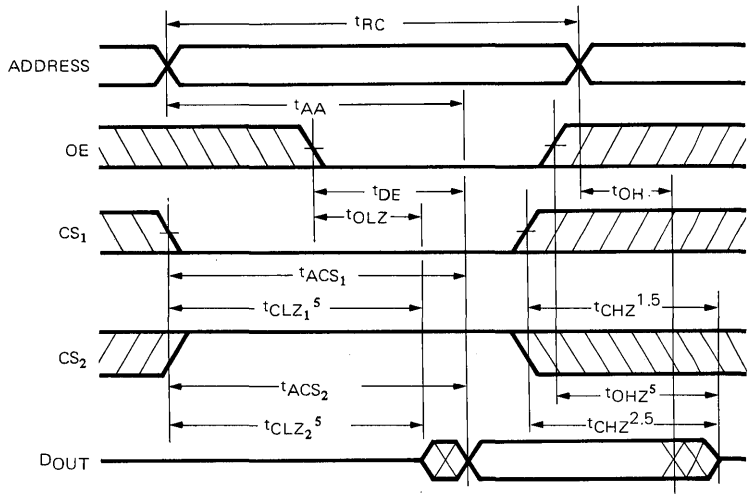
READ CYCLE 2[1, 3, 4, 6]



READ CYCLE 3[1, 4, 7]

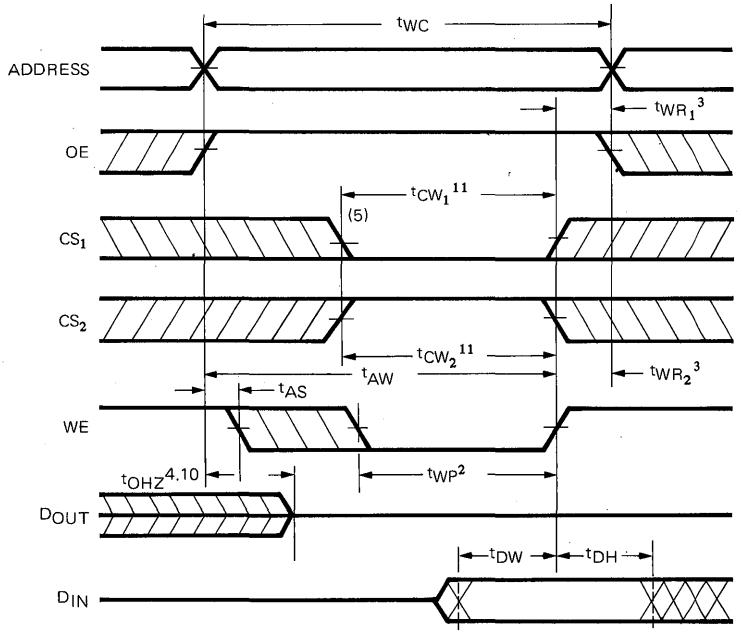


READ CYCLE 4[1]

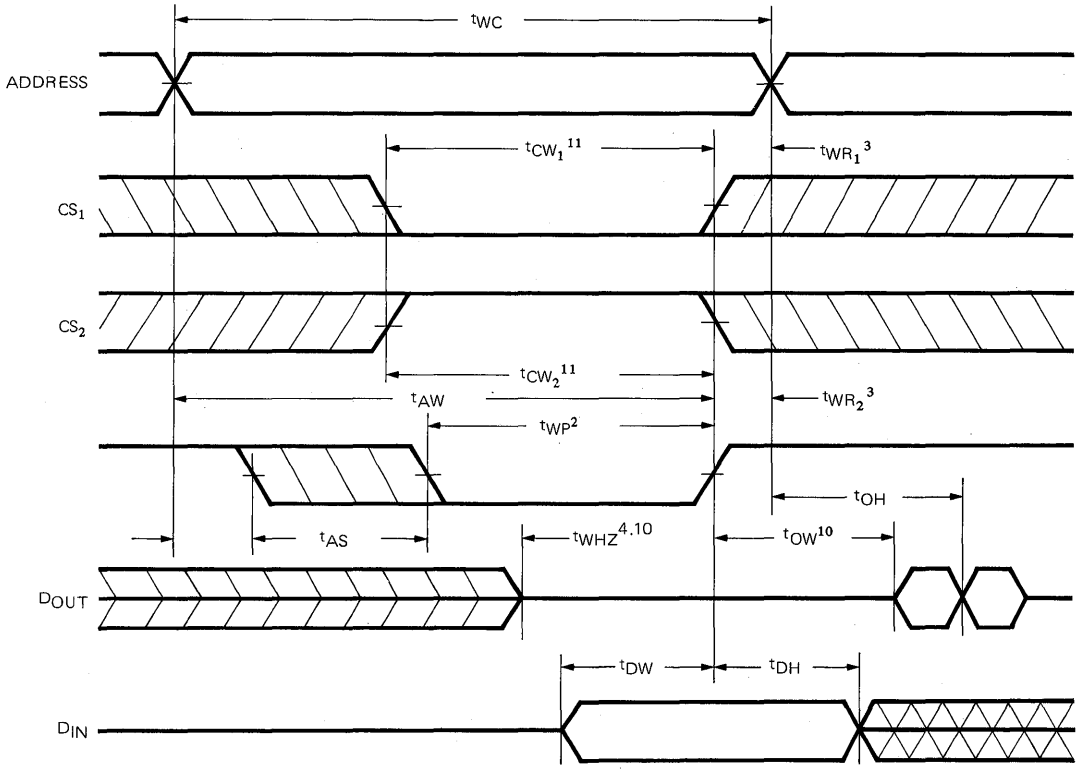


Notes: 1. WE is high for READ cycle.
2. Device is continuously selected $CS_1 = V_{IL}$ and $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with CS_1 transition low.
4. $OE = V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. CS_1 is low.

WRITE CYCLE 1[1]



WRITE CYCLE 2[1, 6]



Notes:

1. WE must be high during address transitions.
2. A write occurs during the overlap (t_{WP}) of a low CS_1 a high CS_2 and a low WE.
3. t_{WR} is measured from the earlier of CS, or WE going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state SQ that the input signals of opposite phase to the outputs must not be applied.
5. If the CS_1 low transition or the CS_2 high transition occurs simultaneously with the WE low transitions or after the WE transition. Outputs remain in a high impedance state.
6. OE is continuously low (OE = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If CS_1 is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
11. t_{CW} is measured from the later of CS_1 going low or CS_2 going high to the end of write.

Data Retention Characteristics

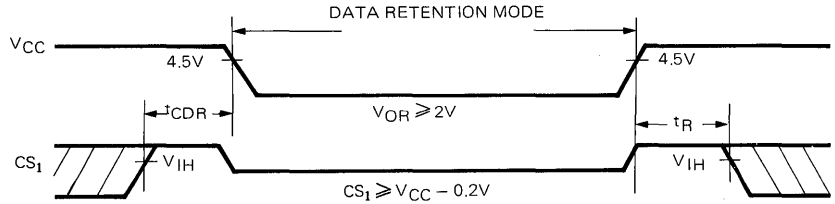
(T_A = 0 to +70°C)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{DR1}	V_{CC} for Data Retention	$CS_1 \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	–	V
V_{DR2}		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	–	V
I_{CCDR1}	Data Retention Current	$CS_1 \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	2	50	μA
I_{CCDR2}		$CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	–	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	–	–	ns
t_R	Operation Recovery Time		t_{RC}(2)	–	–	ns

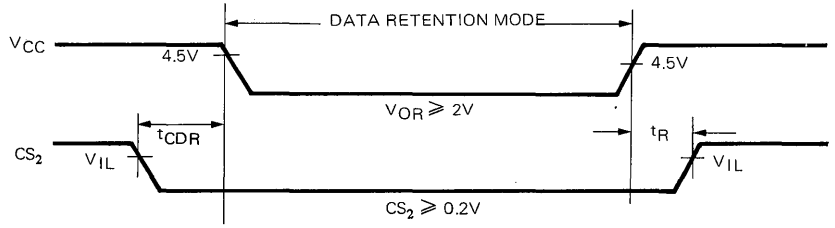
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform

CS_1 CONTROLLED



CS_2 CONTROLLED



Ordering Information

Part Number	Access Time (Max.)	Package
UM6164	70	Plastic DIP
UM6164-1	45	Plastic DIP
UM6164-2	55	Plastic DIP

SRAM