# UM6168

## 4K × 4 High Speed CMOS SRAM



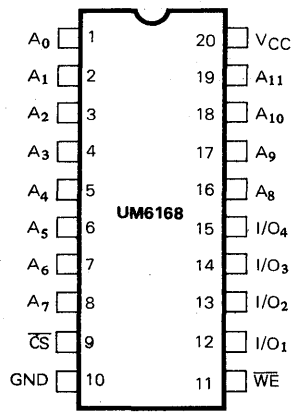
### Features

- High-speed – 35/40/45/55/70 ns
- Low power dissipation
  225mW (typ.) operating
  100μW (typ.) standby
- Single 5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Data retention supply voltage: 2.0 – 5.5V

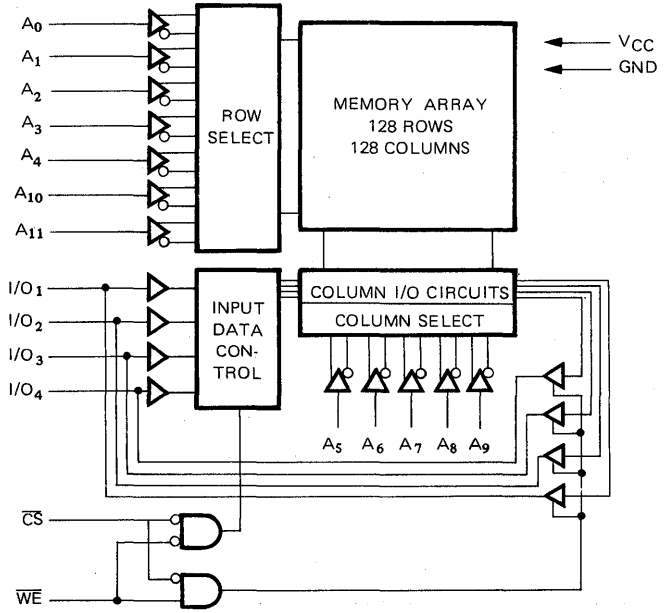
### General Description

The UMC UM6168 is a 16,384 bit static random access memory organized as 4096 words by 4 bits and operates from a single 5 volt supply. It is built with UMC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible. The UM6168 is moulded in a standard 20-pin, 300 mil-DIP.

### Pin Configuration




### Block Diagram



## Absolute Maximum Ratings*

Terminal Voltage with Respect to GND, $V_T$ ..... −0.5V to +7.0V
Operating Temperature, $T_{OPR}$ ..... 0°C to +70°C
Temperature Under Bias, $T_{BLAS}$ ..... −55°C to +125°C
Storage Temperature, $T_{STC}$ ..... −65°C to +150°C
Power Dissipation, $P_T$ ..... 1.0W
DC Output Current, $I_{OUT}$ ..... 20mA

## *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## D.C. Characteristics

($T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ±10%)

| Symbol | Parameter | Test Conditions | UM6168 | | | UM6168L | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = 5.5V, $V_{IN}$ = 0V to $V_{CC}$ | – | – | 2 | – | – | 2 | μA |
| $\|I_{LO}\|$ | Output Leakage Current | $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = 0V to $V_{CC}$ | – | – | 2 | – | – | 2 | μA |
| $I_{CC1}$ | Operating Power Supply Current | $\overline{CS}$ = $V_{IL}$, Output Open | – | 30 | 60 | – | 25 | 50 | mA |
| $I_{CC2}$ | Dynamic Operating Current | Min. Duty Cycle = 100% | – | 30 | 60 | – | 25 | 50 | mA |
| $I_{SB}$ | Standby Power Supply Current | $\overline{CS} \geqslant V_{IH}$ | – | 5 | 20 | – | 5 | 20 | mA |
| $I_{SB1}$ | Full Standby Power Supply Current | $\overline{CS} \geqslant V_{CC}$ = −0.2V<br>$V_{IN} \geqslant V_{CC}$ = −0.2V or $\leqslant$ 0.2V | – | 0.02 | 2 | – | 0.002 | 0.05 | mA |
| $V_{IL}$ | Input Low Voltage | | −0.5 | – | 0.8 | −0.5 | – | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.2 | – | 6.0 | 2.2 | – | 6.0 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA | – | – | 0.4 | – | – | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −4mA | 2.4 | – | – | 2.4 | – | – | V |

## Capacitance

($T_A$ = 25°C, f = 1.0MHz)

| Symbol | Item | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 6 | pF |

Note: This parameter is sampled and not 100% tested.

## Truth Table

| Mode | $\overline{CS}$ | $\overline{WE}$ | Output | Power |
|---|---|---|---|---|
| Standby | H | X | High Z | Standby |
| Read | L | H | $D_{OUT}$ | Active |
| Write | L | L | High Z | Active |

## A.C. Characteristics

($T_A$ = 0° C to +70° C, $V_{CC}$ = 5V ± 10%)

READ CYCLE

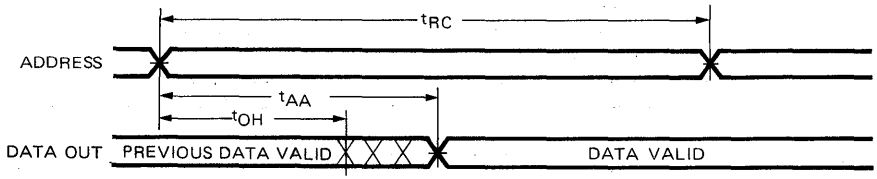
| Symbol | Parameter | UM6168 | | UM6168-1 | | UM6168-2 | | UM6168-3 | | UM6168-4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 70 | – | 55 | – | 45 | – | 40 | – | 35 | – | ns |
| $t_{AA}$ | Address Access Time | – | 70 | – | 55 | – | 45 | – | 40 | – | 35 | ns |
| $t_{ACE}$ | Chip Enable Access Time | – | 70 | – | 55 | – | 45 | – | 40 | – | 35 | ns |
| $t_{OH}$ | Output Hold from Address Change | 5 | – | 5 | – | 5 | – | 5 | – | 5 | – | ns |
| $t_{LZ}$ | Chip Selection to Output in Low Z | 5 | – | 5 | – | 5 | – | 5 | – | 5 | – | ns |
| $t_{HZ}$ | Chip Deselection to Output in High Z | 0 | 30 | – | 25 | – | 20 | – | 20 | – | 15 | ns |
| $t_{PU}$ | Chip Selection to Power Up Time | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – | ns |
| $t_{PD}$ | Chip Deselection to Power Down Time | – | 40 | – | 35 | – | 35 | – | 35 | – | 25 | ns |
| $t_{RCS}$ | Read Command Set-up Time | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – | ns |
| $t_{RCH}$ | Read Command Hold Time. | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – | ns |

WRITE CYCLE

| Symbol | Parameter | UM6168 | | UM6168-1 | | UM6168-2 | | UM6168-3 | | UM6168-4 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WC}$ | Write Cycle Time | 60 | – | 50 | – | 40 | – | 40 | – | 35 | – | ns |
| $t_{CW}$ | Chip Enabled to End of Write | 60 | – | 50 | – | 40 | – | 40 | – | 35 | – | ns |
| $t_{AW}$ | Address Valid to End of Write | 60 | – | 50 | – | 40 | – | 40 | – | 35 | – | ns |
| $t_{AS}$ | Address Set-up Time | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – | ns |
| $t_{WP}$ | Write Pulse Width | 40 | – | 35 | – | 30 | – | 30 | – | 25 | – | ns |
| $t_{WR}$ | Write Recovery Time | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – | ns |
| $t_{DW}$ | Date Valid to End of Write | 25 | – | 25 | – | 20 | – | 20 | – | 17 | – | ns |
| $t_{DH}$ | Data Hold Time | 3 | – | 3 | – | 3 | – | 3 | – | 3 | – | ns |
| $t_{WZ}$ | Write Enabled to Output in High Z | – | 25 | – | 25 | – | 20 | – | 20 | – | 13 | ns |
| $t_{OW}$ | Output Active from End of Write | – | 40 | – | 35 | – | 35 | – | 35 | – | 30 | ns |

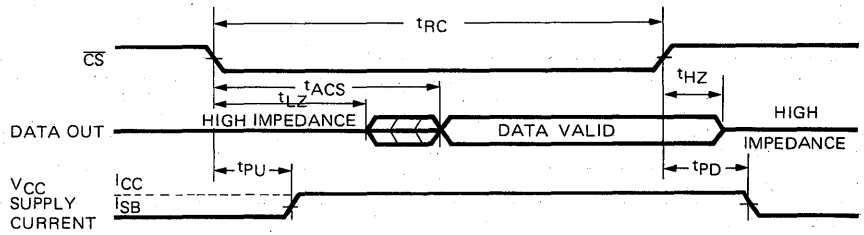
## Timing Diagrams

READ CYCLE NO. 1 (NOTES 1 AND 2)

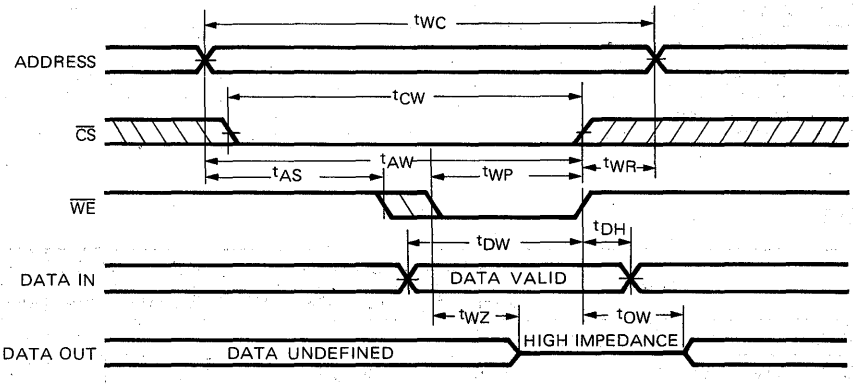



SRAM

## READ CYCLE NO. 2 (NOTES 1 AND 3)

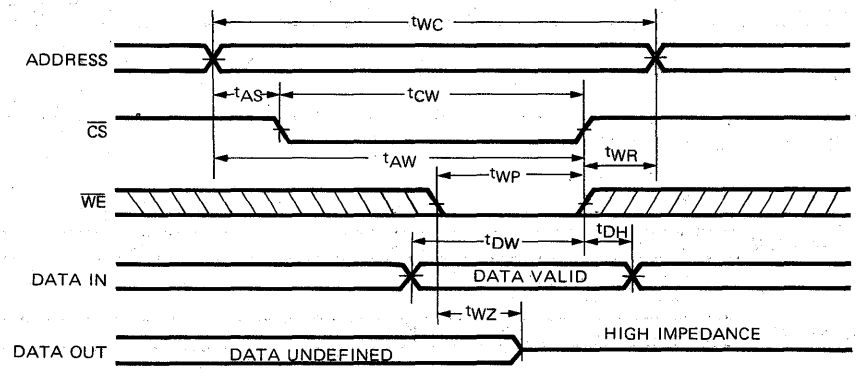



## WRITE CYCLE NO. 1 (WE CONTROLLED) (NOTE 4)




Notes:
1. CS or WE must be high during address transitions.
2. If CS goes high simultaneously with WE high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transition address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

## WRITE CYCLE NO. 2 (CS CONTROLLED) (NOTE 4)



## A.C. Test Conditions

| Test | Typ. |
|---|---|
| Input Pulse Levels | GND to 30V |
| Input Rise and Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |

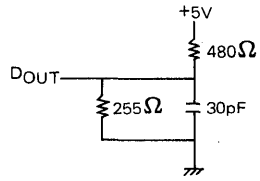



Figure 1. Output Load

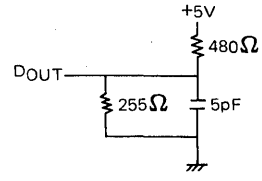



Figure 2. Output Load (for $t_{MZ}$, $t_{LZ}$, $t_{WZ}$, and $t_{OW}$)

* Including scope and jig.

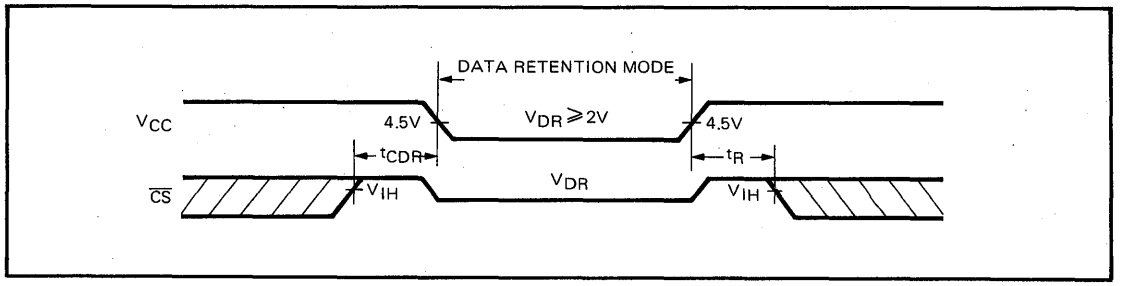


## Low $V_{CC}$ Data Retention Characteristics For L Version Only ($T_A$ = 0 to 70°C)

| Symbol | Parameter | Test Conditions | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OR}$ | $V_{CC}$ for Data Retention | | 2.0 | – | – | V |
| $I_{CCDA}$ | Data Retention Current | $\overline{CS} \geq V_{CC} - 0.2V$ | –<br>– | 0.5[2]<br>1.0[3] | 20[2]<br>30[3] | μA |
| $t_{CDA}$ | Chip Deselect to Data Retention Time | $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$ | 0 | – | – | ns |
| $t_R$ | Operation Recovery Time | | $t_{RC}$[4] | – | – | ns |

Notes: 1. $T_A = 25°C$, 2. at $V_{CC} = 2V$, 3. $V_{CC} = 3V$, 4. $t_{RC}$ = Read Cycle Time

## Timing Waveform Low $V_{CC}$ Data Retention Waveform




## Ordering Information

| Part Number | Access Time (Max.) | Operating Current (Max.) | Standby Current (Max.) | Package Type |
|---|---|---|---|---|
| UM6168 | 70 ns | 90 mA | 2 mA | Plastic |
| UM6168-1 | 55 ns | 90 mA | 2 mA | Plastic |
| UM6168-2 | 45 ns | 90 mA | 2 mA | Plastic |
| UM6168-3 | 40 ns | 90 mA | 2 mA | Plastic |
| UM6168-4 | 35 ns | 90 mA | 2 mA | Plastic |
| UM6168L | 70 ns | 90 mA | 50 μA | Plastic |
| UM6168L-1 | 55 ns | 90 mA | 50 μA | Plastic |
| UM6168L-2 | 45 ns | 90 mA | 50 μA | Plastic |
| UM6168L-3 | 40 ns | 90 mA | 50 μA | Plastic |
| UM6168L-4 | 35 ns | 90 mA | 50 μA | Plastic |