

6 Line ESD/EMI Protection for Color LCD Interfaces

UM6401 DFN12 3.0×1.6

General Description

The UM6401 is a low pass filter array with integrated TVS diodes. It is designed to suppress unwanted EMI/RFI signals and provide electrostatic discharge (ESD) protection in portable electronic equipment. This state-of-the-art device utilizes solid-state silicon-avalanche technology for superior clamping performance and DC electrical characteristics. They have been optimized for protection of color LCD panels in cellular phones and other portable electronics. The device consists of six identical circuits comprised of TVS diodes for ESD protection, and a resistor-capacitor network for EMI/RFI filtering. A series resistor value of 100Ω and a capacitance value of 10pF are used to achieve 30dB minimum attenuation from 800MHz to 2.5GHz. The TVS diodes provide effective suppression of ESD voltages in excess of ±15kV (air discharge) and ±8kV (contact discharge) per IEC 61000-4-2, level 4. The UM6401 is in a 12-pin, RoHS compliant, DFN12 3.0×1.6 package. The leads are spaced at a pitch of 0.5mm and are finished with lead-free Ni Pd. The small package makes it ideal for use in portable electronics such as cell phones, digital still cameras, and PDAs.

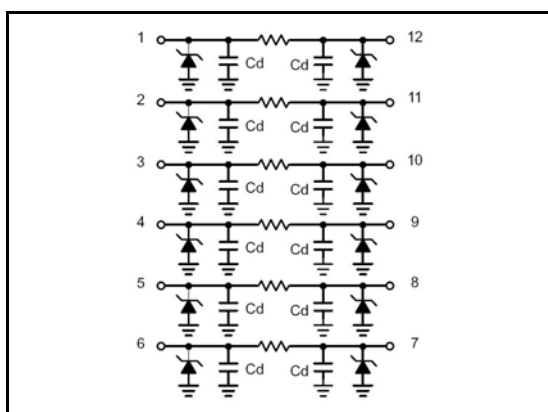
Applications

- Color LCD Protection
- Cell Phone CCD Camera Lines
- Bottom Connector Cell Phones

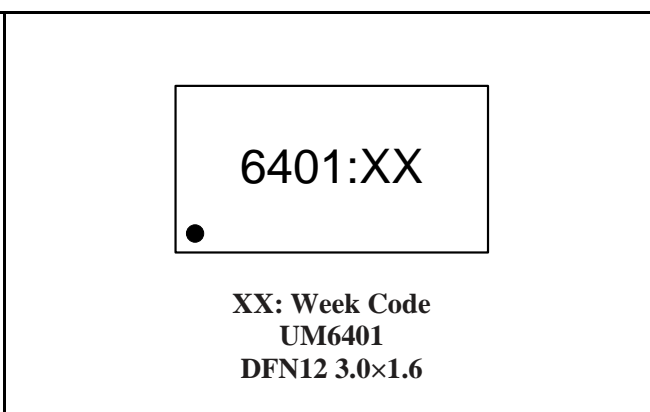
Features

- Bidirectional EMI/RFI Filter with Integrated TVS
- ESD Protection to IEC 61000-4-2 (ESD) Level 4, ±15kV (Air), ±8kV (Contact)
- 30dB Minimum Attenuation: 800MHz to 2.5GHz
- TVS Working Voltage: 5V
- Resistor: 100Ω±15%
- Typical Capacitance: 10pF (V_R=2.5V) Protection and Filtering for Six Lines
- Solid-State Technology

Pin Configurations



Top View



Ordering Information

| Part Number | Working Voltage | Packaging Type | Channel | Marking Code | Shipping Qty |
|-------------|-----------------|----------------|---------|--------------|----------------------------|
| UM6401 | 5.0V | DFN12 3.0×1.6 | 6 | 6401 | 3000pcs/7 Inch Tape & Reel |

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-----------|------------|------|
| Junction Temperature | T_J | 125 | °C |
| Steady-State Power per Resistor @ 25°C | P_R | 328 | mW |
| Operating Temperature Range | T_{OP} | -40 to 85 | °C |
| Storage Temperature Range | T_{STG} | -55 to 150 | °C |
| Maximum Lead Temperature for Soldering | T_L | 260 | °C |

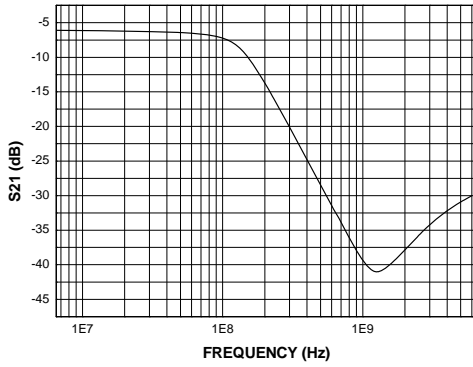
Electrical Characteristics

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|-----------|--|-----|-----|-----|------|
| Reverse Stand-Off Voltage | V_{RWM} | | | | 5 | V |
| Reverse Breakdown Voltage | V_{BR} | $I_T=1mA$ | 6 | 7 | 8 | V |
| Reverse Leakage Current | I_R | $V_{RWM}=3.0V$ | | | 0.5 | μA |
| Total Series Resistance | R_A | $I_R=20mA$, Each Line | 85 | 100 | 115 | Ω |
| Total Capacitance | C_d | Input to GND, Each Line, $V_R=0V$, $f=1MHz$ | 16 | 20 | 24 | pF |
| Total Capacitance | C_d | Input to GND, Each Line, $V_R=2.5V$, $f=1MHz$ | 9 | 10 | 12 | pF |
| Cut-Off Frequency (Note 1) | f_{3dB} | Above this frequency, appreciable attenuation occurs | | 150 | | MHz |

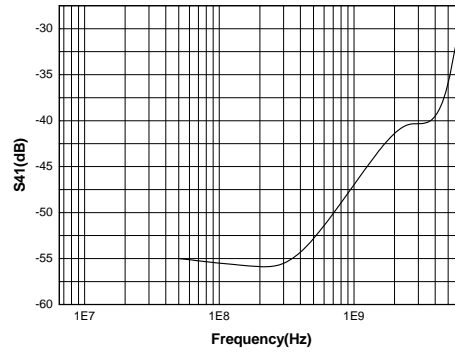
Note 1: 50Ω source and 50Ω load termination.

Typical Operating Characteristics

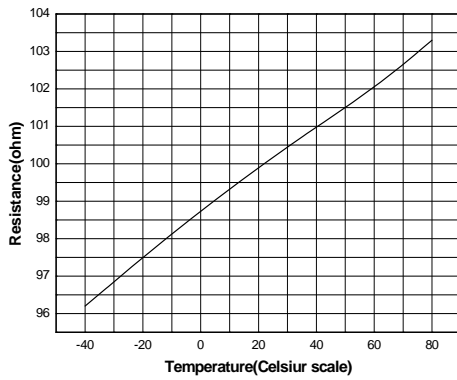
Typical Insertion Loss S21



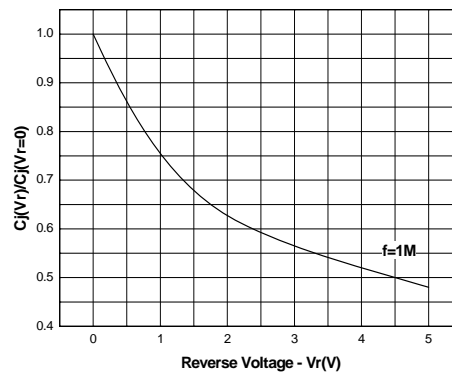
Analog Crosstalk Curve (S41)



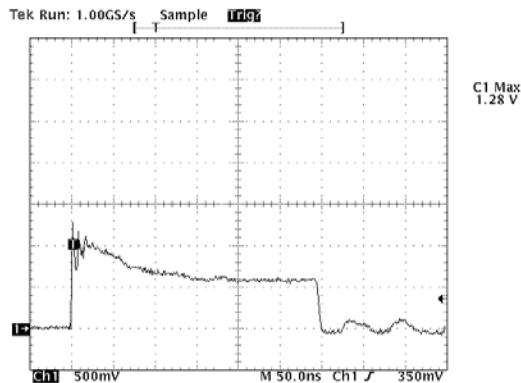
Typical Resistance vs. Temperature



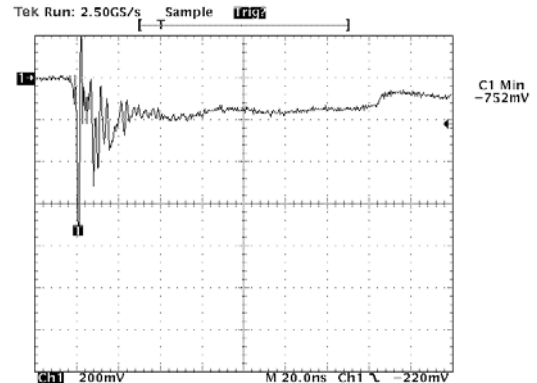
Capacitance vs. Reverse Voltage



ESD Clamping (+8kV Contact)



ESD Clamping (-8kV Contact)



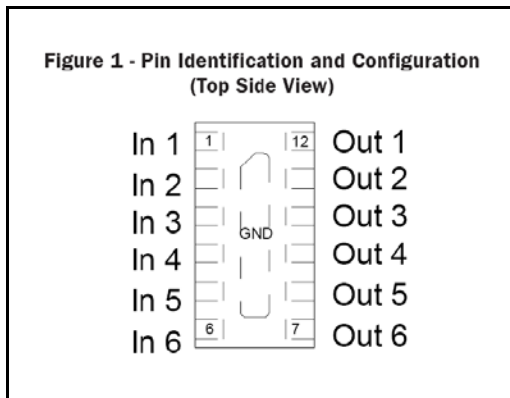
Applications Information

Device Connection

The UM6401 is comprised of six identical circuits each consisting of a low pass filter for EMI/RFI suppression and dual TVS diodes for ESD protection. The device is in a 12-pin DFN package. Electrical connection is made to the 12 pins located at the bottom of the device. A center tab serves as the ground connection. The device has a flow through design for easy layout. Pin connections are noted in Figure 1. All path lengths should be kept as short as possible to minimize the effects of parasitic inductance in the board traces. Recommendations for the ground connection are given below.

Ground Connection Recommendation

Parasitic inductance present in the board layout will affect the filtering performance of the device. As frequency increases, the effect of the inductance becomes more dominant. This effect is given by Equation 1.



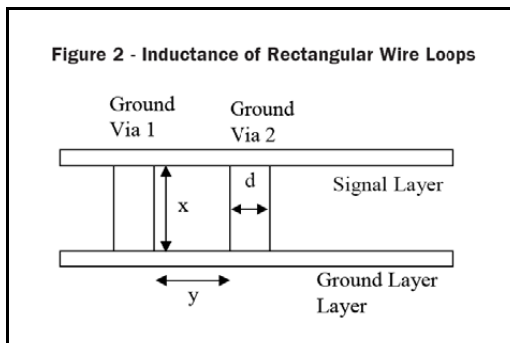
| Pin | Identification |
|------------|----------------|
| 1 - 6 | Input Lines |
| 7 - 12 | Output Lines |
| Center Tab | Ground |

Equation 1: The Impedance of an Inductor at Frequency XLF

$$X_{LF}(L, f) = 2 \times \pi \times f \times L$$

Where:
 L = Inductance (H)
 f = Frequency (Hz)

Via connections to the ground plane form rectangular wire loops or ground loop inductance as shown in Figure 2. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane. Bringing the ground plane closer to the signal layer (preferably the next layer) also reduces ground loop inductance. Multiple vias in the device ground pad will result in a lower inductive ground loop over two exterior vias. Vias with a diameter d are separated by a distance y run between layers separated by a distance x . The inductance of the loop path is given by Equation 2. Thus, decreasing distance x and y will reduce the loop inductance and result in better high frequency filter characteristics.

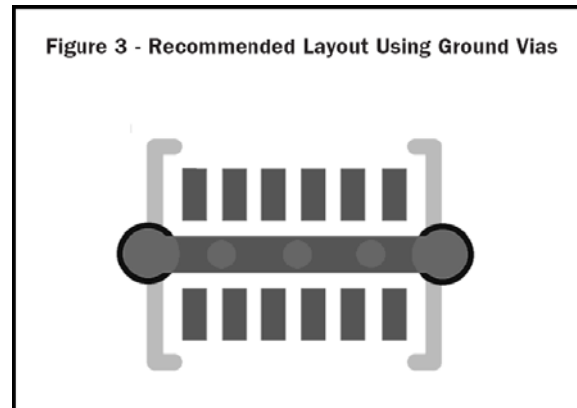


Equation 2: Inductance of Rectangular Wire Loop

$$L_{RECT}(d, x, y) = 10.16 * 10^{-9} * \left[x * \ln \left[\frac{2 * y}{d} \right] + y * \ln \left[\frac{2 * x}{d} \right] \right]$$

Where:
 d = Diameter of the wire (in)
 x = Length of wire loop (in)
 y = Breadth of wire loop (in)

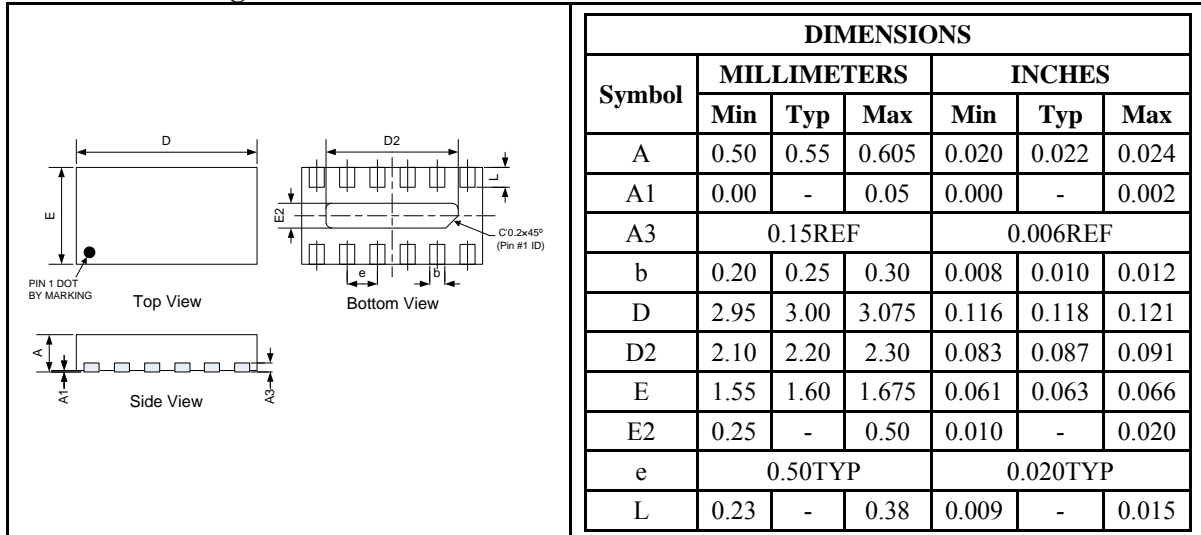
Figure 3 shows the recommended device layout. The ground pad vias have a diameter of 0.008 inches (0.20 mm) while the two external vias have a diameter of 0.010 inches (0.250mm). The internal vias are spaced approximately evenly from the center of the pad. The designer may choose to use more vias with a smaller diameter (such as 0.005 inches or 0.125mm) since changing the diameter of the via will result in little change in inductance (i.e. the log function in Equation 2 is highly insensitive to parameter d).



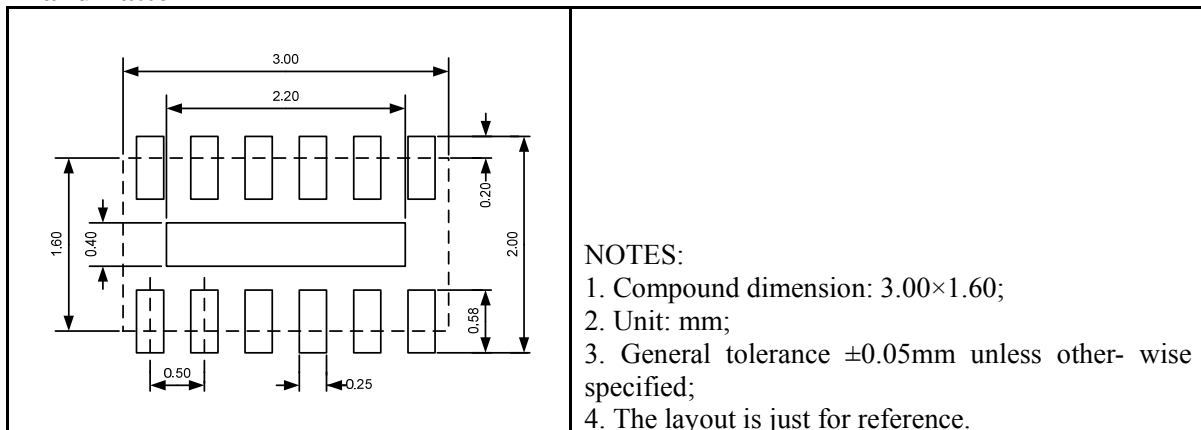
Package Information

UM6401: DFN12 3.0×1.6

Outline Drawing



Land Pattern



Tape and Reel Orientation



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