UM6521 / UM6521A

Peripheral Interface Adapter(PIA)

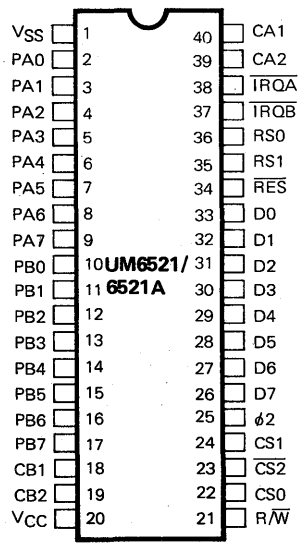
Features

- Extended performance version of UM6520
- Single +5V power supply
- Two 8-bit bi-directional I/O ports with individual data direction control
- CMOS-compatible peripheral port A lines
- Automatic "handshake" control of data transfers
- Programmable interrupt capability
- Automatic initialization on power up
- 1 and 2 MHz versions
- Direct replacement for Motorola MC6821

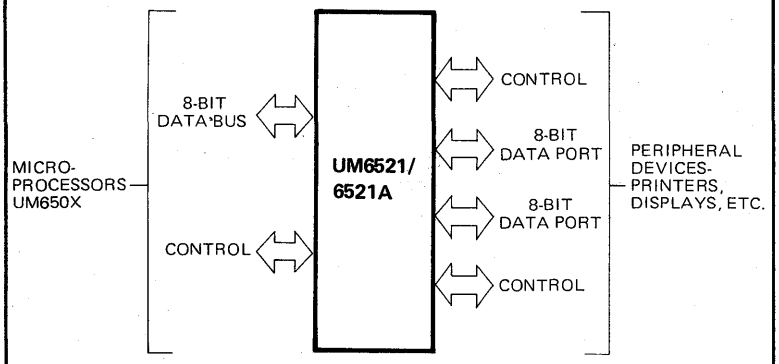
General Description

The UM6521/A Peripheral Interface Adapter (PIA) is designed to provide a broad range of peripheral control to microcomputer systems. It is functionally compatible with the UM6520, but with more drive capability and improved performance. Control of peripheral devices is accomplished through two 8-bit bi-directional I/O ports. Each I/O line may be programmed to be either an input or an output. In addition, four peripheral control lines are provided to perform "handshaking" during data transfers.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage V_{CC} . . . . . −0.3V to +7.0V
Input Voltage V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature Range T_A . . . . . 0°C to +70°C
Storage Temperature Range T_{STG} . . . . −55°C to +150°C
Notice:
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Units
V_{IH}	Input High Voltage	+2.0	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	+0.8	V
I_{IN}	Input Leakage Current V_{IN} = 0 to 5.0V R/W, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	–	±2.5	μA
I_{TSI}	Three-State (Off State Input Current) (V_{IN} = 0.4 to 2.4 V, V_{CC} = max), D_0-D_7, PB_0-PB_7, CB_2	–	±10	μA
I_{IH}	Input High Current (V_{IH} = 2.4 V), PA_0-PA_7, CA_2	−200	–	μA
I_{IL}	Input Low Current (V_{IL} = 0.4 V), PA_0-PA_7, CA_2	–	2.4	mA
V_{OL}	Output Low Voltage (I_L = 3.2 mA), $\overline{IRQA}$, $\overline{IRQB}$	–	0.4	V
V_{OH}	Output High Voltage (I_L = 205 μA), D_0-D_7	2.4	–	V
V_{OL}	Output Low Voltage (I_L = 3.2mA), PA_0-PA_7, PB_0-PB_7, CA_2, CB_2	–	0.4	V
V_{OH}	Output High Voltage (I_H = −200 μA), PA_0-PA_7, PB_0-PB_7, CA_2, CB_2	2.4	–	V
I_{OH}	Output High Current (Direct Transistor Drive Outputs) (V_{OUT} = 1.5 V), PB_0-PB_7, CB_2	−1.0	−10.0	mA
I_{OFF}	Output Leakage Current (Off-State), $\overline{IRQA}$, $\overline{IRQB}$	–	10	μA
P_D	Power Dissipation (V_{CC} = 5.25 V)	–	500	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz) D_0-D_7, PA_0-PA_7, PB_0-PB_7, CA_2, CB_2 R/$\overline{W}$, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$ CA_1, CB_1, ϕ_2	 – – –	 10 7.0 20	 pF pF pF
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz)	–	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

Peripheral IC

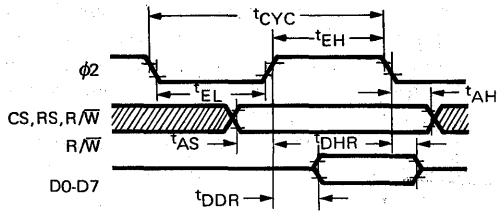


Figure 1. Read Timing Characteristic

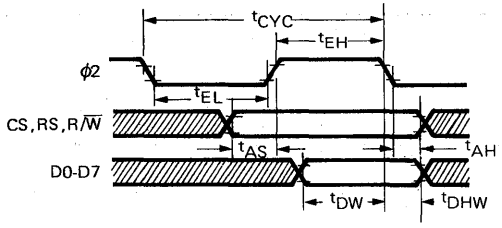


Figure 2. Write Timing Characteristics

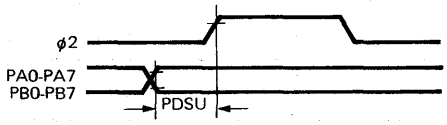


Figure 3. Peripheral Data Setup Time

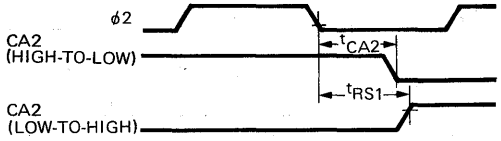


Figure 4. CA_2 Timing

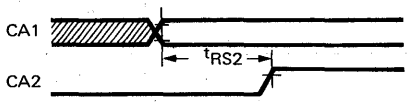


Figure 5. CA_1 /CA_2 Timing

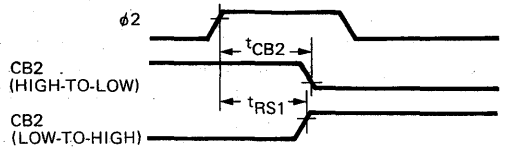


Figure 6. CB_2 Timing

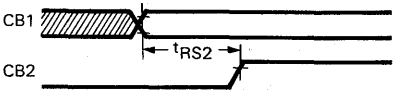


Figure 7. CB_1 /CB_2 Handshake Timing

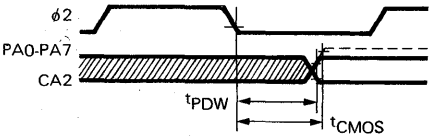


Figure 8. PA Port Delay Time

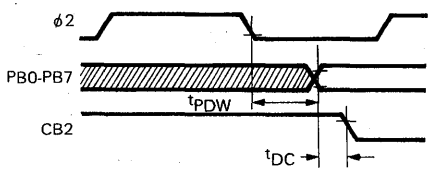


Figure 9. PB Port Delay Time

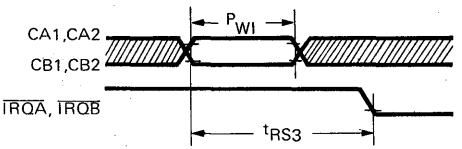


Figure 10. Interrupt Timing

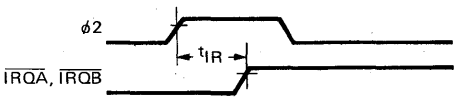


Figure 11. Interrupt Clear Timing

Processor Interface Timing

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise noted)

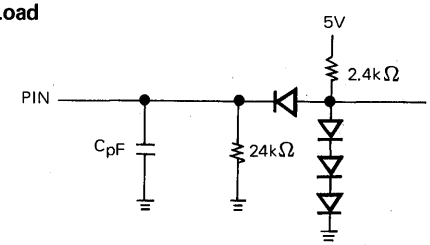
Symbol	Parameter	UM6521		UM6521A		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Cycle Time	1000	–	500	–	ns
t_{EH}	ϕ_2 Pulse Width	440		200	–	ns
t_{EL}	ϕ_2 Pulse Delay	430	–	210	–	ns
t_{AS}	CS, RS, R/$\overline{W}$ Setup Time	160	–	70	–	ns
t_{AH}	CS, RS, R/$\overline{W}$ Hold Time	10	–	10	–	ns
t_{DDR}	Data Delay Time, Read Cycle	–	320	–	180	ns
t_{DHR}	Data Hold Time, Read Cycle	10	–	10	–	ns
t_{DSW}	Data Setup Time, Write Cycle	195	–	60	–	ns
t_{DHW}	Data Hold Time, Write Cycle	10	–	10	–	ns

Processor Interface Timing

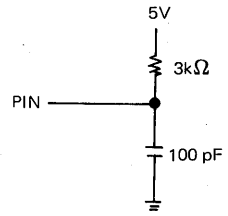
(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise noted)

Symbol	Parameter	UM6521		UM6521A		Units
		Min.	Max.	Min.	Max.	
t_{PDSU}	Peripheral Data Setup Time	200	–	100	–	ns
t_{CA2}	CA_2 Delay Time, High-to-Low	–	1.0	–	0.5	μs
t_{RS1}	CA_2 Delay Time, Low-to-High	–	1.0	–	0.5	μs
t_{RS2}	CA_2 Delay Time, Handshake Mode	–	2.0	–	1.0	μs
t_{CB2}	CB_2 Delay Time, High-to-Low	–	1.0	–	0.5	μs
t_{RS1}	CB_2 Delay Time, Low-to-High	–	1.0	–	0.5	μs
t_{RS2}	CB_2 Delay Time, Handshake Mode	–	2.0	–	1.0	μs
t_{PDW}	Peripheral Port Delay Time	–	1.0	–	0.5	μs
t_{CMOS}	Peripheral Port Delay Time (CMOS)	–	2.0	–	1.0	μs
t_{DC}	CB_2 Delay Time from Data Valid	20	–	20	–	ns
P_{WI}	Interrupt Input Pulse Width	500	–	500	–	ns
t_{RS3}	Interrupt Response Time	–	1.0	–	1.0	μs
t_{IR}	Interrupt Clear Delay	–	1.6	–	0.85	μs
t_R, t_F	Rise and Fall Times – CA_1, CA_2, CB_1, CB_2	–	1.0	–	1.0	μs

Test Load



C = 130 pF MAX. FOR DB0-DB7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS



OPEN COLLECTOR
OUTPUT TEST LOAD

Peripheral IC

Interface Signal Description

$\overline{RES}$ (Reset)

This signal is used to initialize the PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

ϕ_2 (Input Clock)

This input is the system ϕ_2 clock and is used to trigger all data transfers between the microprocessor and the PIA.

R/$\overline{W}$ (Read/Write)

This signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ signal permits the processor to read data supplied by the PIA; a low on the R/$\overline{W}$ signal permits the processor to Write into the PIA.

$\overline{IRQA}$, $\overline{IRQB}$ (Interrupt Requests)

$\overline{IRQA}$ and $\overline{IRQB}$ are interrupt lines generated by the PIA for ports A and B respectively. These signals are active low signals and have open-drain outputs, thus allowing multiple IRQ signals from multiple PIA's to be wire-ORed together before connecting to the processor IRO signal input.

D_0-D_7 (Data Bus)

These eight data bus lines are used to transfer data information between the processor and the PIA. These signals are bi-directional and are normally highimapedance except when selected for a read operation.

CS0, CS1, $\overline{CS2}$ (Chip Selects)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits.

RS0, RS1 (Register Selects)

These two signals are used to select the various registers inside the PIA.

Internal Architecture

The UM6520 is organized into two independent sections referred to as the "A Side" and the "B Side." Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control and the buffers necessary to drive the Peripheral Interface buses. Figure 12 is a block diagram of the UM6521.

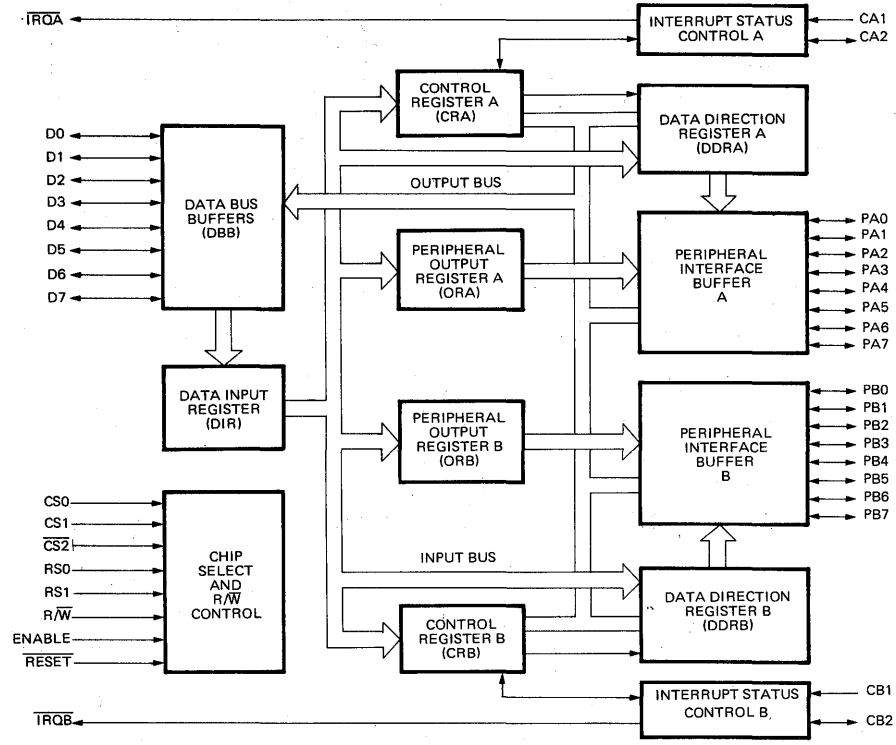


Figure 12. UM6521 Block Diagram

	7	6	5 4 3	2	1 0
CRA	IRQA1	IRQA2	CA2 Control	DDRA Access	CA1 Control
	7	6	5 4 3	2	1 0
CRB	IRQB1	IRQB2	CB2 Control	DDRB Access	CB1 Control

Figure 13. Control Registers

Data Input Register

When the microprocessor writes data into the Um6521, the data which appears on the data bus during the Phase Two clock pulse is latched into the Data Input Register. It is then transferred into one of six internal registers of the UM6521 after the trailing edge of Phase Two. This assures that the data on the peripheral output lines will make smooth transitions from high to low or from low to high and the voltage will remain stable except when it is going to the opposite polarity.

Control Registers (CRA and CRB)

Figure 4 illustrates the bit designation and functions in the Control Registers. The Control Registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) are provided in each control register to indicate the status of the interrupt input lines (CA1, CA2, CB1, CB2). These interrupt status bits (IRQA1, (IRQB1) are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These are the interrupt lines which drive the interrupt input ($\overline{IRQ}$, $\overline{NMI}$) of the microprocessor.

Data Direction Registers (DDRA, DDRB)

The Data Direction Registers allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Placing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Peripheral Output Registers (ORA, ORB)

The Peripheral Output Registers store the output data which appears on the Peripheral I/O port. Writing a "0" into a bit in ORA causes the corresponding line on the Peripheral A port to go low ($\leq$ 0.4V) if that line is programmed to act as an output. A "1" causes the corresponding output to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

Interrupt Status Control

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register, detects active transitions on the interrupt inputs and performs those operations necessary to assure proper operation of these four peripheral interface lines.

Peripheral Interface Buffers (A, B) and Data Bus Buffers (DBB)

These Buffers provide the necessary current and voltage drive on the peripheral I/O ports and data bus to assure proper system operation and to meet the device specifications.

Functional Description

Bit 2 (DDR) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1", a Peripheral Output register (ORA, ORB) is selepted, and if bit 2 is a "0", a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, SR1) selects the various internal registers as shown in Figure 14.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

Register Select Lines (RS0), (RS1)

These two register select lines are used to select the various registers inside the UM6521. These input lines are used in conjunction with internal control registers to select a particular register that is to be accessed by the microprocessor. These lines are normally connected to microprocessor address output lines. These lines operate in conjunction with the chip-select inputs to allow the microprocessor to address a single 8-bit register within the microprocessor address space. This register may be an internal register (CRA, ORA, etc.) or it may be a Peripheral I/O port.

The processor may write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are discussed separately below.

Reading the Peripheral A I/O Port

The Peripheral A I/O port consists of 8 lines which can be programmed to act as inputs or outputs. When programmed to act as outputs, each line reflects the contents of the corresponding bit in the Peripheral Output Register. When programmed to act as inputs, these lines will go high or low depending on the input data. The Peripheral Output Register (ORA) has no effect on those lines programmed to act as inputs. The eight lines of the Peripheral A I/O port therefore contain either input or output data depending on whether the line is programmed to act as an input or an output. Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines into the processor (via the data bus). This will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read into the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

Reading the Peripheral B I/O Port

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back into the processor on a Read operation.

Interrupt Request Lines ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are "open drain" and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a "wired-OR" configuration. The "A" and "B" in the titles of these lines correspond to the "A" peripheral port and the "B" peripheral port. Hence each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits

Register Select Pin		Data Direction Register Access Control Bit		Register Selected
RS1	RS0	CRA-2	CRB-2	
0	0	1	–	Peripheral Interface A
0	0	0	–	Data Direction Register A
0	1	–	–	Control Register A
1	0	–	1	Peripheral Interface B
1	0	–	0	Data Direction Register B
1	1	–	–	Control Register B

Figure 14. Register Addressing

which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers. These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2).

The four interrupt flags are set by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

Control of $\overline{IRQA}$

Control Register A bit 7 is always set by an active transition of the CA1 interrupt input signal. Interrupting from this flag can be disabled by setting bit 0 in the Control Register A (CRA) to a logic 0. Likewise, Control Register A bit 6 can be set by an active transition of the CA2 interrupt input signal. Interrupting from this flag can be disabled by setting bit 3 in the Control Register to a logic 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the proper chip-select and register-select signals are provided to allow the processor to read the Peripheral A I/O port.

Control of $\overline{IRQB}$

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB is set by an active transition on CB1; interrupting from this flag is controlled by CRB bit 0. Likewise, bit 6 in CRB is set by an active transition on CB2; interrupting from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 are reset by a "Read Peripheral B Output Register" operation.

SUMMARY:	
$\overline{IRQA}$ goes low	when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low	when CRB-7 = 1 and CRB-0 = 1 or when CRB-6 = 1 and CRB-3 = 1

It should be stressed at this point that the flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

Interface Between UM6521 and Peripheral Devices

The UM6521 provides two 8-bit bi-directional ports and 4 interrupt/control lines for interfacing to peripheral devices. These ports and the associated interrupt/control lines are referred to as the "A" side and the "B" side. Each side has its own unique characteristics and will therefore be discussed separately below.

Peripheral I/O Ports

The Peripheral A and Peripheral B I/O Ports allow the microprocessor to interface to the input lines on the peripheral device by loading data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Peripheral A I/O Port (PA0-PA7)

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a "1" in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A "0" in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-ups as shown in Figure 15. These pull-up devices are resistive in nature and therefore allow the output voltage to go to V_{CC} for a logic 1. The switches can sink a full 1.6mA, making these buffers capable of driving one standard TTL load.

In the input mode, the pull-up devices shown in Figure 15 are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral B I/O Port (PB0-PB7)

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an output has been discussed previously. Likewise, the effect of reading or writing this port has been discussed. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices as shown in Figure 16. The pull-up devices are switched "OFF" in the "0" state and "ON" for a logic 1. Since

these pull-ups are active devices, the logic "1" voltage is not guaranteed to go higher than +2.4V. They are TTL compatible but are not CMOS compatible.

However, the active pull-up devices can source up to 1mA at 1.5V. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows very simple control of relays, lamps, etc.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic which is a function of the Peripheral B push-pull buffers is the high-impedance input state. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

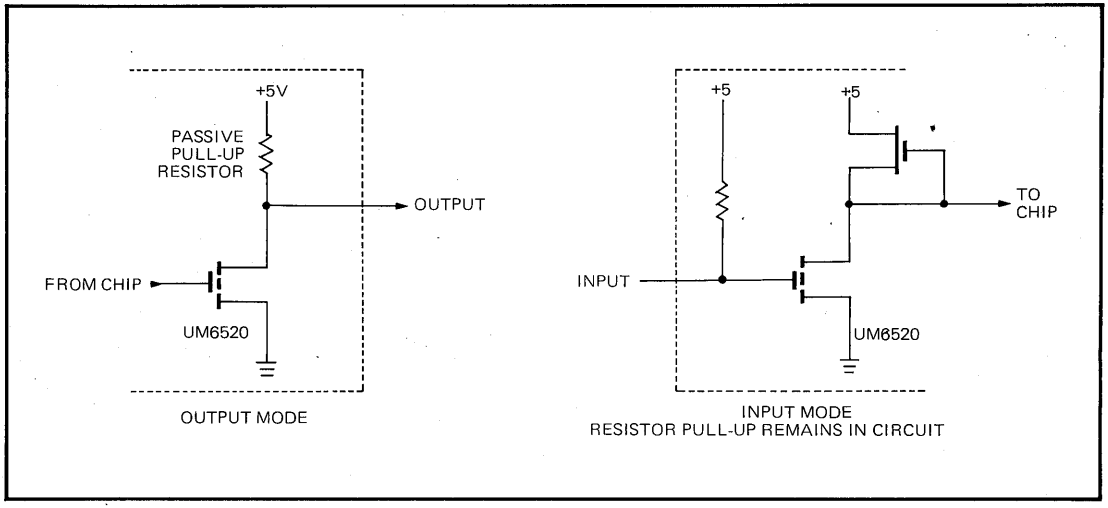


Figure 15. Port A Buffer Circuit (PA_0-PA_7)

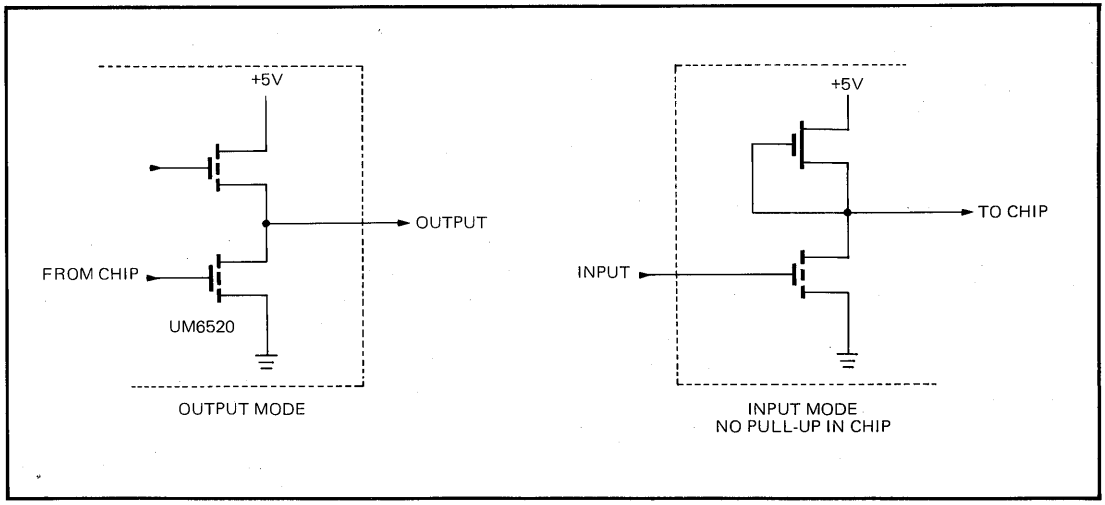


Figure 16. Port B Buffer Circuit (PB_0-PB_7)

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 17 summarizes the operation of these control lines.

Peripheral A Interrupt Input/Peripheral Control Lines (CA1, CA2)

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

NOTE: A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

Setting the interrupt flag will interrupt the processor through $\overline{IRQA}$ if bit 0 of CRA is a 1 as described previously.

CA2 can act as a totally independent interrupt input or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupts.

In the Output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a "0" and CRA, bit 3 to a "1". This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output model allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and set CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

Peripheral B Interrupt Input/Peripheral Control Lines (CB1, CB2)

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

CA1/CB1 CONTROL

CRA (CRB)		Active Transition	IRQA (IRQB) Interrupt Outputs
Bit 1	Bit 0	of Input Signal*	
0	0	Negative	Disable – remain high
0	1	Negative	Enable – goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable – remain high
1	1	Positive	Enable – as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB)			Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
Bit 5	Bit 4	Bit 3		
0	0	0	Negative	Disable – remains high
0	0	1	Negative	Enable – goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable – remains high
0	1	1	Positive	Enable – as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA			Mode	Descriptions
Bit 5	Bit 4	Bit 3		
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB			Mode	Descriptions
Bit 5	Bit 4	Bit 3		
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Figure 17. Summary of Operation of Control Lines

Ordering Information

Part Number	Speed	Package
UM6521	1 MHz	Plastic
UM6521A	2 MHz	Plastic