UM6532/UM6532A

RAM, I/O, Timer Array

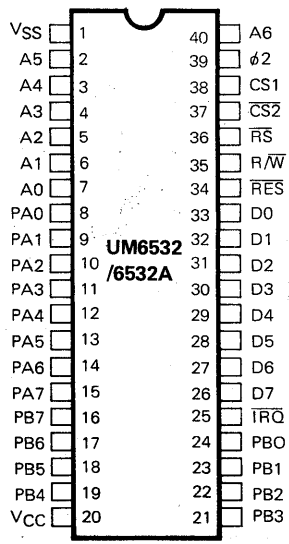
Features

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- Programmable edge-sensitive interrupt
- 128 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O peripheral data direction registers
- Programmable interval timer
- Programmable interval timer interrupt
- Peripheral pins with direct transistor drive capability
- High impedance three-state data pins

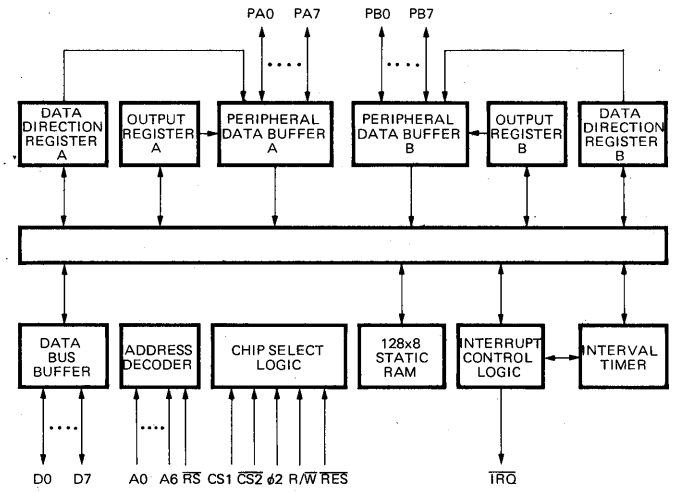
General Description

The UM6532 is designed to operate in conjunction with the UM6500 Microprocessor Family. It is comprised of a 128x8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect interrupt circuit.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Supply Voltage . . . . . +8.0 Volts
Operating Voltage Range . . . . . +4V to +7V
Input Voltage Applied . . . . . GND–2.0V to 6.5V
I/O Pin Voltage Applied . . . . . GND–0.5V to V_{CC}+0.5V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Maximum Power Dissipation . . . . . 1 Watt

*Comments

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may effect device relability.

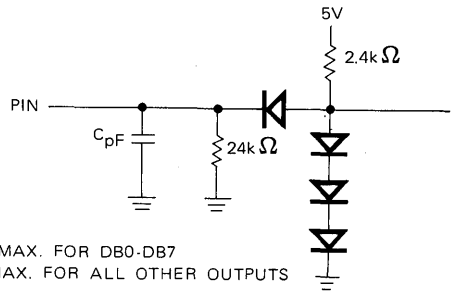
D.C. Characteristics

(V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0 – 70°C)

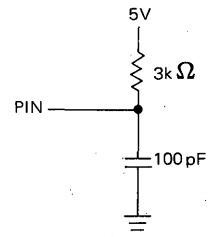
Characteristic	Symbol	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	0.3		0.4	V
Input Leakage Current; V_{IN} = V_{SS}+ 5V A0-A6, $\overline{RS}$, R/W, $\overline{RES}$, ϕ2, CS1, $\overline{CS2}$	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = 0.4V to 2.4V; D0-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	–100	–300		μA
Output High Voltage V_{CC} = MIN, I_{LOAD} –100μA (PA0-PA7, PB0-PB7, D0-D7) I_{LOAD} 3MA (PB0-PB7)	V_{OH}	 2.4 1.5			V
Output Low Voltage V_{CC} = MIN, I_{LOAD} 1.6MA	V_{OL}			0.4	V
Output High Current (Sourcing); V_{OH} ⩾ 2.4V (PA0-PA7, PB0-PB7, D0-D7) ⩾ 1.5V Available for direct transistor drive (PB0-PB7)	I_{OH}	 –100 3.0	 –1000 5.0		 μA mA
Output Low Current (Sinking); V_{OL} ⩽ 0.4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{CIK}			30	pf
Input Capacitance	C_{IN}			10	pf
Output Capacitance	C_{OUT}			10	pf
Power Dissipation (V_{CC} = 5.25V)	P_D			680	mW

*All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

Test Load



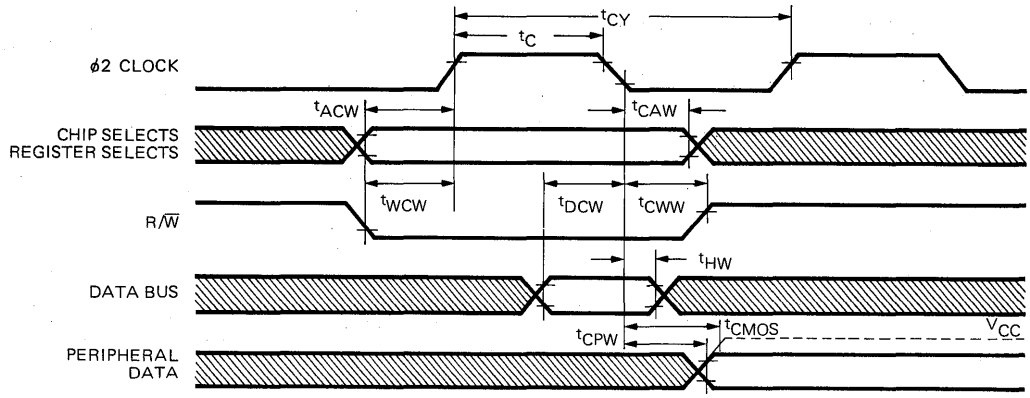
C = 130 pF MAX. FOR DB0-DB7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS



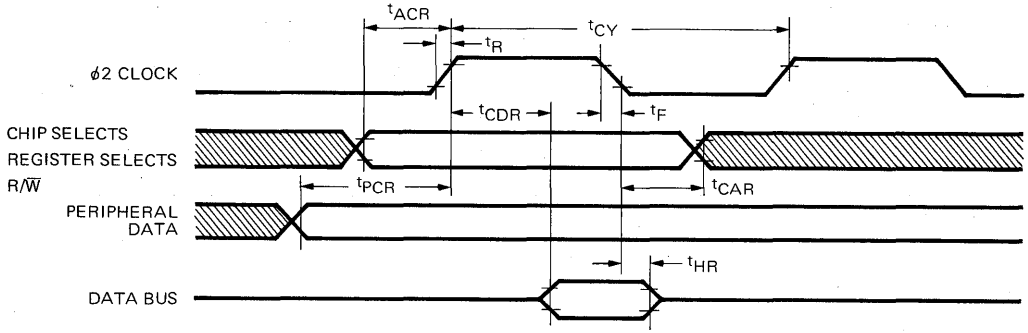
OPEN COLLECTOR
OUTPUT TEST LOAD

Peripheral IC

Write Timing Characteristics



Read Timing Characteristics



Write Timing Characteristics

Symbol	Parameter	UM6532		UM6532A		Units
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	ϕ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	265	–	100	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

Note: t_r , t_f = 10 to 30 ns.

Read Timing Characteristics

Symbol	Parameter	UM6532		UM6532A		Units
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

Note: tr, tf = 10 to 30ns.

Interface Signal Description

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL}<0.4$, $V_{IH}>2.4$) or high level clock ($V_{IL}<0.2$, $V_{IH} = V_{CC}{}^{+0.3}_{-0.2}$).

Read/Write (R/$\overline{W}$)

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the UM6532. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the UM6532. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the UM6532.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ output is derived from the interrupt control logic. It will normally be high with a low indicating an interrupt from the UM6532. $\overline{IRQ}$ is an open-drain output, permitting several units to be wire-or'ed to the common $\overline{IRQ}$ microprocessor input pin. The $\overline{IRQ}$ output may be activated by a transition on PA7 or timeout of the Interval Timer.

Data Bus (D0-D7)

The UM6532 has eight bi-directional data lines (D0-D7). These lines connect to the system's data bus and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports (PA0-PA7, PB0-PB7)

The UM6532 has two 8-bit peripheral I/O Ports, Port A (lines PA0-PA7) and Port B (lines PB0-PB7). Each line is individually programmable as either an input or an output. By writing a "0" to any bit position of the Data Direction Register (DDRA or DDRB) the corresponding line will be programmed an an input. Likewise, by writing a "1" to any bit position in DDRA or DDRB will cause the corresponding line to act as an output.

When a Port line is programmed as an input and its output register (ORA or ORB) is read by the MPU, the TTL level on the Port line will be transferred to the data bus. When the Port lines are programmed as outputs, the lines will reflect the data written by the MPU into the output registers. See Edge Sense Interrupt Section for an additional use of PA7.

Address and Select Lines (A0-A6, $\overline{RS}$, CS1 and $\overline{CS2}$)

A0-A6 and $\overline{RS}$ are used to address the RAM, I/O registers, Timer and Flag register. CS1 and $\overline{CS2}$ are used to select (enable access to) the UM6532.

Internal Organization

A block diagram of the internal architecture is shown in Figure 1. The UM6532 is divided into four basic sections: RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O register.

RAM 128 Bytes (1024 Bits)

A 128 x 8 static RAM is contained on the UM6532. It is addressed by A0-A6 (Byte Select), $\overline{RS}$, CS1, and $\overline{CS2}$.

Internal Peripheral Registers

There are four 8-bit internal registers: two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral I/O. A logic zero in a bit of the data direction register (DDRA and DDRB) causes the corresponding line of the I/O port to act as an input. A logic one causes the corresponding line to act as an output. The voltage on any line programmed as an output is determined by the corresponding bit in the output register (ORA and ORB).

Data is read directly from the PA lines during a peripheral read operation. For a PA pin programmed as an output, the data transferred into the processor will be the same as the data in the ORA only if the voltage on the line is allowed to be $\geqslant$2.4 volts for a logic one and $\leqslant$0.4 volts for a zero. If the loading on the line does not allow this, then the data resulting from the read operation may not match the contents of ORA.

The output buffers for the PB lines are somewhat different from the PA buffers. The PB buffers are push-pull devices which are capable of sourcing 3 mA at 1.5 volts. This allows these lines to directly drive transistor circuits. To assure that the processor will read the proper data when performing a peripheral read operation, logic is provided in the peripheral B port to permit the processor to read the contents of ORB, instead of the PB lines.

Interval Timer

The Timer section of the UM6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 1.

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T, or 1024T increments, where T is the system clock period. When a full count is reached, the interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock continues counting down, but at a 1T rate to a maximum of-255T. This allows the user to read the counter and then determine how long the interrupt has been set.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of $\overline{IRQ}$, i.e., A3=1 enables $\overline{IRQ}$, A3=0 disables $\overline{IRQ}$. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read from or written to by the processor. If $\overline{IRQ}$ is enabled by A3 and an interrupt occurs $\overline{IRQ}$ will go low. When the Timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the Timer has counted down to 0 0 0 0 0 0 0 0 an interrupt will occur on the next count time and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the Timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the Timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
Add 1 = 0 0 0 1 1 1 0 0 = 28.

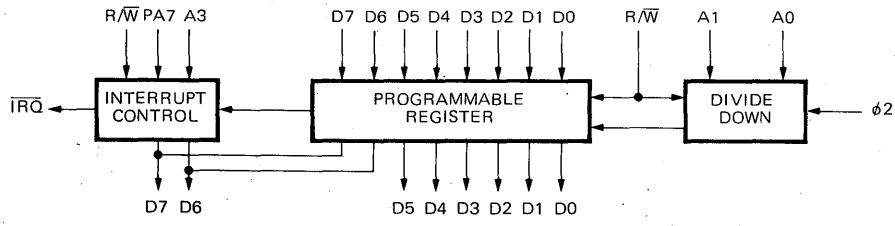


Figure 1. Basic Elements of Interval Timer

Thus, to arrive at the total elapsed time, merely do a two's complement and add to the original time written into the Timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52x8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After an interrupt, whenever the Timer is written or read the interrupt is reset. However, the reading of the Timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 2 illustrates an example of interrupt.

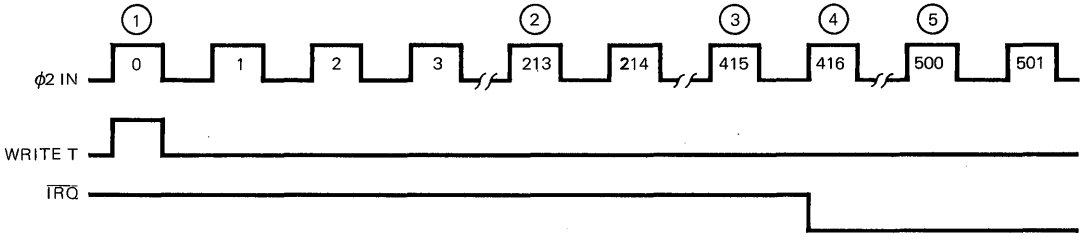


Figure 2. Timer Interrupt Timing

1. Data written into Interval Timers is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in Interval timer is 0 0 0 1 1 0 0 1 = 25_{10}

$$52 - \frac{231}{8} - 1 = 52 - 26 - 1 = 25$$

3. Data in Interval Timer is 0 0 0 0 0 0 0 0 = 0_{10}

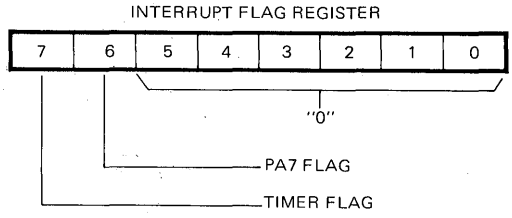
$$52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$$

4. Interrupt has occurred at $\phi 2$ pulse #416
   Data in Interval Timer = 1 1 1 1 1 1 1 1
5. Data in Interval Timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 + (52 \times 8) = 500_{10}$

When reading the Timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write operation.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits: the timer interrupt flag and the PA7 interrupt flag. When a read operation is performed on the Interrupt Flag Register, the bits are transferred to the processor on the data bus, as the diagram below, indicates.



The PA7 flag is cleared when the Interrupt Flag Register is read. The timer flag is cleared when the timer register is either written or read.

Addressing

Addressing of the UM6532 is accomplished by the 7 address inputs, the $\overline{RS}$ input and the two chip select inputs $\overline{CS1}$ and $\overline{CS2}$. To address the RAM, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ low. To address the I/O and Interval Timer CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. As can be seen to access the chip CS1 is high and $\overline{CS2}$ is low. To distinguish between RAM or I/O-Timer Section the $\overline{RS}$ input is used. When this input is low the RAM is addressed, when high the I/O Interval Timer section is addressed. To distinguish between Timer and I/O, address line A2 is utilized. When A2 is high the Interval Timer is accessed. When A2 is low the I/O section is addressed. Table 1 illustrates the chip addressing.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, PA7 can function as an edge sensitive input. In this mode, an active transition on PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, and providing the PA7 interrupt is enabled, the IRQ output will go low.

Control of the PA7 edge detecting logic is accomplished by performing a write operation to one of four addresses. The data lines for this operation are "don't care" and the addresses to be used are found in Table 1.

The setting of the internal interrupt flag by an active transition on PA7 is always enabled, whether PA7 is set up as an input or an output.

The $\overline{RES}$ signal disables the PA7 interrupt and sets the active transition to the negative edge-detect state. During the reset operation, the interrupt flag may be set by a negative transition. It may, therefore, be necessary to clear the flag before its normal use as an edge detecting input is enabled. This can be achieved by reading the Interrupt Flag Register.

I/O Register-Timer Addressing

Table 1 illustrates the address deconding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the Timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the "divide-by" matrix. This decoding is defined in Table 1. In addition. Address A3 is used to enable the interrupt flag to $\overline{IRQ}$.

Table 1 Addressing Decode

Functions	$\overline{RS}$	A6	A5	A4	A3	A2	A1	A0	WR	RD
RAM	L	X	X	X	X	X	X	X	✓	✓
ORA	H	–	–	–	–	L	L	L	✓	✓
DDRA	H	–	–	–	–	L	L	H	✓	✓
ORB	H	–	–	–	–	L	H	L	✓	✓
DDRB	H	–	–	–	–	L	H	H	✓	✓
Time, ÷1, IRQ ON	H	–	–	H	H	H	L	L	✓	
Timer, ÷8, IRQ ON	H	–	–	H	H	H	L	H	✓	
Timer, ÷64, IRQ ON	H	–	–	H	H	H	H	L	✓	
Timer, ÷1024, IRQ ON	H	–	–	H	H	H	H	H	✓	
Timer, ÷1, IRQ OFF	H	–	–	H	L	H	L	L	✓	
Timer, ÷8, IRQ OFF	H	–	–	H	L	H	L	H	✓	
Timer, ÷64, IRQ OFF	H	–	–	H	L	H	H	L	✓	
Timer, ÷1024, IRQ OFF	H	–	–	H	L	H	H	H	✓	
Read Timer, IRQ ON	H	–	–	–	H	H	–	L		✓
Read Timer, IRQ OFF	H	–	–	–	L	H	–	L		✓
Read Interrupt Flags	H	–	–	–	–	H	–	H		✓
RA7 IRQ OFF, NEG EDGE	H	–	–	L	–	H	L	L	*	
PA7 IRQ OFF, POS EDGE	H	–	–	L	–	H	L	H	*	
PA7 IRQ ON, NEG EDGE	H	–	–	L	–	H	H	L	*	
PA7 IRQ ON, POS EDGE	H	–	–	L	–	H	H	H	*	

Notes: X = Address – = Address bits don't care * = Data bits are "don't care"

Ordering Information

Part Number	Speed	Package
UM6532	1 MHz	Plastic
UM6532A	2 MHz	Plastic