UM8048/8035/8049/8039

Single Chip 8-Bit Microcomputer

Features

- 8-Bit CPU, ROM, RAM, I/O in single package
- Single 5V supply
- Up to 1.36 μsec instruction cycle for 11 MHz operation. All instructions 1 or 2 cycles
- Basic machine instructions: 96
  1-byte instructions: 68
  2-byte instructions: 28
- Single level interrupt
- UM8048/8049 is interchangeable with Intel's P8048/8049 in pin configuration and electrical characteristics
- UM8049-2K x 8 ROM 128 x 8 RAM 27 I/O Lines
  UM8048-1K x 8 ROM 64 x 8 RAM 27 I/O Lines
- Internal timer/event counter
- Easily expandable memory and I/O
- Compatible with MCS memory and I/O

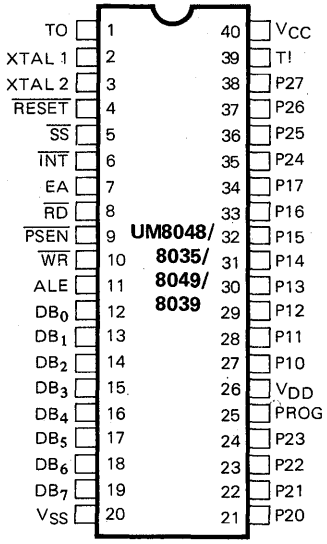
General Description

The UM8048/8035/8049/8039 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using UMC N-channel silicon gate MOS process.

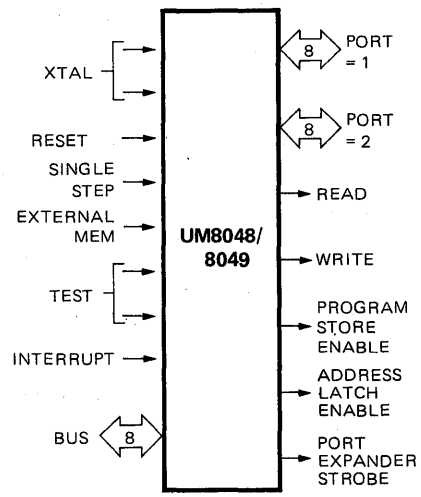
The UM8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. The UM8049 contains a 2K x 8 program memory, a 128 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the UM8048/8049 can be expanded using standard memories and MCS-48, MCS-80 and MCS-85 peripherals. The UM8035 is the equivalent of an UM8048 without program memory. The UM8039 is the equivalent to an UM8049 without program memory.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The UM8048/8049 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and non instructions over two bytes in length.

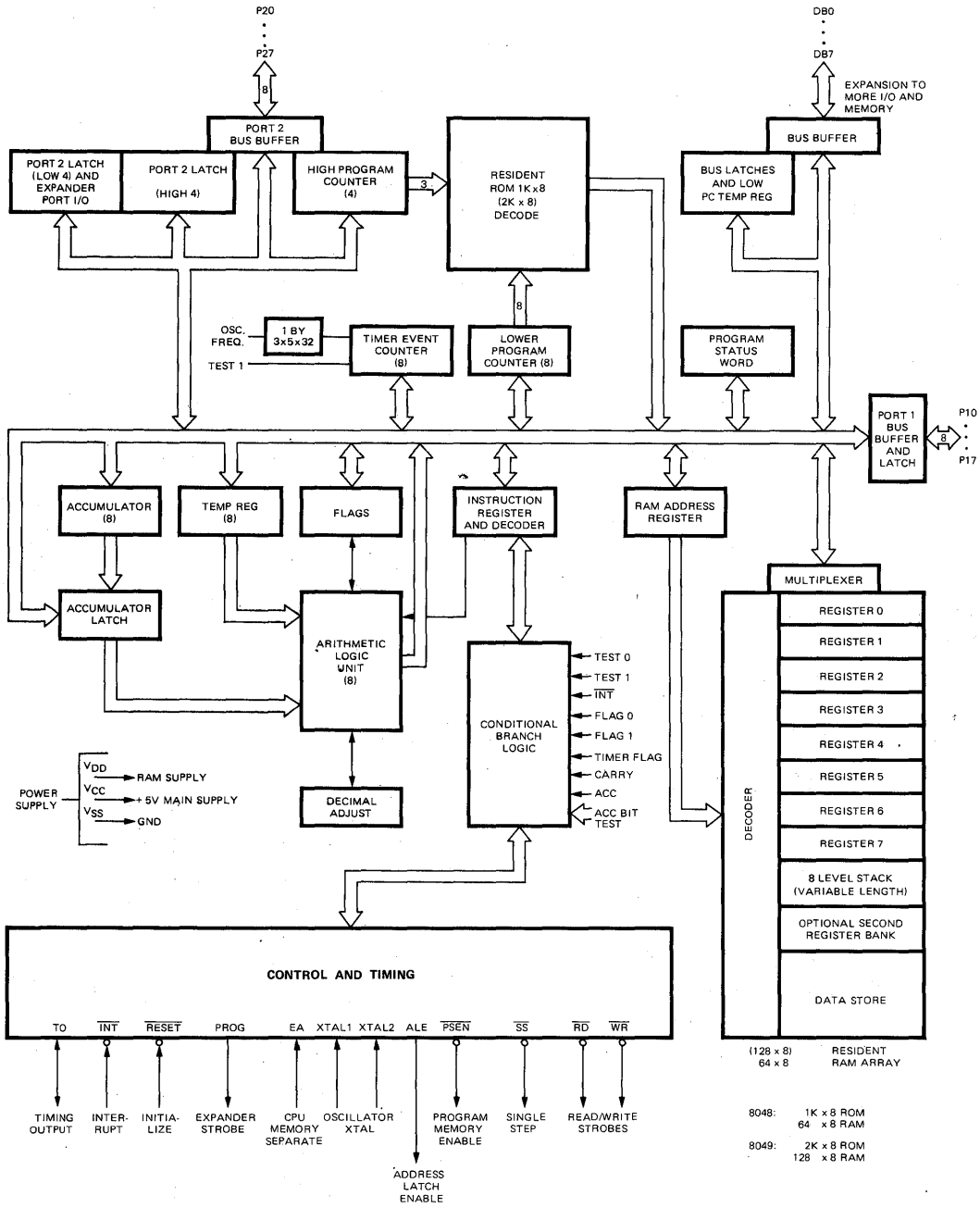
Pin Configuration



Logic Symbol



Block Diagram



Absolute Ratings*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Voltage on Any Pin . . . . . −0.5V to +7V
Power Dissipation 1.5W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(T = 0°C – 70°C V_{CC} = V_{DD} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
Input Low Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	V_{IL}	−0.5		0.8	V	
Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage ($\overline{RESET}$, XTAL1, XTAL2)	V_{IH1}	3.8		V_{CC}	V	
Input Low Voltage ($\overline{RESET}$, XTAL1, XTAL2)	V_{IL1}	V_{SS}		0.5	V	
Output Low Voltage (BUS)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}			0.45	V	I_{OL} = 1.8 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 1.0 mA
Output Low Voltage (All Other Outputs)	V_{OL3}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage (BUS)	V_{OH}	2.4			V	IOH = −400 μA
Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	2.4			V	I_{OH} = −100 μA
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	I_{OH} = −40 μA
Input Leakage Current (T1, $\overline{INT}$)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$)	I_{IL1}			−500	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
Input Leakage Current ($\overline{RESET}$)	I_{IL2}	20		−300	=A	$V_{CC} \geq V_{IN} \geq V_{IL1}$
Output Leakage Current (BUS, T0) (High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
Power Down Supply Current	I_{DD}			8	mA	8MHz, 6MHz
				12		11MHz
Total Supply Current	I_{DD} + I_{CC}		35	70	mA	8MHz, 6MHz
			45	100		11MHz

A.C. Characteristics

(T_A = 0°C – 70°C, V_{CC} = V_{DD} = +5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Limits						Units	Test Conditions(1)
		6MHz		8MHz		11MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{CY}	2.5	15.0	1.875	15.0	1.36	15.0	μs	
ALE Pulse Width	t_{LL}	410		270		150		ns	
Address Setup Before ALE	t_{AL}	200		140		70		ns	
Address Hold From ALE	t_{LA}	120		85		50		ns	
Control Pulse Width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	1050		730		480		ns	
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}	800		550		350		ns	
Data Setup Before $\overline{WR}$	t_{DW}	880		610		390		ns	
Data Hold After $\overline{WR}$	t_{WD}	115		75		40		ns	(2)
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	0	220	0	160	0	110	ns	
$\overline{RD}$ to Data in	t_{RD1}		800		520		330	ns	
$\overline{PSEN}$ to Data in	t_{RD2}		550		330		190	ns	
Address Setup Before $\overline{WR}$	t_{AW}	850		470		300		ns	
Address Setup Before Data in ($\overline{RD}$)	t_{AD1}		1680		1100		730	ns	
Address Setup Before Data in ($\overline{PSEN}$)	t_{AD2}	1250			720		460	ns	
Address Float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	290		210		140		ns	(2)
Address Float to $\overline{PSEN}$	t_{AFC2}	40		20		10		ns	(2)
Control Pulse ALE ($\overline{RD}$, $\overline{WR}$)	t_{CA1}	120		85		50		ns	
Control Pulse to ALE ($\overline{PSEN}$)	t_{CA2}	620		460		320		ns	
Interrupt Pulse Width	t_{INT}	3		3		3		MC	(3)
Power on Reset Time	t_{RES}	5		5		5		MC	(3)

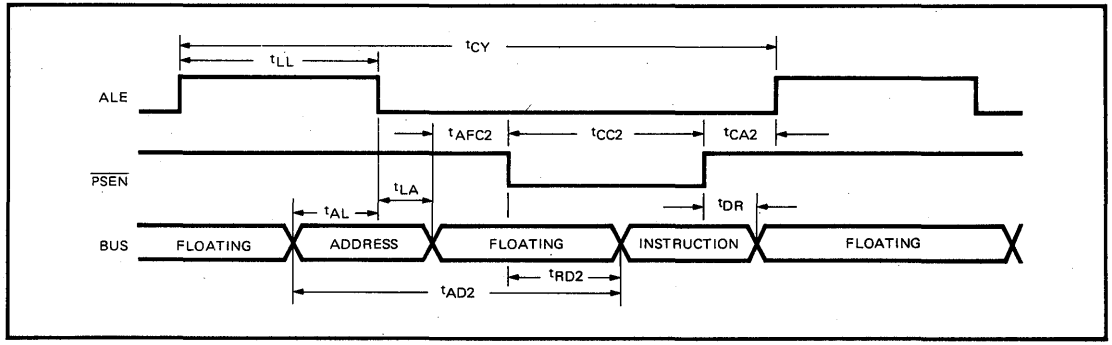
A.C. Characteristics (Continued)

Parameter	Symbol	Limits						Unit	Test Conditions(1)
		6MHz		8MHz		11MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		
Port Control Setup Before Falling Edge of PROG	t_{CP}	200		110		100		ns	
Port Control Hold After Falling Edge of PROG	t_{PC}	460		300		160		ns	
PROG to P2 Input must be Valid	t_{PR}		1300		940		650	ns	
Output Data Setup Time	t_{DP}	850		600		400		ns	
Output Data Hold Time	t_{PD}	200		130		90		ns	
Input Data Hold Time	t_{PF}	0	250	0	190	0	140	ns	
PROG Pulse Width	t_{PP}	1500		1060		700		ns	
Port 2 I/O Data Setup to ALE	t_{PL}	460		300		160		ns	
Port 2 I/O Data Hold to ALE	t_{LP}	150		90		40		ns	
Port Output From ALE	t_{PV}		850		660		510	ns	

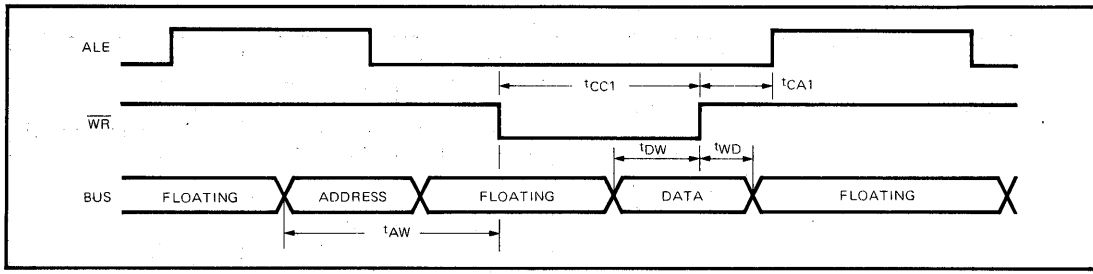
Notes: (1) Control Outputs C_L = 80 pf, Bus Outputs C_L = 150 pf
(2) Bus High Impedance Load 20 pf
(3) MC means machine cycle

Waveforms

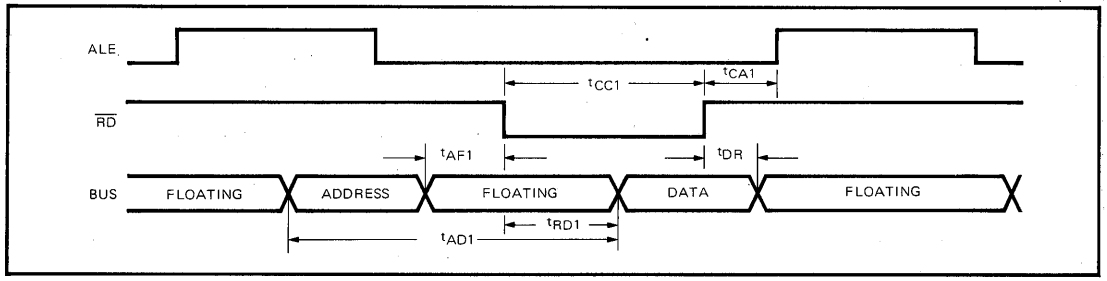
INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



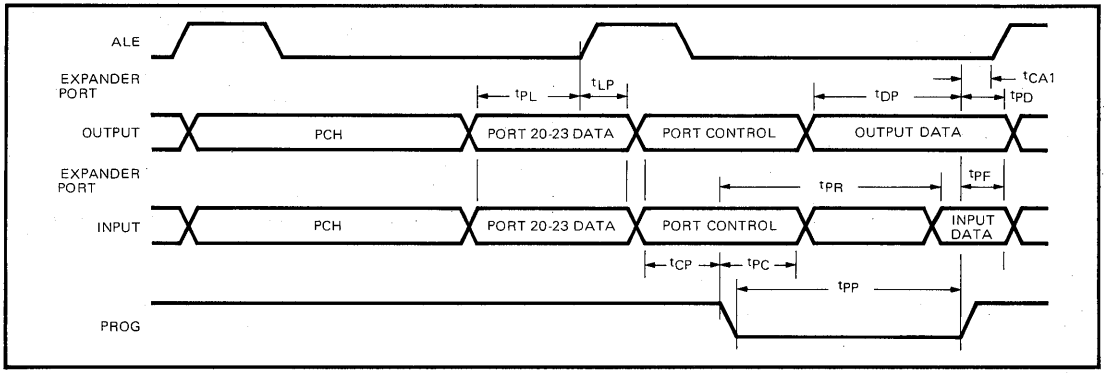
WRITE TO EXTERNAL DATA MEMORY



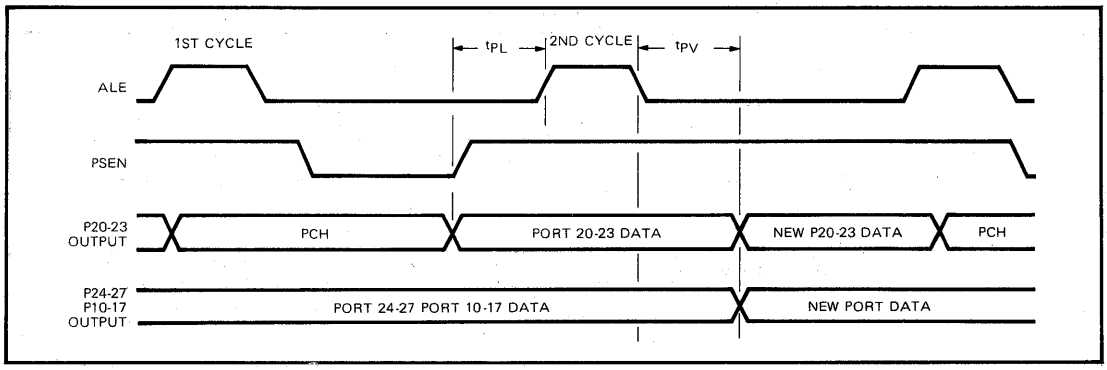
READ FROM EXTERNAL DATA MEMORY



PORT 2 TIMING



I/O PORT TIMING



Pin Description

Designation	Pin	Functions
V_{SS}	20	Circuit GND Potential
V_{DD}	26	+5V during operation. Low power standby pin
V_{CC}	40	Main power supply; +5V during operation
PROG	25	Output strobe for UM8243 I/O expander
Port 1: P10-P17	27-34	8-bit quasi-bidirectional port
Port 2:		
P24-P27	35-38	8-bit quasi-bidirectional port
P20-P23	21-24	P20-P23 contain the four high order program counter bits during an external program fetch and serve as a 4-bit I/O expander bus for UM8243.
BUS: D0-D7	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under control of $\overline{PSEN}$. They also contains the address and data during an external RAM data access instruction under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as clock output using ENTO CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$ (Active Low)	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active Low)
$\overline{RD}$ (Active Low)	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. Used as a Read Strobe to External Data Memory.
$\overline{WR}$ (Active Low)	10	Output strobe during a BUS write. Used as write strobe to External Data Memory.
$\overline{RESET}$ (Active Low)	4	Input which is used to initialize the processor. Also used during verification, and power down.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$ (Active Low)	9	Program Store Enable. This output occurs only during a fetch to external program memory.
$\overline{SS}$ (Active Low)	5	Single step input can be used in conjuction with ALE to "single step" the processor through each instruction
EA	7	External Access input which forcess all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification
XTAL1	2	One side of crystal input for internal oscillator Also input for external source.
XTAL2	3	Other side of crystal input

Instruction Set

Mnemonic	Functions	Descriptions	Instruction Codes D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
		Accumulntor										
ADD A, #data	(A)←(A) + data	Add immediate the specified Data to the Accumulator	0 d7	0 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	2	2
ADD A, Rr	(A)←(A) + (Rr) for r = 0–7	Add contents of designated register to the Accumulator	0	1	1	0	1	r	r	r	1	1
ADD A,@ Rr	(A)←(A) + ((Rr)) for r = 0–1	Add indirect the contents of the data memory location to the Accumulator	0	1	1	0	0	0	0	r	1	1
ADDC A;# data	(A)←(A) + (C) + data	Add immediate with carry the specified data to the Accumulator	0 d7	0 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	2	2
ADDC A, Rr	(A)←(A) + (C) + (Rr) for r = 0–7	Add with carry the contents of the designated register to the Accumulator	0	1	1	1	1	r	r	r	1	1
ADDC A,@ Rr	(A)←(A) + (C) + ((Rr)) for r = 0–1	Add indirect with carry the contents of data memory location to the Accumulator	0	1	1	1	0	0	0	r	1	1
ANL A, #data	(A)←(A) AND data	Logical AND specified immediate Data with Accumulator	0 d7	1 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	2	2
ANL A, Rr	(A)←(A) AND (Rr) for r = 0–7	Logical NAD contents of designated register with Accumulator	0	1	0	1	1	r	r	r	1	1
ANL A,@ Rr	(A)←(A) AND ((Rr)) for r = 0–1	Logical AND indirect the contents of data memory with Accumulator	0	1	0	1	0	0	0	r	1	1
CPL A	(A)← NOT (A)	Complement the contents of the Accumulator	0	0	1	1	0	1	1	1	1	1
CLR A	(A)←0	Clear the contents of the Accumulator	0	0	1	0	0	1	1	1	1	1
DA A		Decimal Adjust the contents of the Accumulator	0	1	0	1	0	1	1	1	1	1
DEC A	(A)←(A) – 1	Decrement by 1 the Accumulator's contents	0	0	0	0	0	1	1	1	1	1
INC A	(A)←(A) + 1	Increment by 1 the Accumulator's contents	0	0	0	1	0	1	1	1	1	1
ORL A, #data	(A)←(A) OR data	Logical OR specified immediate data with Accumulator	0 d7	1 d6	0 d5	0 d4	0 d3	0 d2	1 d1	1 d0	2	2
ORL A, Rr	(A)←(A) OR (Rr) fro r = 0–7	Logical OR contents of designated register with Accumulator	0	1	0	0	1	r	r	r	1	1
ORL A,@ Rr	(A)←(A) OR ((Rr)) for r = 0–1	Logical OR indirect the contents of data memory location with Accumulator	0	1	0	0	0	0	0	r	1	1
RL A	(AN+1)←(AN) (A0)←(A7) for N = 0–6	Rotate Accumulator left by 1 bit without carry	1	1	1	0	0	1	1	1	1	1
RLC A	(AN+1)←(AN); N = 0–6, (A0)←(C) (C)←(A7)	Rotate Accumulator left by 1 bit through carry	1	1	1	1	0	1	1	1	1	1
RR A	(AN)←(AN+1); N = 0–6, (A7)←(A0)	Rotate Accumulator right by 1 bit without carry	0	1	1	1	0	1	1	1	1	1
RRC A	(AN)←(AN+1); N = 0–6, (A7)←(C) (C)←(A0)	Rotate Accumulator right by 1 bit through carry	0	1	1	0	0	1	1	1	1	1
SWAP A	(A4–7)⇌(A0–3)	Swap the two 4-bit nibbles in the Accumulator	0	1	0	0	0	1	1	1	1	1
XRL A1, # data	(A)←(A) XOR data	Logic XOR specified immediate data with Accumulator	1 d7	1 d6	0 d5	1 d4	0 d3	0 d2	1 d1	1 d0	2	2
XRL A, Rr	(A)←(A) XOR (Rr) for r = 0–7	Logical XOR contents of designated register with Accumulator	1	1	0	1	1	r	r	r	1	1
XRL A,@ Rr	(A)←(A) XOR ((Rr)) for r = 0–1	Logical XOR indirect the contents of data memory location with Accumulator	1	1	0	1	0	0	0	r	1	1

Instruction Set (Continued)

Mnemonic	Functions	Descriptions	Instruction Codes D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
		Branch										
DJNZ Rr, addr	(Rr)←(Rr)−1; r=0–7 If (Rr) ≠ 0 (PC0–7)←addr	Decrement the specified register and test contents	1 a7	1 a6	1 a5	0 a4	1 a3	r a2	r a1	r a0	2	2
JBb addr	(PC0–7)←addr if Bb=1 (PC)←(PC)+2 if Bb=0	Jump to specified address if Accumulator bit is set	b2 a7	b1 a6	b0 a5	1 a4	0 a3	0 a2	1 a1	0 a0	2	2
JC addr	(PC0–7)←addr if C=1 (PC)←(PC)+2 if C=0	Jump to sepecified address if carry flag is set	1 a7	1 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JF0 addr	(PC0–7)←addr if P0=1 (PC)←(PC)+2 if F0=0	Jump to specified address if Flag F0 is set	1 a7	0 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JF1 addr	(PC0–7)←addr if F1=1 (PC)←(PC)+2 if F1=0	Jump to specified address if Flag F1 is set	0 a7	1 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JMP addr	(PC8–10)←addr 8–10 (PC0–7)←addr 0–7 (PC11)←DBF	Direct Jump to specified address within the 2K address block	a10 a7	a9 a6	a8 a5	0 a4	0 a3	1 a2	0 a1	0 a0	2	2
JMPP @A	(PC0–7)←((A))	Jump indirect to specified address with address page	1	0	1	1	0	0	1	1	2	1
JNC addr	(PC0–7)←addr if C=0 (PC)←(PC)+2 if C=1	Jump to specified address if carry flag is low	1 a7	1 a6	1 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
JN1 addr	(PC0–7)←addr if I=0 (PC)←(PC)+2 if I=1	Jump to specified address if interrupt is low	1 a7	0 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
JNT0 addr	(PC0–7)←addr if T0=0 (PC)←(PC)+2 if T0=1	Jump to specified address if Test 0 is low	0 a7	0 a6	1 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
JNT1 addr	(PC0–7)←addr if T1=0 (PC)←(PC)+2 if T1=1	Jump to specified address if Test 1 is low	0 a7	1 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
JNZ addr	(PC0–7)←addr if A≠0 (PC)←(PC)+2 if A=0	Jump to specified address if Accumulator is non-zero	1 a7	0 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JTF addr	(PC0–7)←addr if TF=1 (PC)←(PC)+2 if TF=0	Jump to specified address if Timer Flag is set to 1	0 a7	0 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JT0 addr	(PC0–7)←addr if T0=1 (PC)←(PC)+2 if T0=0	Jump to specified address if Test 0 is a 1	0 a7	0 a6	1 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JT1 addr	(PC0–7)←addr if T1=1 (PC)←(PC)+2 if T1=0	Jump to specified address if Test 1 is a 1	0 a7	1 a6	0 a5	1 a4	0 a3	1 a2	1 a1	0 a0	2	2
JZ addr	(PC07)←addr if A=0 (PC)←(PC)+2 if A≠0	Jump to specified address if Accumulator is 0	1 a7	1 a6	0 a5	0 a4	0 a3	1 a2	1 a1	0 a0	2	2
		Control										
EN I		Enable the External Interrup input	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the External Interrupt input	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enable the Clock Output pin T0	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF)←0	Select Bank 0-(locations 0-02047) of program Memory	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF)←1	Select Bank 1 (locations 2048-4095) of Program Memory	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS)←0	Select Bank 0 (locations 0-7) of Data Memory	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS)←1	Select Bank 1 (locations 24-31) of Data Memory	1	1	0	1	0	1	0	1	1	1
		Data Moves										
MOV A, #data	(A)←data	Move immediate the specified data into the Accumulator	0 d7	0 d6	1 d5	0 d4	0 d3	0 d2	1 d1	1 d0	2	2
MOV A, Rr	(A)←(Rr); r=0–7	Move the contents of the designated registers into the Accumulator	1	1	1	1	1	r	r	r	1	1

Instruction Set (Continued)

Mnemonic	Functions	Descriptions	Instruction Codes D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
		Data Moves (Cont.)										
MOV A, @ Rr	(A) ← ((Rr)); r=0–1	Move indirect the contents data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator	1	1	0	0	0	1	1	1	1	1
MOV Rr, # data	(Rr) ← data; r=0–7	Move immediate the spocified data into the designated register	1 d7	0 d6	1 d5	1 d4	1 d3	r d2	r d1	r d0	2	2
MOV Rr, A	(Rr) ← (A); r=0–7	Move Accumulator Contents into the designated register	1	0	1	0	1	r	r	r	1	1
MOV @ Rr, A	((Rr)) ← (A), r=0–1	Move indirect Accumulator Contents into data memory location	1	0	1	0	0	0	0	r	1	1
MOV @ Rr, # data	((Rr)) ← data; r=0–1	Move immediate the specified data into data memory	1 d7	0 d6	1 d5	1 d4	0 d3	0 d2	0 d1	r d0	2	2
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word	1	1	0	1	0	1	1	1	1	1
MOVP A, @ A	(PC0–7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	(PC0–7) ← (A) (PC8–10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	(A) ← ((Rr)); r=0–1	Move indirect the contents of external data memory into the Accumulator	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	((Rr)) ← (A), r=0–1	Move indirect the contents of the Accumulator into external data memory	1	0	0	1	0	0	0	r	2	1
XCH A, Rr	(A) ⇌ (Rr); r=0–7	Exchange the Accumulator and designated register's contents	0	0	1	0	1	r	r	r	1	1
XCH A, @ Rr	(A) ← ((Rr)); r=0–1	Exchange indirect contents of Accumulator and location in data memory	0	0	1	0	0	0	0	r	1	1
XCHD A, @ Rr	(A0–3) ⇌ ((Rr0–3)); r=0–1	Exchange indirect 4 bit contents of Accumulator and data memory	0	0	1	1	0	0	0	r	1	1
		Flags										
CPL C	(C) ← NOT (C)	Complement carry bit	1	0	1	0	0	1	1	1	1	1
CPL F0	(F0) ← NOT (F0)	Complement Flag F0	1	0	0	1	0	1	0	1	1	1
CPL F1	(F1) ← NOT (F1)	Complement Flag F1	1	0	1	1	0	1	0	1	1	1
CLR C	(C) ← 0	Clear carry bit to 0	1	0	0	1	0	1	1	1	1	1
CLR F0	(F0) ← 0	Clear Flag 0 to 0	1	0	0	0	0	1	0	1	1	1
CLR F1	(F1) ← 0	Clear Flag 1 to 0	1	0	1	0	0	1	0	1	1	1
		Input/Output										
ANL BUS, #. data	(BUS) ← (BUS) AND data	Logical AND immediate specified data with contents of Bus	1 d7	0 d6	0 d5	1 d4	1 d3	0 d2	0 d1	0 d0	2	2
ANL Pp, # data	(Pp) ← (Pp) AND data p=1–2	Logical AND immediate specified data with designated port (1 or 2)	1 d7	0 d6	0 d5	1 d4	1 d3	0 d2	p d1	p d0	2	2
ANLD Pp, A	(Pp) ← (Pp) AND (A0–3) p=4–7	Logical AND contents of Accumulator with designated port (4–7)	1	0	0	1	1	1	p	p	2	1
IN A, Pp	(A) ← (Pp), p=1–2	Input data from designated port (1–2) into Accumulator	0	0	0	0	1	0	p	p	2	1
INS A, BUS	(A) ← (BUS)	Input strobed Bus data into Accumulator	0	0	0	0	1	0	0	0	2	1
MOVD A, Pp	(A0–3) ← (Pp); p=4–7 (A1–7) ← 0	Move contents of designated port (4–7) into Accumulator	0	0	0	0	1	1	p	p	2	1
MOVD Pp, A	(Pp) ← A0–3; p=4–7	Move contents of Accumulator into designated port (4–7)	0	1	1	1	1	p	p	1	2	1

Instruction Set (Continued)

Mnemonic	Functions	Descriptions	Instruction Codes D7	D6	D5	D4	D3	D2	D1	D0	Cycles	Bytes
		Input/Output (Cont.)										
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical OR immediate specified data with contents of Bus	1 d7	0 d6	0 d5	0 d4	1 d3	0 d2	0 d1	0 d0	2	2
ORLD Pp, A	(Pp) ← (Pp) OR (A0–3) p=4–7	Logical OR contents of Accumulator with designated port (4–7)	1	0	0	0	1	1	p	p	2	1
ORL Pp, # data	(Pp) ← (Pp) OR data p=1–2	Logical OR immediate specified data with designated port (1–2)	1 d7	0 d6	0 d5	0 d4	1 d3	0 d2	p d1	p d0	2	2
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto Bus	0	0	0	0	0	0	1	0	2	1
OUTL Pp, A	(Pp) ← (A); p=1–2	Output contents of Accumulator to designated port (1–2)	0	0	1	1	1	0	p	p	2	1
		Register										
DEC Rr	(Rr) ← (Rr) – 1; r=0–7	Decrement by 1 contents of designated register	1	1	0	0	1	r	r	r	1	1
INC Rr	(Rr) ← (Rr) + 1; r=0–7	Increment by 1 conents of designated register	0	0	0	1	1	r	r	r	1	1
INC @ R	((Rr)) ← ((Rr)) + 1; r=0–1	Increment indirect by 1 the contents of data memory location	0	0	0	1	0	0	0	r	1	1
		Subroutine										
Call addr	((SP)) ← (PC), (PSW4–7) (SP) ← (SP) + 1 (PC8–10) ← addr 8–10 (PC0–7) ← addr 0–7 (PC11) ← DBF	Call designated Subroutine	a10 a7	a9 a6	a8 a5	1 a4	0 a3	1 a2	0 a1	0 a0	2	2
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW4–7) ← ((SP))	Return from Subroutine restoring Program Status Word	1	0	0	1	0	0	1	1	2	1
		Timer/Counter										
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stop Count for Event Counter	0	1	1	0	0	1	0	1	1	1
STRT CNT		Start Count for Event Counter	0	1	0	0	0	1	0	1	1	1
STRT T		Start Counter foe Timer	0	1	0	1	0	1	0	1	1	1
		Miscellaneous										
NOP		No Operation performed	0	0	0	0	0	0	0	0	1	1

Notes: 1. Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
2. References to the address and data are specified in bytes 2 and/or 1 of the instruction.
3. Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Ordering Information

Part Number	Max. Freq.
UM8035-6	6 MHz
UM8039-6	
UM8035-8	8 MHz
UM8039-8	
UM8035-11	11 MHz
UM8039-11	