UM8051 / UM8031

Single Chip 8-Bit Microcomputer

Features

- 4K x 8 ROM
- 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128K
- Boolean processor
- UM8048 architecture enhanced with:
  - Non-paged jumps
  - Direct addressing
  - Four 8-register banks
  - Stack depth up to 128-bytes
  - Multiply, divide, subtract, compare
- Most instructions execute in 1μs
- 4μs multiply and divide

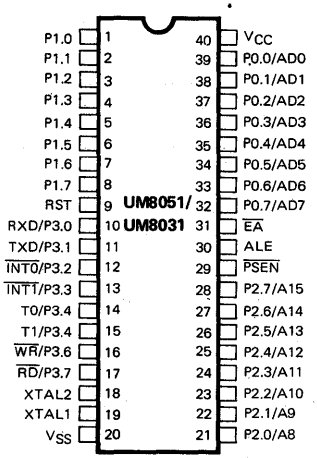
General Description

The UM8051/8031 is a stand-alone, high-performance single-chip computer fabricated with UMC's highly-reliable +5 Volt, NMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

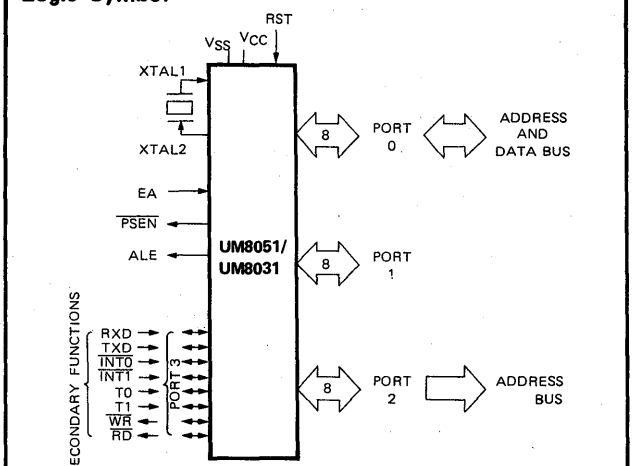
The UM8051/8031 contains a non-volatile 4K x 8 read-only program memory, a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The UM8031 is identical, except that it lacks the program memory. For systems that require extra capability, the UM8051 can be expanded using standard TTL compatible memories.

The UM8051 microcomputer, like its UM8048 predecessor, is efficient both as a controller and as an arithmetic processor. The UM8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1μs, 40% in 2μs and multiply and divide require only 4μs. Among the many instructions added to the standard UM8048 instruction set are multiply, divide, subtract and compare.

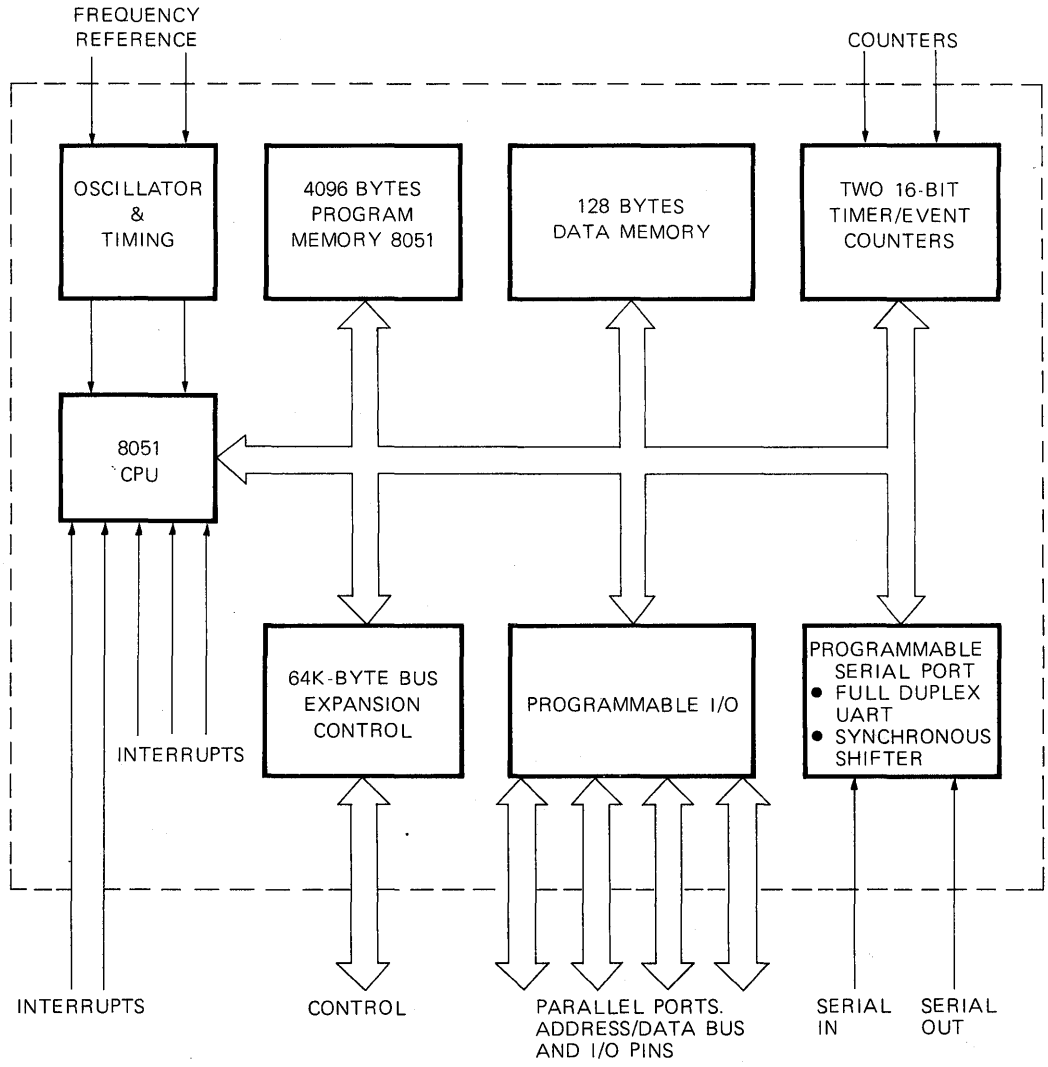
Pin Configuration



Logic Symbol



Block Diagram



Pin Description

Designation	Pin	Functions
V_{SS}	20	Circuit ground potential.
V_{CC}	40	+5V power supply during operation and program verification.
Port 0	32-39	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data input and output during programming and verification. Port 0 can sink/source eight TTL loads.
Port 1	1-8	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four TTL load.
Port 2	21-28	Port 2 is an 8-bit bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four TTL load.
Port 3	10-17	Port 3 is an 8-bit quasi-bidirectional I/O port with internal pullups. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four TTL load. The secondary function are assigned to the pins of Port 3, as follows: –RXD/data (P3.0). Serial port's receiver data input (asynchronous). –TXD/clock (P3.1). Serial port's transmitter data output (asynchronous). –$\overline{INT0}$ (P3.2). Interrupt 0 input. –$\overline{INT1}$ (P3.3). Interrupt 1 input. –T0 (P3.4). Input to counter 0. –T1 (P3.5). Input to counter 1. –$\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. –$\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.
RST	9	A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor ($\approx 8.2k\Omega$) from RST to V_{SS} permits power-on reset when a capacitor ($\approx 10\,\mu f$) is also connected from this pin to V_{CC}.
ALE	30	Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs.
$\overline{PSEN}$	29	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods except during external data memory access. $\overline{PSEN}$ remains high during internal program execution.
$\overline{EA}$	31	When held at a TTL high level, the 8051 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the 8031/8051 fetches all instructions from external Program Memory. Do not float $\overline{EA}$ during normal operation.
XTAL1	19	Input to the inverting amplifier that forms part of the oscillator. This pin should be connected to ground when an external oscillator is used.
XTAL2	18	Output of the inverting amplifier that forms part of the oscillator, and input to the internal clock generator. XTAL2 receives the oscillator signal when an external oscillator is used.

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

Voltage on Any Pin With Respect to

Ground (V_{SS}) . . . . . −0.5V to +7V

Power Dissipation . . . . . 1 Watts

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

(T_A = 0°C to 70°C; V_{CC} = 5V ± 10%; V_{SS} = 0V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
VIL	Input Low Voltage	−0.5	0.8	V	
VIH	Input High Voltage (Except RST and XTAL2)	2.0	V_{CC} + 0.5	V	
VIH1	Input High Voltage to RST For Reset. XTAL2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
VOL	Output Low Voltage Ports 1, 2, 3 (Note 1)		0.45	V	IOL = 1.6mA
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$ (Note 1)		0.45	V	IOL = 3.2mA
VOH	Output High Voltage Ports 1, 2, 3	2.4		V	IOH = −80μA
VOH1	Output High Voltage Port 0, ALE, $\overline{PSEN}$	2.4		V	IOH = −400μA
IIL	Logical 0 Input Current Ports 1, 2, 3		−800	μA	Vin = 0.45V
IIL2	Logical 0 Input Current for XTAL2		−2.5	mA	XTAL1 = V_{SS}, Vin = 0.45V
ILI	Input Leakage Current To Port 0, $\overline{EA}$		±10	μA	0.45V < Vin < V_{CC}
IIH1	Input High Current to RST/V_{PD} For Reset		500	μA	Vin < V_{CC} − 1.5V
ICC	Power Supply Current		125	mA	All outputs disconnected
CIO	Capacitance of I/O Buffer		10	pF	f_C = 1 MHz, T_A = 25°C

Note: VOL is degraded when the 8031/8051 rapidly discharges external capacitance. This AC noise is most pronounced during emission of address data. When using external memory, locate the latch or buffer as close to the 8031/8051 as possible.

A.C. Characteristics

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, C_L for Port 0, ALE and PSEN Outputs = 100 pF; C_L for all other outputs = 80 pF)

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz 1Clock			Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		
		Min.	Max.	Units	Min.	Max.	Units
TLHLL	ALE Pulse Width	127		ns	2TCLCL-40		ns
TAVLL	Address Setup to ALE	43		ns	TCLCL-40		ns
TLLAX	Address Hold After ALE	48		ns	TCLCL-35		ns
TLLIV	ALE to Valid Instr In		233	ns		4TCLCL-100	ns
TLLPL	ALE To $\overline{PSEN}$	58		ns	TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		ns	3TCLCL-35		ns
TPLIV	$\overline{PSEN}$ To Valid Instr In		125	ns		3TCLCL-125	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns	0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		63	ns		TCLCL-20	ns
TPXAV	Address Valid After $\overline{PSEN}$	75		ns	TCLCL-8		ns
TAVIV	Address To Valid Instr In		302	ns		5TCLCL-115	ns
TAZPL	Address Float To $\overline{PSEN}$	0		ns	0		ns

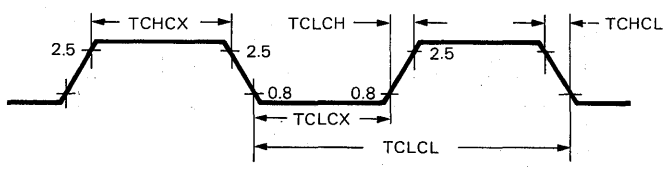
EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		
		Min.	Max.	Unit	Min.	Max.	Unit
TRLRH	$\overline{RD}$ Pulse Width	400		ns	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		ns	6TCLCL-100		ns
TLLAX	Address Hold After ALE	48		ns	TCLCL-35		
TRLDV	$\overline{RD}$ To Valid Data In		250	ns		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns	0		ns
TRHDZ	Data Float After $\overline{RD}$		97	ns		2TCLCL-70	ns
TLLDV	ALE To Valid Data In		517	ns		8TCLCL-150	ns
TAVDV	Address To Valid Data In		585	ns		9TCLCL-165	ns
TLLWL	ALE To $\overline{WR}$ or $\overline{RD}$	200	300	ns	3TCLCL-50	3TCLCL + 50	ns
TAVWL	Address To $\overline{WR}$ or $\overline{RD}$	203		ns	4TCLCL-130		ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ High To ALE High	43	123	ns	TCLCL-40	TCLCL + 40	ns
TDVWX	Data Valid To $\overline{WR}$ Transition	23		ns	TCLCL-60		ns
TQVWH	Data Setup Before $\overline{WR}$	433		ns	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	33		ns	TCLCL-50		ns
TRLAZ	Address Float After $\overline{RD}$		0	ns		0	ns

Datum	Emitting Ports	Degraded I/O Lines	VOL (peak) (Max.)
Address	P2, P0	P1, P3	0.8V
Write Data	P0	P1, P3, ALE	0.8V

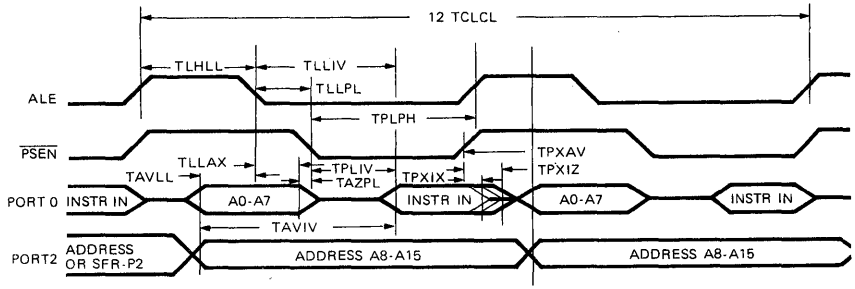
EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL2)

Symbol	Parameter	Variable Clock freq = 3.5 MHz to 12 MHz		Unit
		Min.	Max.	
TCLCL	Oscillator Period	83.3	286	ns
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

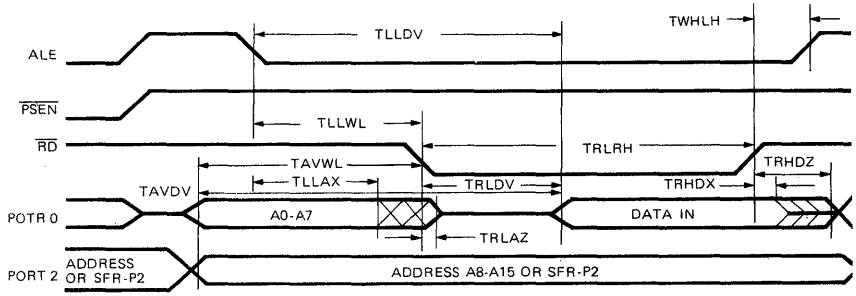


A.C. Timing Diagrams

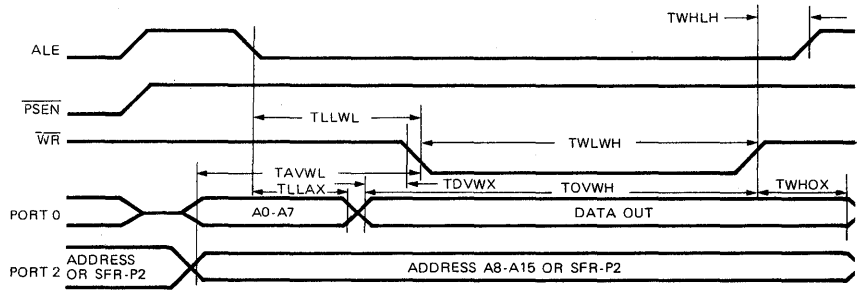
EXTERNAL PROGRAM MEMORY READ CYCLE



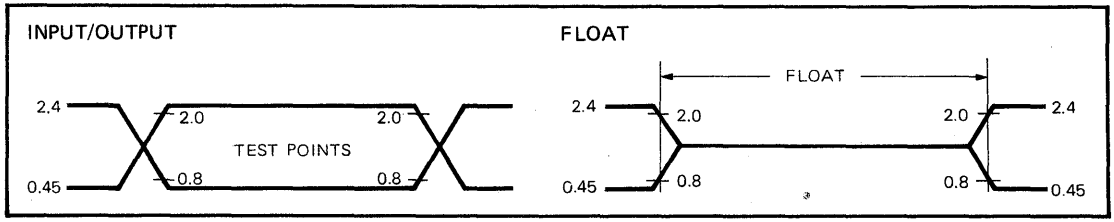
EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

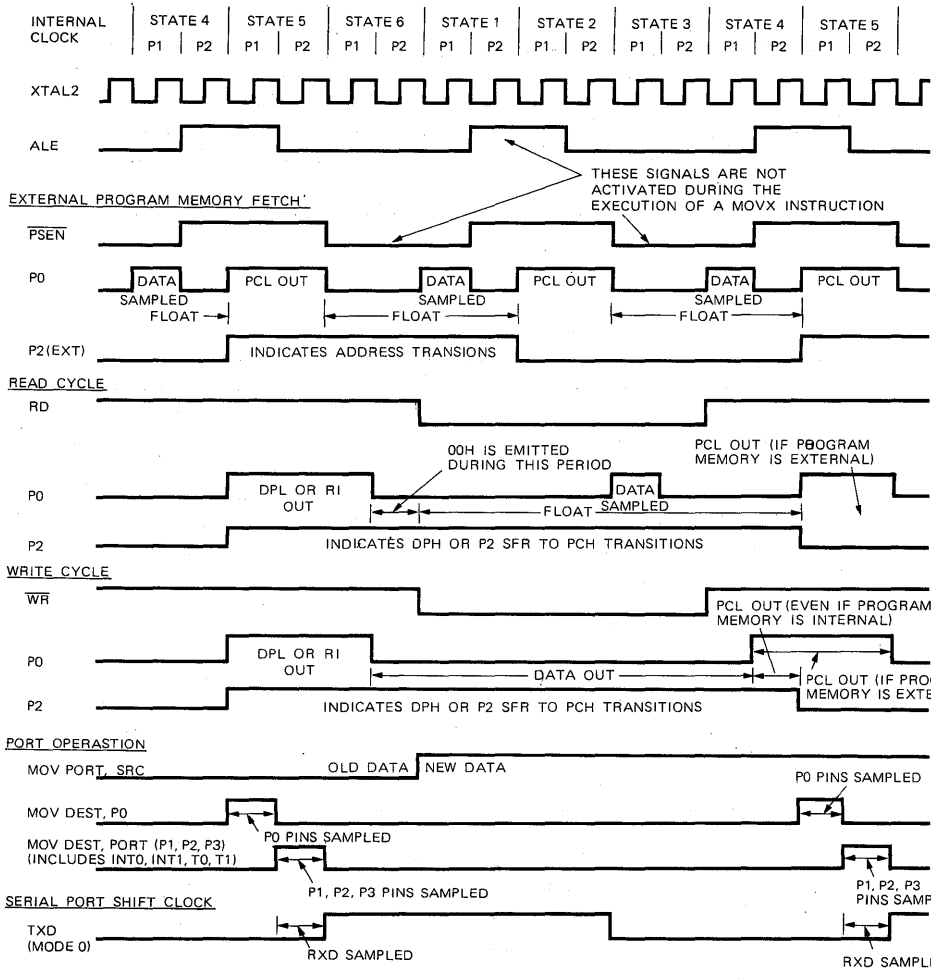


A.C. Testing Input/Output, Float Waveforms



AC inputs during testing are driven at 2.4V for a logic "1" and 0.45V for logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic."0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 μA at the voltage test levels.

Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 15 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

UM8051 Instruction Set Summary

INTERRUPT RESPONSE TIME

To finish execution of current instruction, respond to the interrupt request, push the PC and to vector to the first instruction of the interrupt service program requires 38 to 81 oscillator periods (3 to 7μs @ 12 MHz).

INSTRUCTIONS THAT AFFECT FLAG SETTINGS*

Instruction	Flag		
	C	OV	AC
Add	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	O	X	
DIV	O	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		
CLR C	O		
CPL C	X		
ANL C, bit	X		
ORL C, bit	X		
ORL C, bit	X		
MOV C, bit	X		
CJNE	X		

* Note that operations on SFR byte address 208 or bit addresses 209–215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

Rn

Register R7 – R0 of the currently selected Register Bank.

Data

8-bit internal data location's address. This could be an Internal Data RAM location (0 – 127) or a SFR [i.e., I/O port, control register, status register, etc. (128 – 255)].

@ Ri

8-bit internal data RAM location (0 – 255) addressed indirectly through register R1 or R0.

#data

8-bit constant included in instruction.

#data 16

16-bit constant included in instruction.

Addr. 16

16-bit destination address. Used by LCALL & LJMP. A branch can be anywher within the 64K-byte Program Memory address space.

Addr. 11

11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K-byte page of program memory as the first byte of the following instruction.

Rel

Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is – 128 to +127 bytes relative to first byte of the following instruction.

Bit

Direct Addressed bit in Internal Data RAM or Special Function Register.

* New operation not provided by UM8048/8049.

ARITHMETIC OPERATIONS

Mnemonic	Descriptions	Bytes	Cycles
ADD A, Rn	Add register to accumulator	1	1
ADD A, direct	Add direct byte to accumulator	2	1
ADD A, @ Ri	Add indirect RAM to accumulator	1	1
ADD A, # data	Add immediate data to accumulator	2	1
ADDC A, Rn	Add register to accumulator with carry	1	1
ADDC A, direct	Add direct byte to accumulator with carry	2	1
ADDC A, @ Ri	Add indirect RAM to accumulator with carry	1	1
ADDC A, # data	Add immediate data to Acc with carry	2	1
SUBB A, Rn	Subtract register from Acc with borrow	1	1
SUBB A, direct	Subtract direct byte from Acc with borrow	2	1
SUBB A, @ Ri	Subtract indirect RAM from Acc with borrow	1	1
SUBB A, # data	Subtract immediate data from Acc with borrow	2	1
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @ Ri	Decrement indirect RAM	1	1
INC DPTR	Increment data pointer	1	2
MUL AB	Multiply A & B	1	4
DIV AB	Divide A by B	1	4
DA A	Decimal adjust accumulator	1	1

LOGICAL OPERATIONS

Mnemonic	Descriptions	Bytes	Cycles
ANL R, Rn	AND register accumulator	1	1
ANL A, direct	AND direct byte to accumulator	2	1
ANL A, @ Ri	AND indirect RAM to accumulator	1	1
ANL A, # data	AND immediate data to accumulator	2	1
ANL direct, A	AND accumulator to direct byte	2	1
ANL direct, # data	AND immediate data to direct byte	3	2
ORL A, Rn	OR register to accumulator	1	1
ORL A, direct	OR direct byte to accumulator	3	1
ORL A, @ Ri	OR indirect RAM to accumulator	1	1
ORL A, # data	OR immediate data to accumulator	2	1
ORL direct, A	OR accumulator to direct byte	2	1
ORL direct, # data	OR immediate data to direct byte	3	2
XRL A, Rn	Exclusive-OR register to accumulator	1	1
XRL A, direct	Exclusive-OR direct byte to accumulator	2	1
XRL A, @ Ri	Exclusive-OR indirect RAM to accumulator	1	1
XRL A, # data	Exclusive-OR immediate data to accumulator	2	1
XRL direct, A	Exclusive-OR accumulator to direct byte	2	1
XRL direct, # data	Exclusive-OR immediate data to direct byte	3	2
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through the carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right through the carry	1	1
SWAP A	Swap nibbles within the accumulator	1	1

DATA TRANSFER

Mnemonic	Descriptions	Bytes	Cycles
MOV A, Rn	Move register to accumulator	1	1
MOV A, direct	Move direct byte to accumulator	2	1
MOV A, @ Ri	Move indirect RAM to accumulator	1	1
MOV A # data	Move immediate data to accumulator	2	1
MOV Rn, A	Move accumulator to register	1	1
MOV Rn, direct	Move direct byte to register	2	2
MOV Rn, # direct	Move direct byte to register	2	1
MOV direct, A	Move accumulator to direct byte	2	1
MOV direct, Rn	Move register to direct byte	2	2
MOV direct, direct	Move direct byte to direct	3	2
MOV direct, @ Ri	Move indirect RAM to direct byte	2	2
MOV direct, # data	Move immediate data to direct byte	3	2
MOV @ Ri, A	Move accumulator to indirect RAM	1	1
MOV @ Ri, direct	Move direct byte to indirect RAM	2	2
MOV @ Ri, # data	Move immediate data to indirect RAM	2	1
MOV DPTR, # data 16	Load data pointer with a 16-bit constant	3	2
MOVC A, @ A + DPTR	Move code byte relative to DPTR to Acc	1	2
MOVC A, @ A + PC	Move code byte relative to PC and Acc	1	2
MOVX A, @ Ri	Move external RAM (8-bit addr) to Acc	1	2
MOVX A, @ DPTR	Move external RAM (16-bit addr) to Acc	1	2
MOVX @ Ri, A	Move Acc to external RAM (8-bit addr.)	1	2
MOVX @DPTR, A	Move Acc to external RAM (16-bit addr.)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	1
XCH A, direct	Exchange direct byte with accumulator	2	1
XCH A, @ Ri	Exchange indirect RAM with accumulator	1	1
XCHD A, @ Ri	Exchange low-order digit indirect RAM with Acc	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic	Descriptions	Bytes	Cycles
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	1
ANL C, bit	AND direct bit to carry	2	2
ANL C,/bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C,/bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	2
JC rel	Jump if carry is set	2	2
JNC rel	Jump if carry not set	2	2
JB bit, rel	Jump if direct bit is set	3	2
JNB bit, rel	Jump if direct but is not set	3	2
JBC bit, rel	Jump if direct bit is set & clear bit	3	2

PROGRAMING BRANCHING

Mnemonic	Descriptions	Bytes	Cycles
ACALL addr. 11	Absolute subroutine call	2	2
LCALL addr. 16	Long subroutine call	3	2
RET	Return for subroutine	1	2
RETI	Return for interrupt	1	2
AJMP addr. 11	Absolute jump	2	2
LIMP addr. 16	Long jump	3	2
SJMP rel	Short jump (relative addr.)	2	2
JMP @ A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if accumulator is zero	2	2
JNZ rel	Jump if accumulator is not zero	2	2
CJNE A, direct, rel	Compare direct byte to Acc and jump if not equal	3	2
CJNE A, # data, rel	Compare immediate to Acc and jump if not equal	3	2
CJNE Rn, # data, rel	Compare immediate to register and jump if not equal	3	2
CJNE @ Ri, # data, rel	Compare immediate to indirect and jump if not equal	3	2
DJNZ Rn, rel	Decrement register and jump if not zero	3	2
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	2
NOP	No operation	1	1