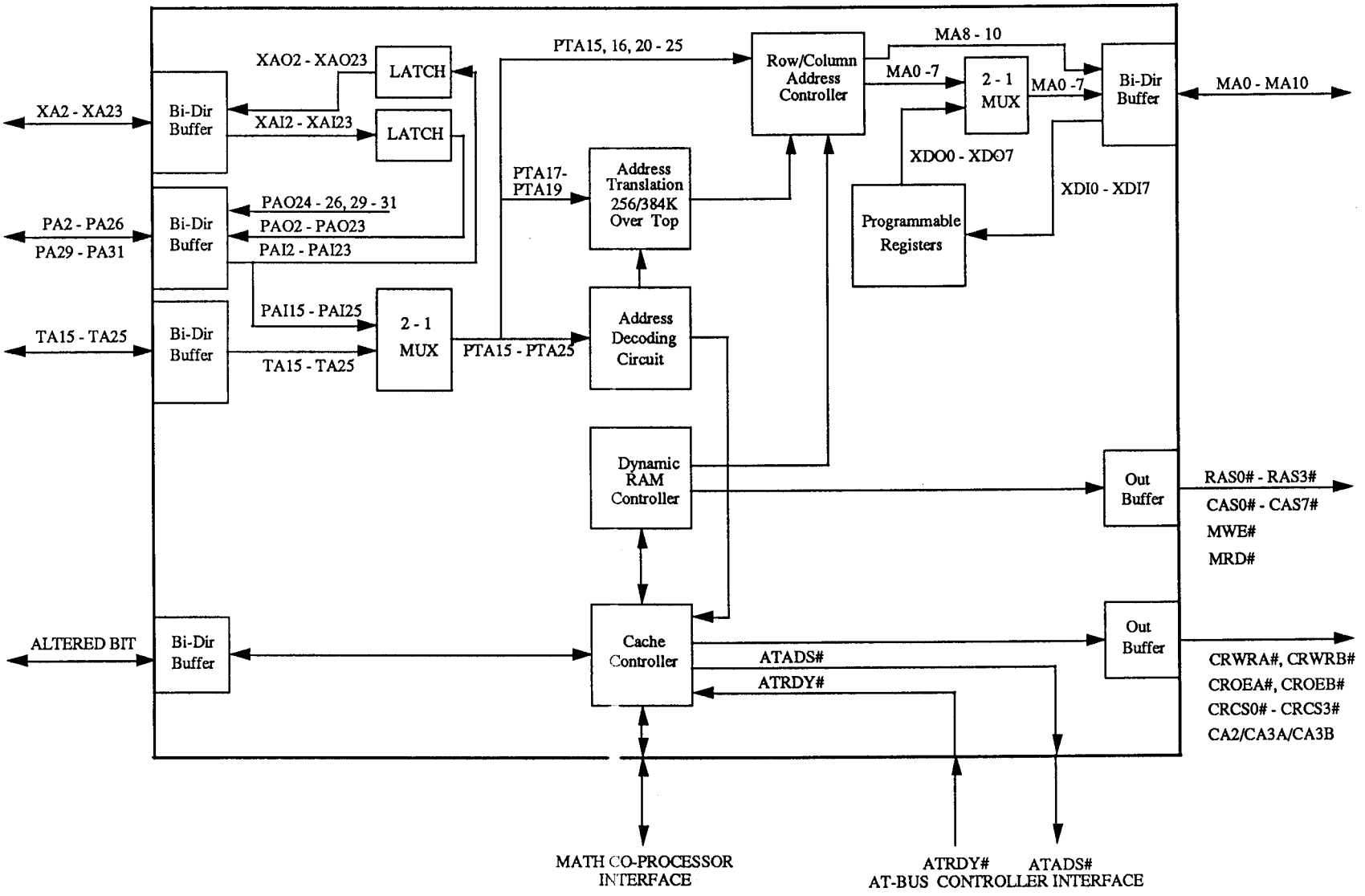
I General Description

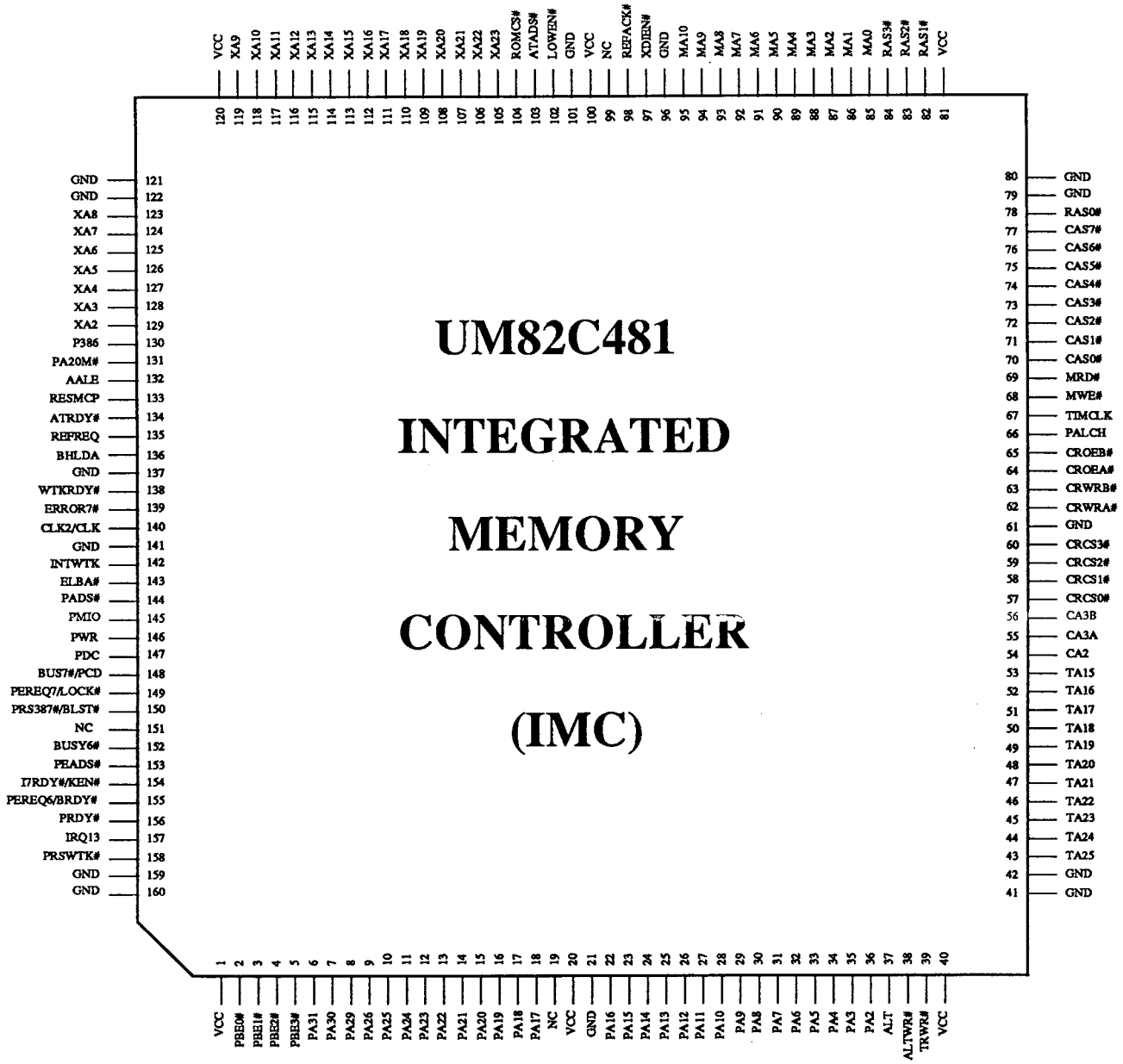
The UM82C481, Integrated Memory Controller (IMC), is part of UMC's high performance 80386/ 80486 PC/AT chip set. It contains sophisticated direct-mapped cache controller with write back operation, and fast page mode DRAM controller. Incorporated with UM82C482, Integrated System Controller (ISC), and UM82C206, Integrated Peripheral Controller (IPC), IMC provides main memory management function for the PC/AT computer system.

II Features

* Built-in cache controller:
  - Direct-mapped organization with write-back operation
  - Cache controller can be enabled/disabled
  - 0 wait state for cache read/write hit if CPU is 80386
  - Programmable 80486 read hit wait state for burst mode
  - Programmable 80486 write hit wait state
  - Programmable cache line size (4/8/16 bytes) if CPU is 80386
  - Flexible cache size: 32/64/128/256/512/1024 KB
  - Support interleaved cache RAM for high speed CPU
  - Hidden DRAM refresh to boost system performance
  - Support Local Bus Access cycles
  - Support three independent non-cacheable regions
  - Video and System BIOS can be cacheable/non-cacheable, write-protected shadow RAM (16 KB resolution for C and D segments)
  - Support fast GATE A20 to optimize OS/2 operations
* Support directly Intel 80387 / Weitek 3167 / Weitek 4167 Floating Point Coprocessors
* Sophisticated DRAM controller:
  - Support Fast/Standard page mode DRAM
  - Support 4 banks of CPU speed DRAM with memory size up to 64 MB
  - Support mixable 256Kx9, 1Mx9, 4Mx9 modules
  - Programmable DRAM wait states
  - Support 256KB or 384KB (A to F segments of first 1MB) relocation to the top of DRAM memory
  - Support Automatic Memory Size Detection
* 1.0μm low-power, high-speed CMOS technology in 160 QFP package



UM82C481 INTEGRATED MEMORY CONTROLLER BLOCK DIAGRAM



Pin Assignment of UM82C481