UMC

T-52-33-90

UM82C8167

Real-Time Clock(RTC)

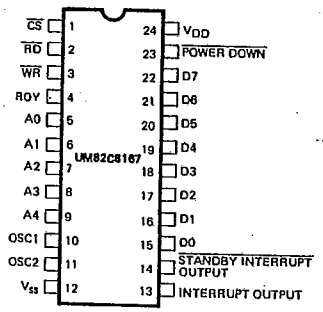
Features

- Microprocessor compatible (8-bit data bus)
- Milliseconds through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- Single +5V power supply
- POWER DOWN input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32,768 Hz crystal oscillator
- Four-year calendar (no leap year)
- 24-hour clock
- 24 pin dual-in-line package

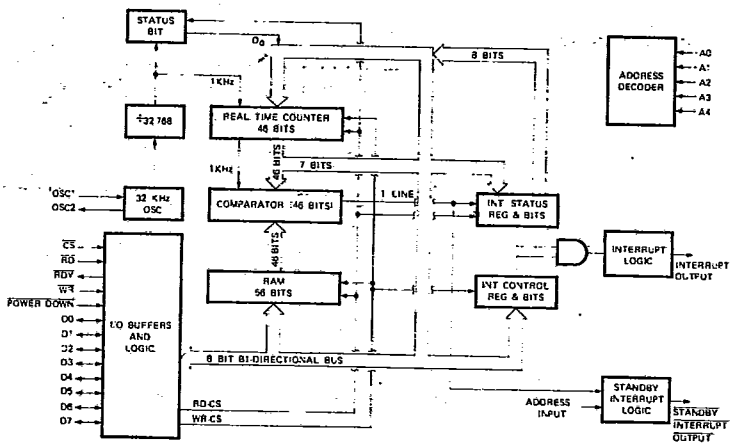
General Description

The UM82C8167 is a Si-gate CMOS LSI used as a real time clock in microprocessor systems. This product includes an addressable real time counter, 56 bits of static RAM and two interrupt outputs. User can disable the chip from the rest of the system for standby low power operation by use of a POWER DOWN input. With an on chip oscillator circuit, it can generate the 32,768 Hz time base.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Voltage at All Inputs and Outputs
. . . . . V_{DD} +0.3 to V_{SS} −0.3
Operating Temperature. . . . . −25°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
$V_{DD} - V_{SS}$ 6V

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Electrical Characteristics

(T_A = −25°C to +85°C, V_{SS} = 0V)

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage V_{DD} V_{DD} (Note 1)	 Outputs Enabled Power Down Mode	 4.0 2.0		 5.5 5.5	 V V
Supply Current I_{DD}, Static I_{DD}, Dynamic I_{DD}, Dynamic	 Outputs TRI-STATE, f_{IN} = DC, V_{DD} = 5.5V Outputs TRI-STATE, f_{IN} = 32 KHz, V_{DD} = 5.5V $V_{IH} \geq V_{DD} - 0.3V$, $V_{IL} \leq V_{SS} + 0.3V$ Outputs TRI-STATE, f_{IN} = 32 KHz V_{DD} = 5.5V, V_{IH} = 2.0V, V_{IL} = 0.8V			 10 20 5	 µA µA mA
Input Voltage V_{IL} Logical Low V_{IH} Logical High		 0.0 2.0		 0.8 V_{DD}	 V V
I_L Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{DD}$	−1		1	µA
Output Voltage V_{OL} Logical Low V_{OH} Logical High TRI-STATE®	(I/O and Interrupt Output) V_{DD} = 4.75V, I_{OL} = 1.6mA V_{DD} = 4.75V, I_{OH} = −400µA, I_{OH} = −10µA V_{OUT} = 0V, V_{OUT} = V_{DD}	 2.4 0.8 V_{DD}		 0.4 −1 1	 V V V µA µA
Output Impedance Logical Low, Sink Logical High, Leakage	(Ready and Standby Interrupt Output) V_{DD} = 4.75V, I_{OL} = 1.6mA $V_{OUT} \leq V_{DD}$			 0.4 10	 V µA

Note 1: To insure that no illegal data is read from or written into the chip during power up, the power down input should be enabled only after all other lines (Read, Write, Chip Select, and Data Bus) are valid.

I/O And Peripherals

AC Characteristics

Interrupt Timing

(0°C ≤ T_A ≤ 70°C, 4.5V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0V)

Symbol	Parameter	Min.	Max.	Units
t_{INTON}	Status Register Clock to INTERRUPT OUTPUT (Pin 13) High (Note 1)		5	µs
t_{SBYON}	Compare Valid to STANDBY INTERRUPT (Pin 14) Low (Note 1)		5	µs
t_{INTOFF}	Trailing Edge of Status Register Read to INTERRUPT OUTPUT Low		5	µs
t_{SBYOFF}	Trailing Edge of Write Cycle 9d0 = 0; Address = 16 H) to STANDBY INTERRUPT Off (high Impedance State)		5	µs

Note 1: The status register clocks are: The corresponding counter's rollover to its reset state or the compare becoming valid. The compare becomes valid 61µs after the 1/10,000 of a second counter is clocked, if the real time counter data matches the RAM data.

Read Cycle Timing

($0°C \leq T_A \leq 70°C$, $4.5V \leq V_{DD} \leq 5.5V$, $V_{SS} = 0V$)

Symbol	Parameter	Min.	Max.	Units
t_{AR}	Address Bus Valid to Read Strobe	100		ns
t_{CSR}	Chip Select to Read Strobe	0		ns
t_{RRY}	Read Strobe to Ready Strobe		150	ns
t_{RYD}	Ready Strobe to Data Valid		800	ns
t_{AD}	Address Bus Valid to Data Valid		1050	ns
t_{RH}	Data Hold Time From Trailing Edge of Read Strobe	0		ns
t_{HZ}	Trailing Edge of Read Strobe to TRI-STATE Mode		250	ns
t_{RYH}	Read Hold Time after Ready Strobe	0		ns
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	50		ns
t_{RYDV}	Rising Edge of Ready to Data Valid		100	ns

Note 2: If $t_{AR} = 0$ and Chip Select, Address Valid or Read are coincident then they must exist for 1050 ns.

Write Cycle Timing

($0°C \leq T_A \leq 70°C$, $4.5V \leq V_{DD} \leq 5.5V$, $V_{SS} = 0V$)

Symbol	Parameter	Min.	Max.	Units
t_{AW}	Address Valid to Write Strobe	100		ns
t_{CSW}	Chip Select to Write Strobe	0		ns
t_{DW}	Data Valid before Write Strobe	100		ns
t_{WRY}	Write Strobe to Ready Strobe		150	ns
t_{RY}	Ready 1 Strobe Width		800	ns
t_{RYH}	Write Hold Time after Ready Strobe	0		ns
t_{WD}	Data Hold Time after Write Strobe	50		ns
t_{WA}	Address Hold Time after Write Strobe	50		ns

Note 3: If data changes while CS and WR are low, then it must remain coincident within 1050 ns after the data change to ensure a valid writing.

Data bus loading is 100 pF.

Ready output loading is 50 pF and 3 kΩ pull-up.

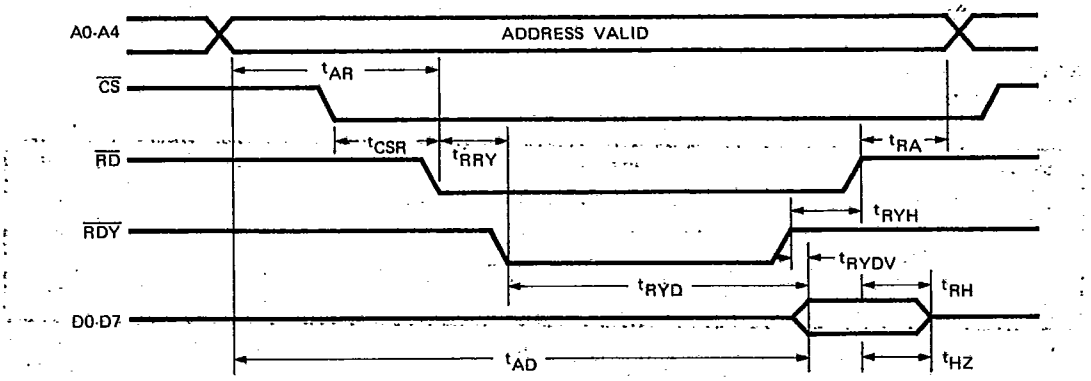
Input and output AC timing levels:

Logical one = 2.0V

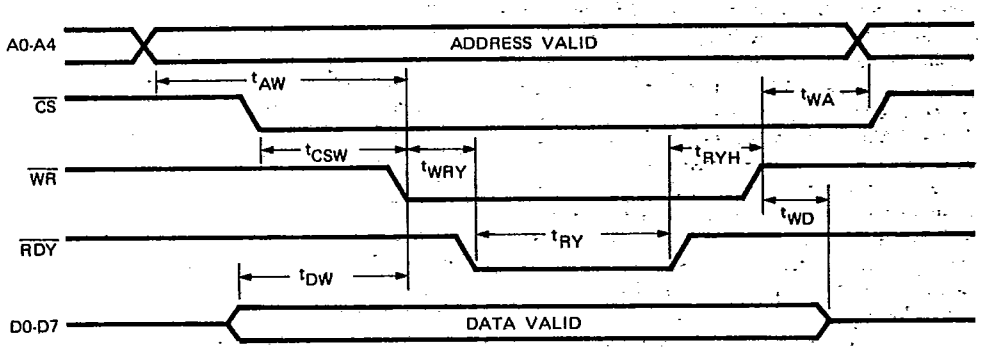
Logical zero = 0.8V

Timing Waveforms

READ CYCLE TIMING



WRITE CYCLE TIMING



Functional Description

Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table 1. Any unused bits are held at a logical zero and ignored during a write. An unused bit is any bit not necessary to provide a full BDC number. For example, tens of hours can not legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table 1 as dashes.

The addressable portion of the counter is from milliseconds to months. The counter itself is a ripple counter. The ripple delay is less than 60μs above 4.0V and 300μs at 2.0V.

Table 1. Real Time Counter Format

Counter Addressed		Units D0	D1	D2	D3	Max. BCD Code	Tens D4	D5	D6	D7	Max. BCD Code
1/10,000 of Seconds	(00_H)	—	—	—	—		D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01_H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02_H)	D0	D1	D2	D3	9	D4	D5	D6	—	5
Minutes	(03_H)	D0	D1	D2	D3	9	D4	D5	D6	—	5
Hours	(04_H)	D0	D1	D2	D3	9	D4	D5	—	—	2
Day of the Week	(05_H)	D0	D1	D2	—	7	—	—	—	—	0
Day of the Month	(06_H)	D0	D1	D2	D3	9	D4	D5	—	—	3
Month	(07_H)	D0	D1	D2	D3	9	D4	—	—	—	1

(—) Indicates unused bits

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit, ten thousandths of seconds and days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones then this RAM location will always compare.

The RAM is formatted the same as the real time counter, 4 bits per digits, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

I/O And Peripherals

Interrupts and Comparator

There are two interrupt outputs. The first and most flexible is the INTERRUPT OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency (Figure 1). Once one or more bits have been set in the interrupt control register, the corresponding counter's rollover to reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupt frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The second interrupt is the STANDBY INTERRUPT (open drain output, active low). This interrupt occurs when enabled and when a RAM/ real time counter comparison occurs. The STANDBY INTERRUPT is enabled by writing a one on the D0 line at address 16H or disabled by writing a zero on the D0 line. This interrupt is not triggered by the edge of the compare signal, but rather by the level. Thus if the compare is enabled when the STANDBY INTERRUPT is enabled, the interrupt will turn on immediately.

The comparator is a cascaded exclusive NOR. Its output is latched 61μs after the rising edge of the 1KHz clock signal (input to the ten thousandth of seconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.0V, the thousandth of seconds counters should not be included in a comparison because of the possibility of having a ripple delay greater than 61μs. (For output timing see interrupt timing.)

Tables 2 and 3 are referred for the address input codes and functions and for the counter and latch reset format.

Power Down Mode

The POWER DOWN input is essentially a second chip select. It disables all inputs and outputs except for the STANDBY INTERRUPT. When this input is at a logical zero, the device will not respond to any external signals. It will, however, maintain time keeping and turn on the STANDBY INTERRUPT if programmed to do so. (The programming must be down before the POWER DOWN input goes to a logical zero.) When switching V_{DD} to the standby or power down mode, the POWER DOWN input should go to a logical zero at least 1μs before V_{DD} is switched. When switching V_{DD} all other inputs must remain between $V_{SS}-0.3V$ and $V_{DD}+0.3V$. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the POWER DOWN input back to a logical one. These precautions are necessary to insure that no data

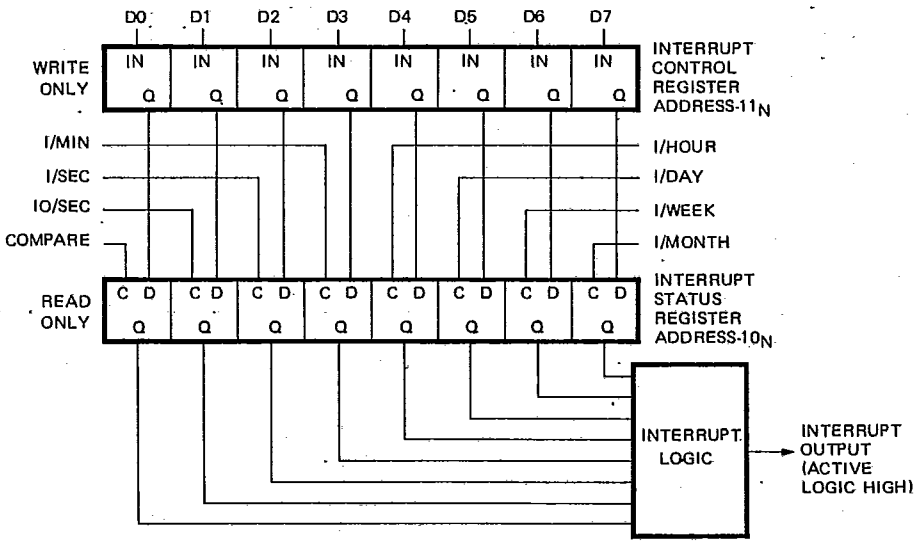


Figure 1. Interrupt Register Format

Table 2. Address Codes and Functions

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter – Thousandths of Seconds
0	0	0	0	1	Counter – Hundredths and Tenths of Seconds
0	0	0	1	0	Counter – Seconds
0	0	0	1	1	Counter – Minutes
0	0	1	0	0	Counter – Hours
0	0	1	0	1	Counter – Day of the Week
0	0	1	1	0	Counter – Day of the Month
0	0	1	1	1	Counter – Months
0	1	0	0	0	Latches – Thousandths of Seconds
0	1	0	0	1	Latches – Hundredths and Tenths of Seconds
0	1	0	1	0	Latches – Seconds
0	1	0	1	1	Latches – Minutes
0	1	1	0	0	Latches – Hours
0	1	1	0	1	Latches – Day of the Week
0	1	1	1	0	Latches – Day of the Month
0	1	1	1	1	Latches – Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counter Reset
1	0	0	1	1	Latch Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	'GO" Command
1	0	1	1	0	Standby Interrupt
1	1	1	1	1	Test Mode

All others unused.

Table 3. Counter and Latch Reset Format

D0	D1	D2	D3	D4	D5	D6	D7	Counter or Latch Reset
1	0	0	0	0	0	0	0	Thousandths of Seconds
0	1	0	0	0	0	0	0	Hundredths and Tenths of Seconds
0	0	1	0	0	0	0	0	Seconds
0	0	0	1	0	0	0	0	Minutes
0	0	0	0	1	0	0	0	Hours
0	0	0	0	0	1	0	0	Day of the Week
0	0	0	0	0	0	1	0	Day of the Month
0	0	0	0	0	0	0	1	Months

For Counter Reset A4–A0 Must be 10010
For Latch Reset A4–A0 Must be 10011

is lost or altered when changing to or from the power down mode.

Counter and RAM Resets; GO Command

The counters and RAM can be reset by writing all 1's (FF) at address 12H or 13H respectively.

A write pulse at address 15H will reset the thousandths, hundredths, tenths, units, and tens of seconds counters. This GO command is used for precise starting of the clock. The data on the data bus is ignored during the writing. If the seconds counter is at a value greater than 39 when the GO is issued, the minute counter will increment; otherwise the minute counter is unaffected. This command is not necessary to start the clock, but merely a convenient way to start precisely at a given minute.

Status Bit

The status bit is provided to inform the user that the clock is in the process of rolling over when a counter is read. The

status bit is set if this 1 KHz clock occurs during or after any counter read. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be reread.

The status bit appears on D0 when address 14H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or after a series of counter reads are done. The trailing edge of the read at address 14H will reset the status bit.

Oscillator

The oscillator is the standard parallel resonant oscillator. Externally, 2 capacitors, a 20M Ohm resistor and the crystal are required. The 20M Ohm resistor is connected between OSC IN and OSC OUT to bias the internal inverter in the linear region. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200K Ohms. The capacitor values should be typically 20 pF – 25 pF. The crystal frequency is 32,768 Hz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input level should be within 0.3V of the supplies.

A ground line or ground plane between pins 9 and 10 may be necessary to prevent interference of the oscillator by the A4 address.

Control Lines

The READ, WRITE, CHIP SELECT signals are active low inputs. The READY signal is an open drain output. At the start of each read or write cycle the READY line (open drain) will pull low and remain low until valid data from a chip read appears on the bus or data on the bus is latched in during a writing. READ and WRITE must be accompanied by a CHIP SELECT (see Timing waveforms for read and write cycle).

During a read or write, address bits must not change while chip select and control strobes are low.

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 KHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at 1 FH.

Typical Application

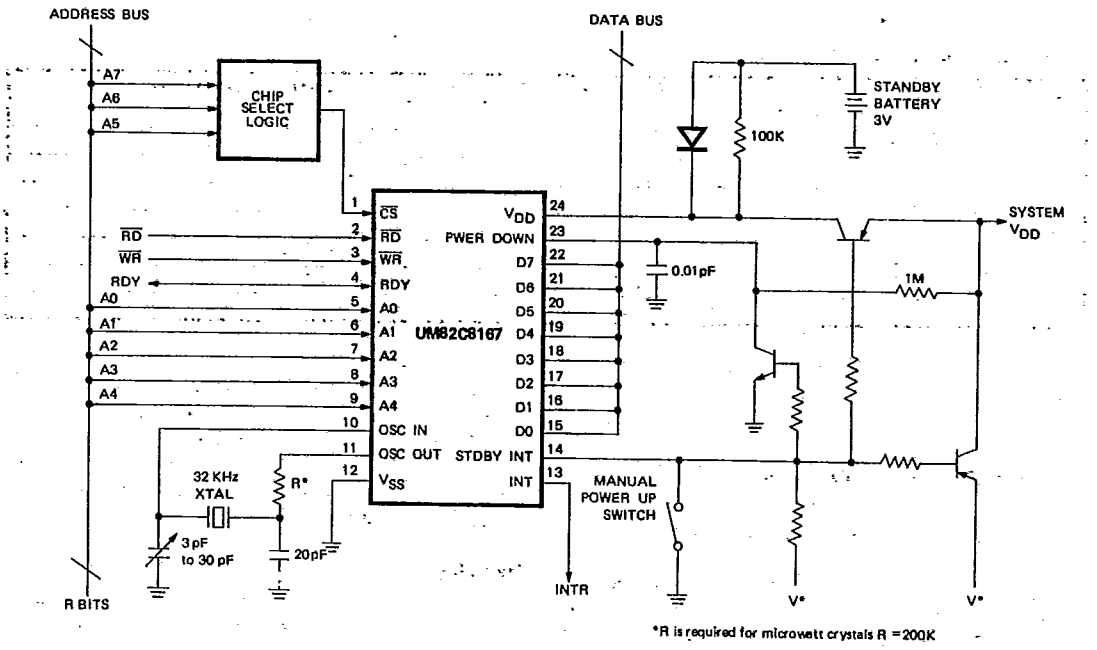


Figure 2. Standby Interrupt is Enable (ON) for Normal Operation and Disabled for Standby Operation