UM8312

Double Row Buffer(DRB)

Features

- Low cost solution to CRT memory contention problem
- Provides enhanced processor throughput for CRT display systems
- Replaces shift registers or several RAM and counter IC's in CRT display system
- Permits display of one data row while next data row is being loaded
- Data may be written into buffer at less than the video painting rate
- Double data row buffer permits second data row to be loaded anytime during the display of the preceding data row
- Permits active video on all scan lines of data row
- Dynamically variable number of characters per data Row—. . . 64, 80, 132, ... up to a maximum of 135
- Cascadable for data rows greater than 135 characters
- Stackable for "Invisible Attributes" or character widths of greater than 8 Bits
- Three-state outputs
- Up to 4 MHz read/write data rate
- Compatible with UM9007 and other CRT controllers
- 28 pin dual-in-line package
- +5 volt only power supply
- TTL compatible

General Description

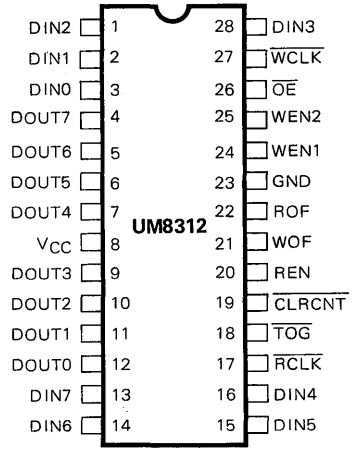
The UM8312 Double Row Buffer (RDB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The UM8312 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

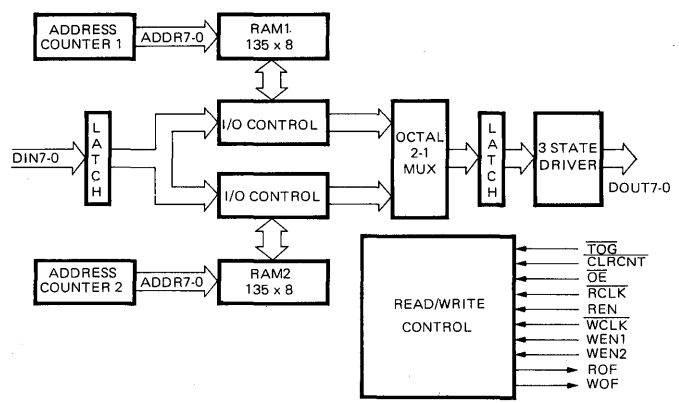
The UM8312 permits the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floopy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.

CRT Controller

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature Range . . . . . 0°C to + 70°C
Storage Temperature Range . . . . . −55°C to + 150°C
Lead Temperature (soldering, 10 sec.) . . . . . +325°C
Positive Voltage on any Pin, with respect to ground . . . . . +8.0V
Negative Voltage on any Pin, with respect to ground . . . . . −0.3V

*Comments

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%)

D.C. CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Conditions
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	excluding $\overline{RCLK}$; $\overline{WCLK}$
High Level V_{IH2}	4.2			V	$\overline{RCLK}$, $\overline{WCLK}$
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	
High Level V_{OH}	2.4			V	
INPUT LEAKAGE CURRENT					
High Leakage I_{LH1}			10	μA	excluding $\overline{OE}$
Low Leakage I_{LL1}			10	μA	excluding WEN1
High Leakage I_{LH2}			400	μA	WEN1
Low Leakage I_{LL2}			400	μA	$\overline{OE}$
INPUT CAPACITANCE					
C_{IN1}		10		pF	excluding $\overline{RCLK}$, $\overline{WCLK}$
C_{IN2}		15		pF	$\overline{RCLK}$, $\overline{WCLK}$
POWER SUPPLY CURRENT					
I_{CC}		100	140	mA	

A.C. CHARACTERISTICS

Parameter	Min.	Typ.	Max.	Units	Conditions
t_{CYW}	300			ns	Write clock period
t_{CYR}	300			ns	Read clock period
t_{CKH}	247		DC	ns	
t_{CKL}	33			ns	
t_{CKR}			10	ns	measured from 10% to 90% points
t_{CKF}			10	ns	measured from 90% to 10% points
t_{DS}	50			ns	referenced to $\overline{WCLK}$
t_{DH}	0			ns	referenced to $\overline{WCLK}$
t_{EN1}[2]	0			ns	
t_{EN2}[2]	100			ns	
t_{ENH}[2]	0			ns	
t_{DV}			175	ns	C_L = 50pF; referenced from $\overline{RCLK}$
t_{DOFF}			175	ns	
t_{DON}			175	ns	
t_{OF}[3]			175	ns	C_L = 30pF
t_{CS}	100			ns	
t_{CH}	0			ns	
t_{WT}[4]		$1t_{CYW}$			

1 – Reference points for all AC parameters are 2.4V high and 0.4V low.
2 – For REN, referenced from $\overline{RCLK}$; for WEN1 or $\overline{WEN2}$ referenced to $\overline{WCLK}$.
3 – For ROF, referenced from $\overline{RCLK}$; for WOF referenced from $\overline{WCLK}$.
4 – At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TNG}$ (whichever occurs last) and WEN (= WEN1-WEN2).

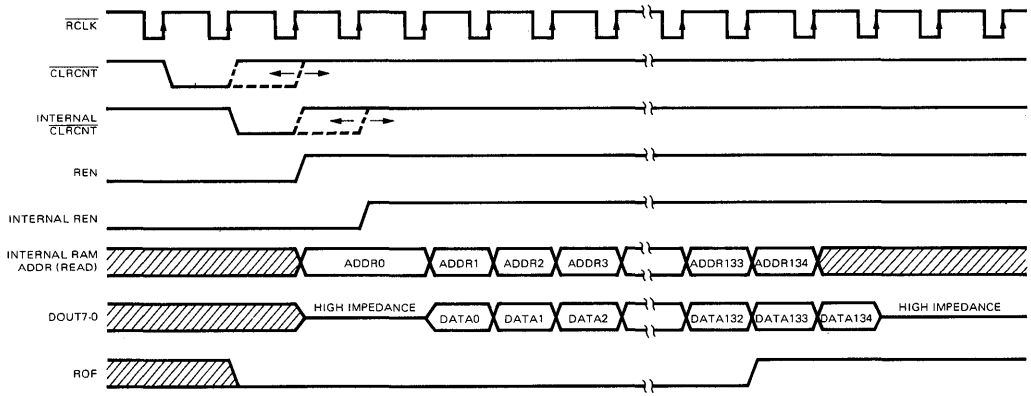


Figure 1. UM8312 Double Row Buffer Read Timing

Pin Description

Pin No.	Name	Symbol	Functions
3-0, 28, 16-13	Data inputs	DIN0-DIN7	DIN DIN7 are the data inputs from the system memory.
12-9, 7-4	Data outputs	DOUT0-DOUT7	DOUT0-DOUT7 are the data outputs from the UM8312 internal data output latch. Valid information will appear on DOUT0-DOUT7 two RCLK periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
17	Read Clock	RCLK	RCLK increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailling edge. See Figure 1.
18	Toggle Signal	TOG	TOG alternates the function of each buffer between read and write. TOG normally occurs at every data row bundary. Switching of the buffers occurs when both TOG and CLRCNT are low. See Figure 2.
19	Clear Counter	CLRCNT	Clear Counter clears the current "read" address counter at the next RCLK positive edge. CLRCNT is normally asserted low at the beginning of each horizontal retrace interval. CLRCNT clears the current "write" address counter when the TOG is active.
20	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when Read Clock is active.
21	Write Overflow	WOF	WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second UM8312 for cascaded operation where data row lengths of greater than 135 characters are desired. See Figure 3.
22	Read Overflow	ROF	The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second UM8312 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of RCLK after ROF goes high. See Figure 3.
24, 25	Write Enable	WEN1, WEN2	WEN allows input data to be written into the selected "write" buffer during WCLK active. Both WEN1 and WEN2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open.
26	Output Enable	OE	When the OE input is low the data outputs DOUT0-DOUT7 are enabled. When OE is high, DOUT0-DOUT7 present a high impedance state. OE has an internal pulldown resistor allowing it to assume a low if pin 26 is left open.
27	Write Clock	WCLK	WCLK clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high.
8	Power Supply	V_{CC}	+5 Volt supply
23	Ground	GND	Ground

Operational Description

Block diagram illustrates the internal architecture of the UM8312. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When both Write Enable (WEN1, WEN2) signals go high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal ($\overline{TOG}$) will go low. When Clear Counter ($\overline{CLRCNT}$) goes low, the next Read Clock ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock ($\overline{RELK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the UM8312 and the internal "read" address counter is cleared independent of the $\overline{CLRCNT}$ pulse width. The $\overline{CLRCNT}$ input may be tied to the REN input for proper operation.

Figures 1 and 2 illustrate the functional timing for reading and writing the UM8312. It is possible to cascade two or more UM8312's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 3 illustrates two UM8312's cascaded together.

The UM8312 is compatible with the UM9007 video processor and controller (VPAC^{TM}) and the UM9021 video attributes controller (VAC). A typical video configuration employing the three parts is illustrate in figure 4.

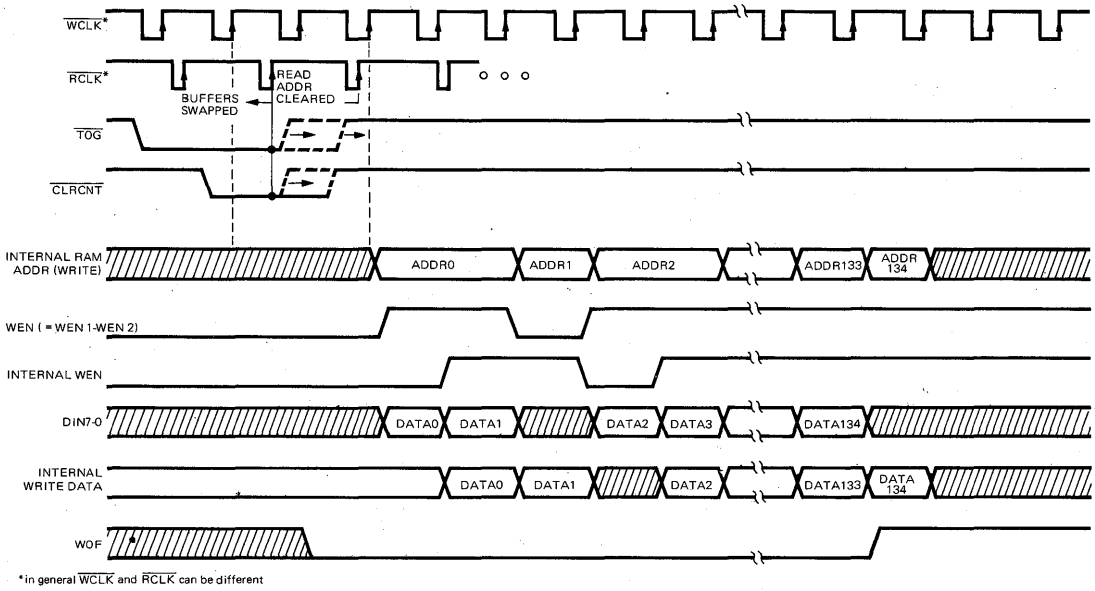


Figure 2. UM8312 Double Row Buffer Write Timing

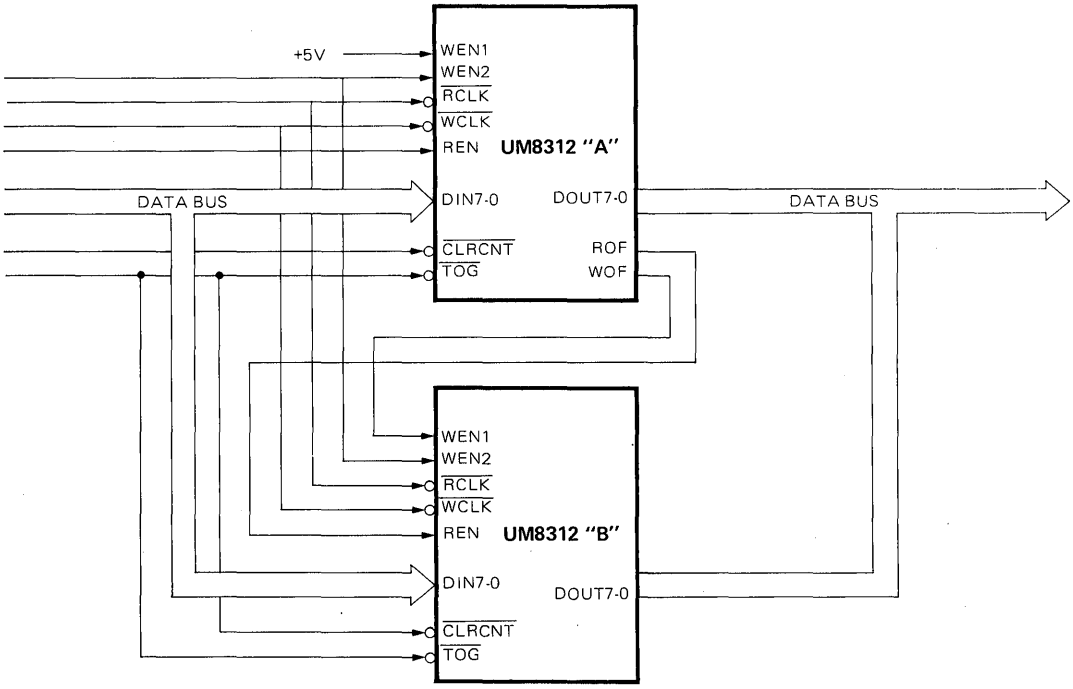


Figure 3. UM8312 Cascaded Configuration For Data Row Lengths Up To 270 Characters

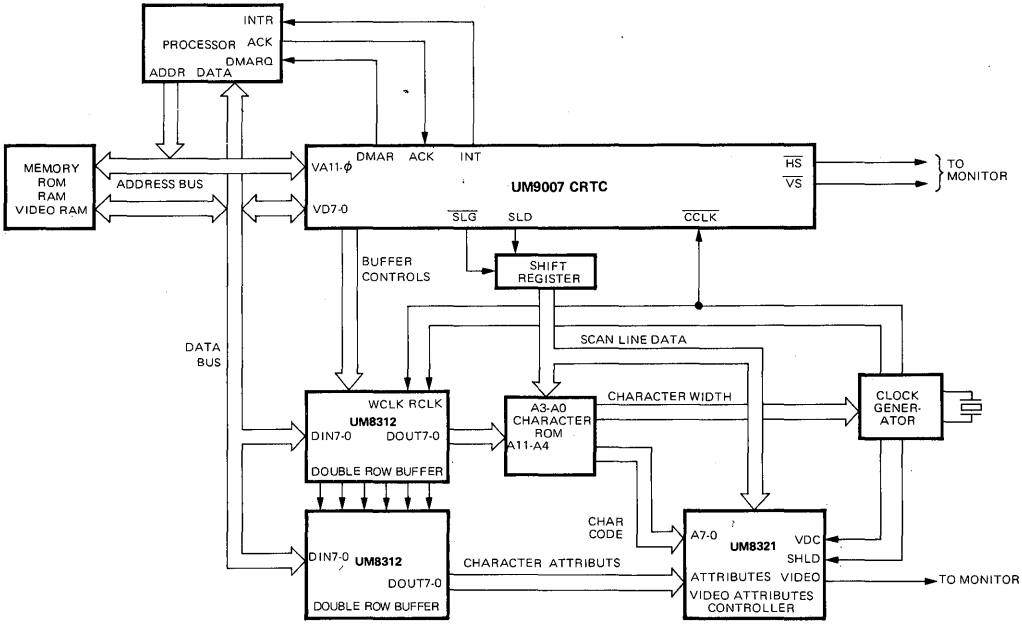


Figure 4. UM8312 Configured With The UM9007 CRTC And The UM8321 CRT VAC

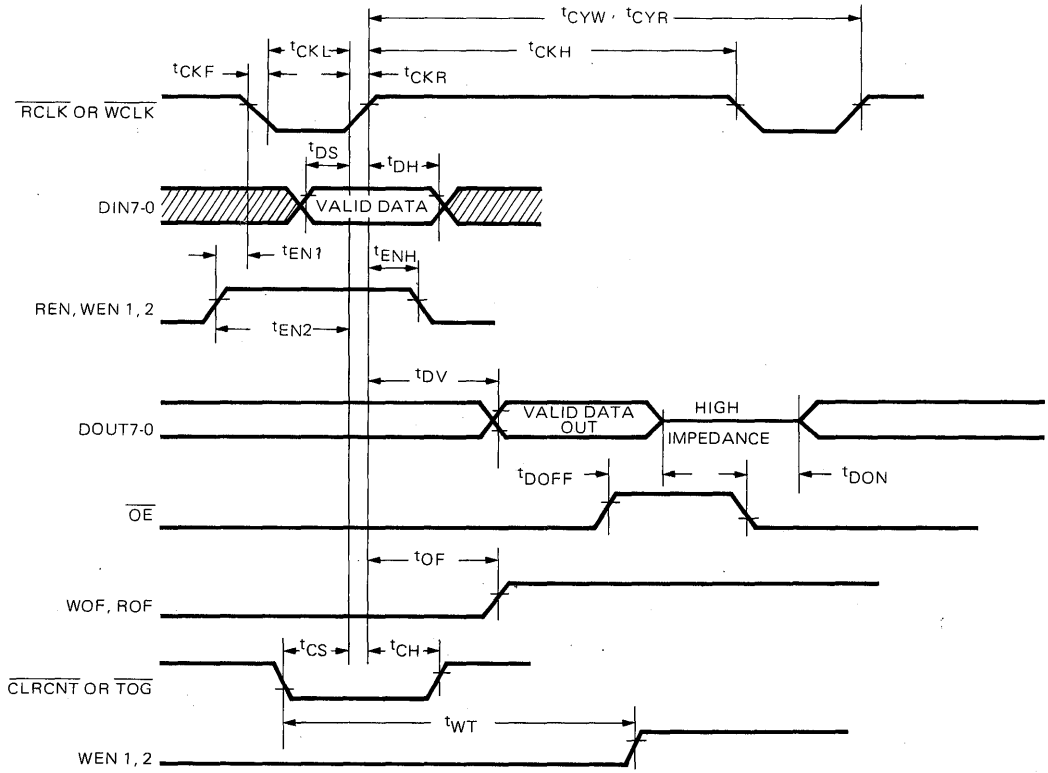


Figure 5. UM8312 I/O Timing