UM8329/8329T/8329B/8329BT

Floppy Disk Interface Circuit

Features

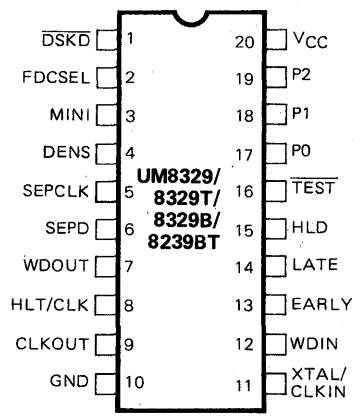
- Digital date separator
  - Performs complete data separation function for floppy disk drives
  - Separates FM and MFM encoded data
  - No critical adjustments necessary
  - 5¼" and 8" compatible
- Variable write precompensation
- Internal crystal oscillator circuit
- Track-selectable write precompensation
- Retriggerable head-load timer
- Compatible with the FDC 179X, 8272A, and other standard floppy disk controllers
- SAN-III MOS N-CHANNEL TECHNOLOGY
- Single + 5 volt supply
- TTL compatible

General Description

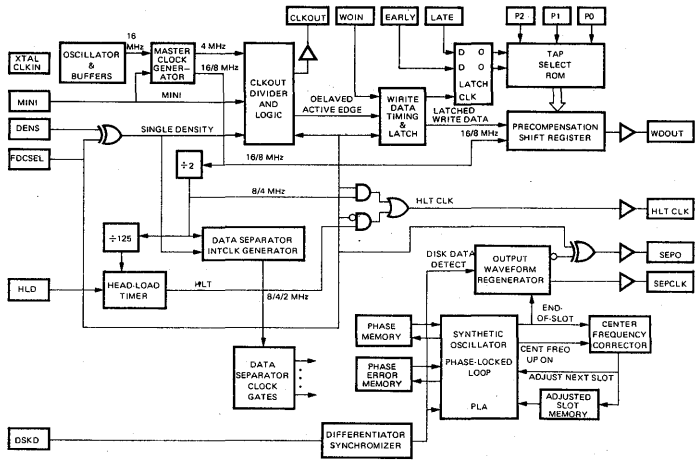
The UM8329/B is an MOS integrated circuit designed to complement either the 179X or 8272A (765A) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 8272A type of controller. The UM8329/B provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The UM8329/B operates from a +5V supply and simply requires that a 16 or 8 MHz crystal or TTL-level clock be connected to the XTAL/CLKIN pin. All inputs and outputs are TTL compatible.

The UM8329 is available in four versions: The UM8329/T are intended for 5¼" disks and the UM8329B/T for 5¼" and 8" disks. The UM8329/B have an internal crystal oscillator circuit; the UM8329T/BT require an external clock.

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −55°C to +150°C
Positive Voltage on any I/O Pin, with respect to ground . . . . . +7.0V
Negative Voltage on any I/O Pin, with respect to ground . . . . . −0.3V
Power Dissipation 0.75W

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is siwtched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

Comments*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

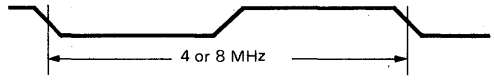
Parameter	Min.	Typ.	Max.	Units	Conditions
D.C. Characteristics					
INPUT VOLTAGE					
Low Level V_{IL}	−0.3		0.8	V	Except XTAL/CLKIN
High Level V_{IH}	2.0		(V_{CC})	V	
XTAL/CLKIN INPUT VOLTAGE					
Low Level	−0.3		0.8	V	
High Level	2.4		(V_{CC})	V	
OUTPUT VOLTAGE					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA except HLT/CLK
					I_{OL} = 0.4 mA, HLT/CLK only
High Level V_{OH}	2.4			V	I_{OH} = −100 μA except HLT/CLK
					I_{OH} = −400 μA, HLT/CLK only
POWER SUPPLY CURRENT					
I_{CC}			100	mA	
INPUT LEAKAGE CURREN					
I_{IL}			10	μA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE			10	pF	Except CLKIN
C_{IN}			25	pF	CLKIN only

Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

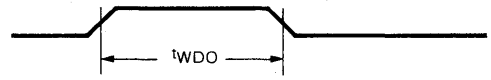
Parameter	Min.	Typ.	Max.	Units	Conditions
A.C. Characteristics	All times assume CLKIN = 16 MHz unless otherwise specified)				
XTAL/CLKIN Frequency	3.95	16	16.2	MHz	UM8329B
	3.95	8	8.1	MHz	UM8329T
XTAL/CLKIN Duty Cycle	25		75	%	
t_{CIKOH}	465	500	515	ns	FDCSEL = low; MINI = high.
	215	250	265	ns	FDCSEL = low; MINI = low.
	90	125	140	ns	FDCSEL = high.
t_{WdO}	280	312.5	350	ns	Time Doubles with MINI = 1
t_d	50		400	ns	
t_{dNEC}	0		400	ns	
t_{WdE}	500	562.5	625	ns	9 clock times ± 1 clock time
t_{WdN}					See fig. 2
t_{WdL}					See fig. 2
t_S	1.0			μs	

A.C. Timing Characteristics

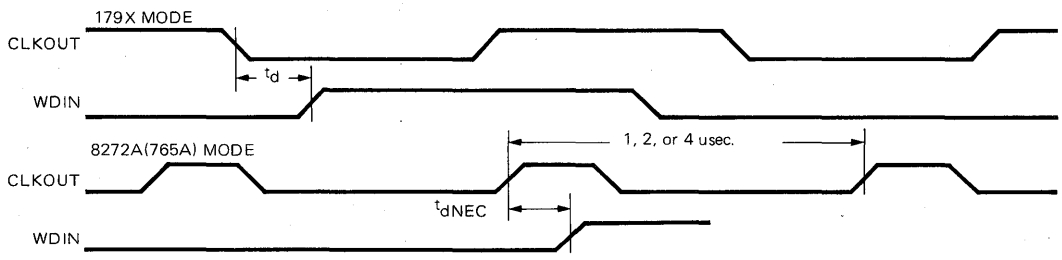
HLT/CLK (8272A MODE)



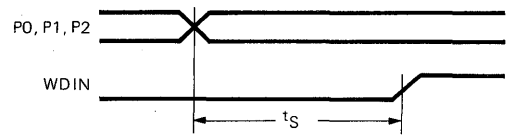
WDOUT PULSE WIDTH



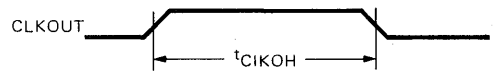
CLKOUT VS. WDIN TIMING



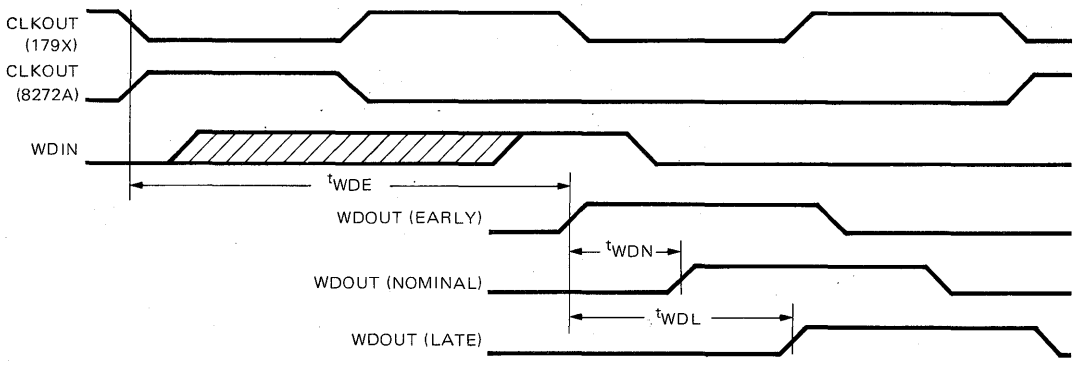
SET-UP TIME P0, P1 AND P2 TO WDIN



CLKOUT



PRECOMPENSATION

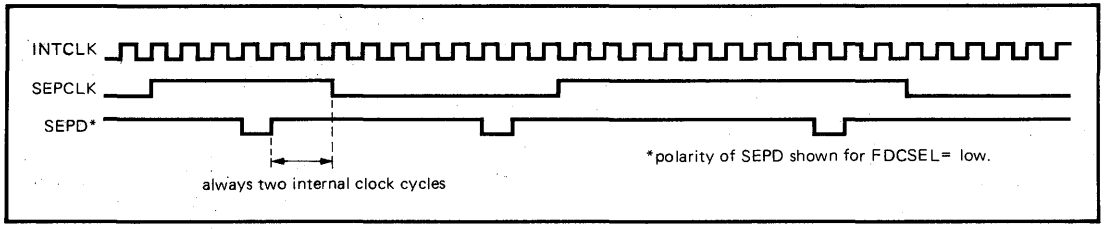


Ref. to Fig. 2 for t_p (precompensation) value

Pin Description

Pin No.	Symbol	I/O	Descriptions
1	$\overline{DSKD}$	I	This input is the raw read data received from the drive. (This input is active low.)
2	FDCSEL	I	This input signal, when low programs the UM8329/B for a 179X type of LSI controller. When FDCSEL is high, the UM8329/B is programmed for a 8272A (765A) type of controller. (See fig. 4.)
3	MINI	I	The state of this input determines whether the UM8329/B is configured to support 8" or 5¼" floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 8272A mode). (See figs. 2, 3, and 4.)
4	DENS	I	The state of this input determines whether the UM8329/B is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 8272A mode. (See figs. 2, 3, and 4.)
5	SEPCLK	O	A square-wave window clock signal output derived from the $\overline{DSKD}$ input.
6	SEPD	O	This output is the regenerated data pulse derived from the raw data input ($\overline{DSKD}$). This signal may be either active low or active high as determined by FDCSEL (pin 2).
7	WDOUT	O	The precompensated WRITE DATA stream to the drive.
8	HLT/CLK	O	When in the 8272A mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See fig. 3.)
9	CLKOUT	O	This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS, and FDCSEL input pins. (See fig. 3.)
10	GND		Ground
11	XTAL/CLKIN	I	This input is for direct connection to a 16 MHz or 8 MHz crystal UM8329/B only). The other pin of the crystal is grounded. XTAL/CLKIN may alternatively be connected to a single-phase TTL-level clock. The UM8329T and BT require an external TTL-level clock.
12	WDIN	I	The write data stream from the floppy disk controller.
13	EARLY	I	When this input is high, the current WRITE DATA pulse will be written early to the disk.
14	LATE	I	When this input is high, the current WRITE DATA pulse will be written late to the disk. When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position.
15	HLD	I	This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state of the MINI output. (See fig. 3.)
16	$\overline{TEST}$	I	This input (when low) decreases the head-load time delay and initializess the data separator. This pin is for test purposes only. This input has an internal pull-up resistor and should be tied high or disconnected for normal operation.
17	P0	I	P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.)
18	P1	I	
19	P2	I	
20	V_{CC}		+5 VOLT SUPPLY

Operational Description



DATA SEPARATOR

The XTAL/CLKIN input clock is internally divided by the UM8329/B to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

The UM8329/B detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.

Inputs			f(XTAL/CLKIN) /f(INTCLK)
FDCSEL	DENS	MINI	
0	0	0	2
0	0	1	4
0	1	0	4
0	1	1	8
1	0	0	4
1	0	1	8
1	1	0	2
1	1	1	4

Fig. 1.

PRECOMPENSATION

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the UM8329/B as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the driver and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

MINI	P2	P1	P0	Precomp Value
0	0	0	0	0 ns
0	0	0	1	62.5 ns
0	0	1	0	125 ns
0	0	1	1	187.5 ns
0	1	0	0	250 ns
0	1	0	1	250 ns
0	1	1	0	312.5 ns
0	1	1	1	312.5 ns
1	0	0	0	0 ns
1	0	0	1	125 ns
1	0	1	0	250 ns
1	0	1	1	375 ns
1	1	0	0	500 ns
1	1	0	1	500 ns
1	1	1	0	625 ns
1	1	1	1	625 ns

Note: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

Fig. 2 Write precompensation value selection

HEAD LOAD TIMER

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 8272A mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the goes high before starting a read or write operation UM8329/B.

Inputs			Outputs	
FDCSEL	DENS	MINI	CLKOUT	HLT/CLK
0	0	0	2 MHz	40 ms*
0	0	1	1 MHz	80 ms*
0	1	0	2 MHz	40 ms*
0	1	1	1 MHz	80 ms*
1	0	0	500 KHz	8 MHz
1	0	1	250 KHz	4 MHz
1	1	0	1 MHz	8 MHz
1	1	1	500 KHz	4 MHz

Note: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

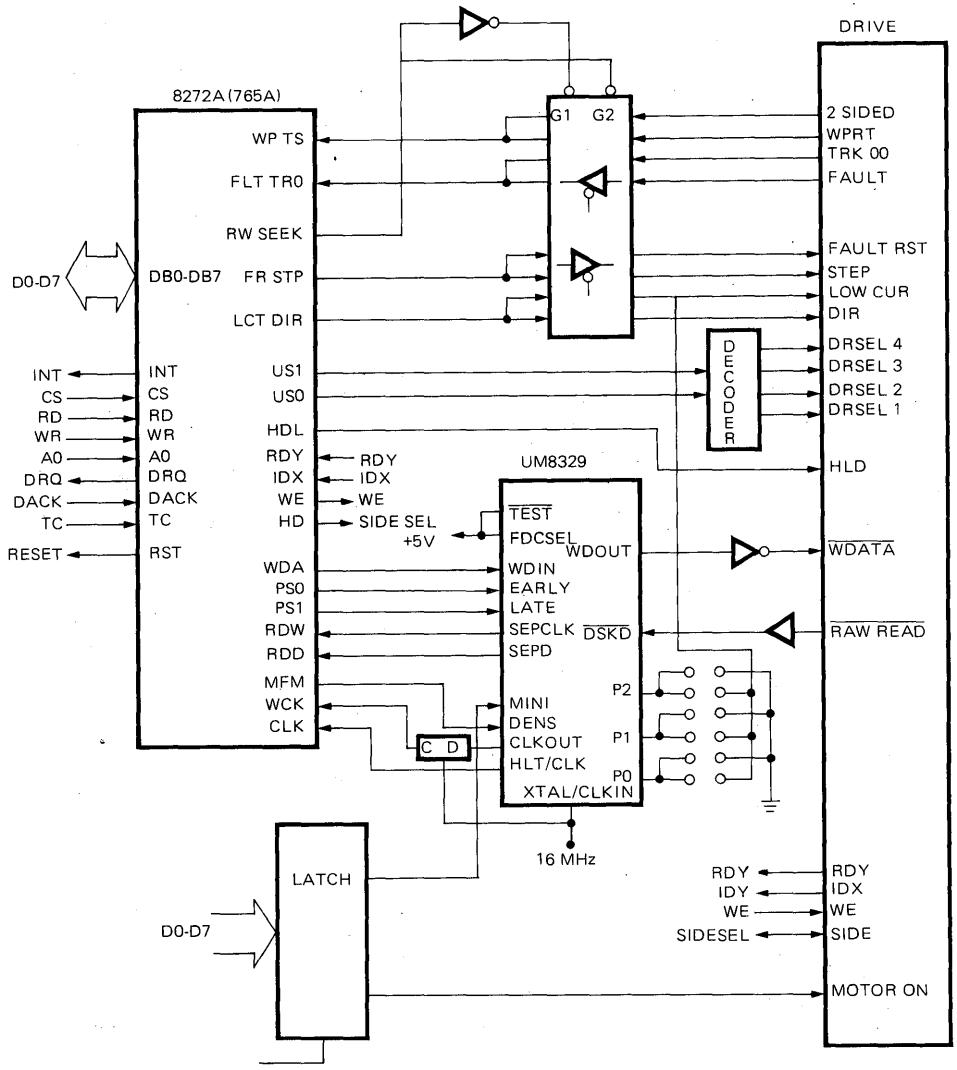
*May be mask programmed at factory to any value from 1 to 512 min is 15.625 μs increments (MINI low) or 1 to 1024 ms in 31.25 μs increments (MINI high).

Fig. 3. Clock and head load time delay selection

Inputs			Floppy Disk Drive Type	Floppy Disk Drive Density	Floppy Disk Controller Type
FDCSEL	DENS	MINI			
0	0	0	8" Drive	Double	179X
0	0	1	5¼" Drive	Double	179X
0	1	0	8" Drive	Single	179X
0	1	1	5¼" Drive	Single	179X
1	0	0	8" Drive	Single	8272A (765A)
1	0	1	5¼" Drive	Single	8272A (765A)
1	1	0	8" Drive	Double	8272A (765A)
1	1	1	5¼" Drive	Double	8272A (765A)

Fig. 4 Floppy disk drive and controller selection

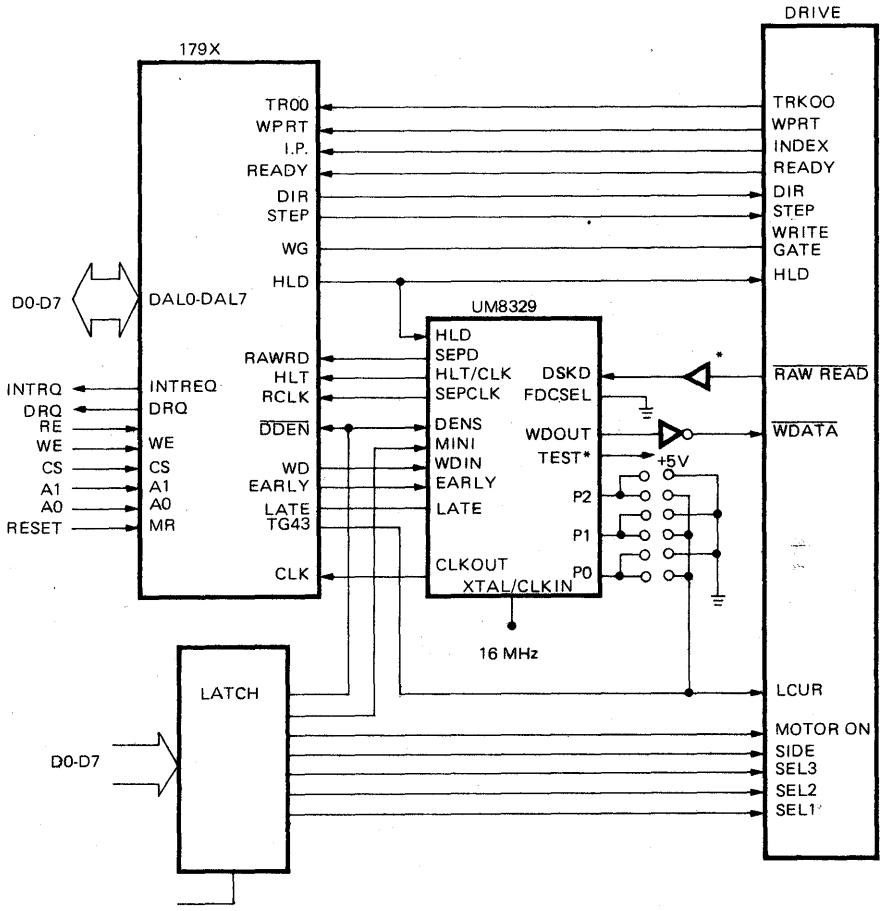
Typical System Implementation – 8272A(765A) FDC



* The UM8329T/BT, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (noninverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the UM9229/B.

Typical System Implementation – 179X FDC



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Ordering Information

Part Number	Operation Type	Frequency Option	Package Type
UM8329	CLK/XTAL	8 MHZ	Plastic
UM8329B	CLK/XTAL	16 MHZ	Plastic
UM8329T	CLK	8 MHZ	Plastic
UM8329BT	CLK	16 MHZ	Plastic