UM9007

ADVANCED PRODUCT DESCRIPTION

CRT Controller

Features

- Fully programmable display format
- Programmable monitor sync. format
- Direct outputs to CRT monitor
- Binary, row-table driven or sequential video addressing modes
- Programmable status row position and address registers
- Bidirectional partial or full page smooth scroll
- Attribute assemble mode
- Double height, double width data row mode
- Programmable DMA burst mode
- Configurable with a variety of memory contention arrangements
- Light pen register
- Maskable processor interrupt line
- Three-state video memory address bus
- Partial or full page blank capability
- Two interlace modes: enhanced video and alternate scan line
- Programmable for horizontal split screen applications
- Graphics compatible
- VT-100 compatible
- RS-170 Interlaced composite sync. available

General Description

The CRTC UM9007 is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the UM9007 provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The UM9007 works with a variety of memory contention schemes including operation with a Single Row Buffer, a Double Row Buffer such as the UM8312, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and CRTC status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".