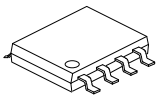
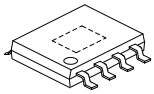
UMD9137 **Preliminary** ***CMOS IC***

LOW-VOLTAGE H-BRIDGE DRIVER



SOP-8



HSOP-8

DFN2020-8

■ DESCRIPTION

The UTC **UMD9137** can supply up to 1.8 A of output current. It operates on a motor power supply voltage from 0 to 11 V, and a device power supply voltage of 1.8 V to 7.0 V.

The UTC **UMD9137** provides an integrated motor driver solution. The device can drive one DC motor or other devices like solenoids. The output driver block consists of N-channel power MOSFET's configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The UTC **UMD9137** has a PWM (IN1/IN2) input interface.Both interfaces are compatible with industry-standard devices.

Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout, and overtemperature.

■ FEATURES

* PWM Interface, IN1/IN2
* Low-power Sleep Mode With 120-nA Maximum Sleep Current
  – nSLEEP pin
* 1.8-A Maximum Drive Current
* Separate Motor and Logic Supply Pins:
  – Motor V_M: 0~11 V
  – Logic V_{CC}: 1.8~7 V
* Protection Features
  – V_{CC} Undervoltage Lockout
  – Overcurrent Protection
* Thermal Shutdown

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UMD9137L-S08-R	UMD9137G-S08-R	SOP-8	Tape Reel
UMD9137L-SH2-R	UMD9137G-SH2-R	HSOP-8	Tape Reel
UMD9137L-K08-2020-R	UMD9137G-K08-2020-R	DFN2020-8	Tape Reel

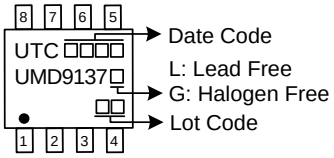
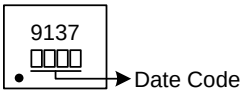
UMD9137G-S08-R

(1)Packing Type — (1) R: Tape Reel

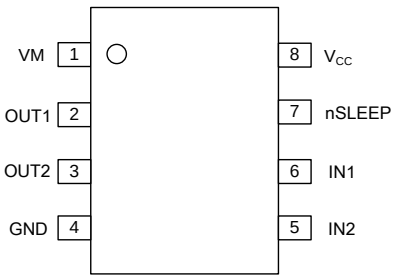
(2)Package Type — (2) S08: SOP-8, SH2: HSOP-8, K08-2020: DFN2020-8

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

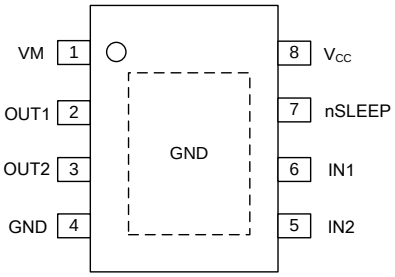
■ MARKING

SOP-8 / HSOP-8	DFN2020-8
	

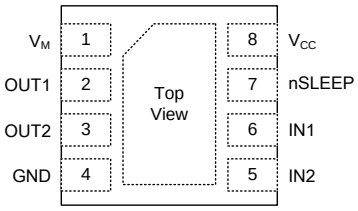
■ PIN CONFIGURATION



SOP-8



HSOP-8

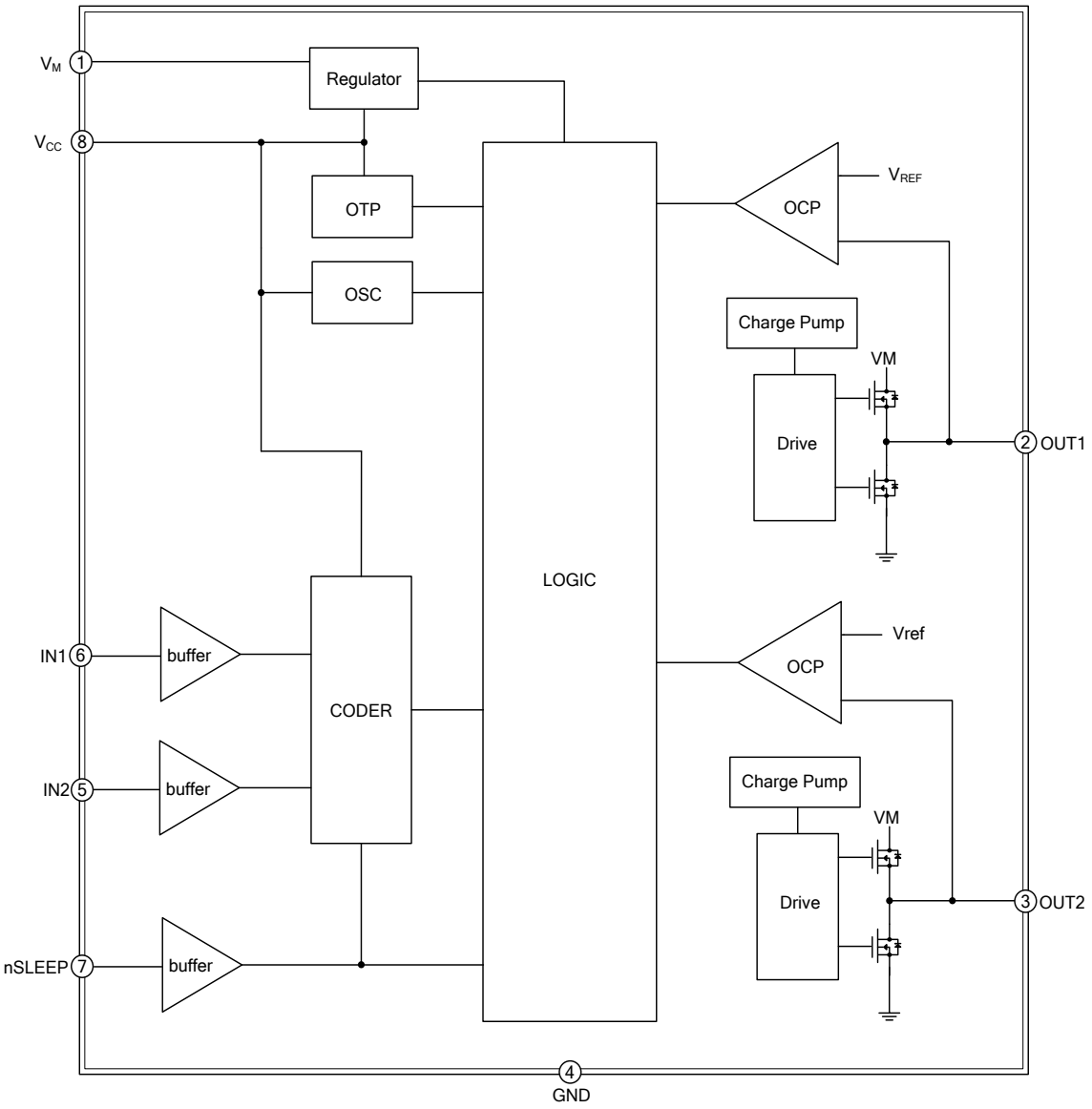


DFN2020-8

■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_M	Motor power supply
2	OUT1	Motor output Connect to motor winding
3	OUT2	
4	GND	Device ground
5	IN2	PHASE input
6	IN1	
7	nSLEEP	Sleep mode input
8	V_{CC}	Logic Power supply

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Motor Power Supply Voltage Range	V_M	12	V
Logic Power Supply Voltage Range	V_{CC}	7	V
Control Pin Voltage Range	IN1, IN2, nSLEEP	7	V
Peak Drive Current	OUT1, OUT2	Internally limited	A
Operating Virtual Junction Temperature Range	T_J	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

(T_A = 25°C, over recommended operating conditions unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_M, V_{CC})						
V_M Operating Voltage	V_M				11	V
V_M Operating Supply Current	I_{VM}	V_M =5V, V_{CC} =3V, No PWM		40		uA
		V_M =5V, V_{CC} =3V, 50kHz PWM		0.8		mA
V_M Sleep Mode Supply Current	I_{VMQ}	V_M =5V, V_{CC} =3V, nSLEEP=0		30		nA
V_{CC} Operating Voltage	V_{CC}				7	V
V_{CC} Operating Supply Current	I_{CC}	V_M =5V, V_{CC} =3V, No PWM		300		uA
		V_M =5V, V_{CC} =3V, 50kHz PWM		0.7		mA
V_{CC} Sleep Mode Supply Current	I_{VCQ}	V_M =5V, V_{CC} =3V, nSLEEP=0		5		nA
CONTROL INPUTS (IN1/PH, IN2/EN, nSLEEP)						
Input Logic Low Voltage	V_{IL}			0.38×V_{CC}		V
Input Logic High Voltage	V_{IH}			0.46×V_{CC}		V
Input Logic Hysteresis	V_{HYS}			0.08×V_{CC}		mV
Input Logic Low Current	I_{IL}	V_{IN}=0V	-5		5	uA
Input Logic High Current	I_{IH}	V_{IN}=3.3V			50	uA
Pulldown Resistance	R_{PD}			100		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
HS+LS FET On-Resistance	$R_{DS(ON)}$	V_M=5V, V_{CC}=3V, I_O=800mA, T_J=25℃		280		mΩ
Off-state leakage current	I_{OFF}	V_{OUT}=0	-200		200	nA
PROTECTION CIRCUITS						
V_{CC} Undervoltage Lockout	V_{UVLO}	V_{CC} falling			1.7	V
		V_{CC} rising			1.8	V
Protection Trip Level	I_{OCP}		1.9		3.5	A
Overcurrent Deglitch Time	t_{DEG}			1		us
Overcurrent Retry Time	t_{RETRY}			1		ms
Thermal Shutdown Temperature	T_{TSD}	Die temperature T_J		160		°C

■ TIMING REQUIREMENTS (T_A=25°C, V_M=5 V, V_{CC}=3 V, R_L=20 Ω)

PARMMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t1	Output enable time		300		ns
t2	Output disable time		300		ns
t3	Delay time, INx high to OUTx high		160		ns
t4	Delay time, INx low to OUTx low		160		ns
t5	Output rise time		188		ns
t6	Output fall time		188		ns
t_{wake}	Wake time, nSLEEP rising dege to part active		30		us

■ PRINCIPLE OF OPERATION

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

The UTC **UMD9137** is a H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using either a PWM interface (IN1/IN2) on the UTC **UMD9137** .

In addition, the UTC **UMD9137** adds protection features above traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

■ DESIGN REQUIREMENTS

Table 1 shows required parameters for a typical usage case.

Table 1.System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor Supply Voltage	V_M	9V
Logic Supply Voltage	V_{CC}	3.3 V
Target RMS Current	I_{OUT}	0.8 A

■ FEATURE DESCRIPTION

Bridge Control

Table 2 shows the logic for the **UMD9137** device:

Table 2.System Design Requirements

nSLEEP	IN1	IN2	OUT1	OUT2	Function（DC Motor）
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the UTC **UMD9137** enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

Power Supplies

V_{CC} and V_M may be applied and removed in any order. When V_{CC} is removed, the device will enter a low power state and draw very little current from V_M.

The V_M voltage supply does not have any under voltage lockout protection (UVLO), so as long as V_{CC} > 1.8 V; the internal device logic will remain active. This means that the V_M pin voltage may drop to 0 V, however, the load may not be sufficiently driven at low V_M voltages.

Overcurrent Protection

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. Operation resumes automatically after tRETRY has elapsed. Overcurrent conditions will be detected on both the high-side and low-side devices.

V_{CC} Undervoltage Lockout

If at any time the voltage on the V_{CC} pin falls below the under voltage lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when V_{CC} rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled.After the die temperature falls to a safe level, operation automatically resumes.

■ TYPICAL APPLICATION CIRCUIT