600mA Low Dropout Linear Regulator

General Description

The uP0111 is a compact fast response low dropout regulator specifically designed to continuously deliver up to 600mA output current. Designed with a P-channel MOSFET series pass transistor, the uP0111 yields extremely low dropout voltage (e.g. 300mV at 600mA) and maintains very low ground current (70uA).

The uP0111 does not require a bypass capacitor, hence achieving the smallest PCB area. The uP0111 is designed and optimized to work with low-value, low-cost ceramic capacitors. Only a 1uF ceramic output capacitor is required for stable operation for any load conditions.

Other features include foldback overcurrent protection, quick soft start, and overtemperature protection. The uP0111 is available in fixed output voltage from 0.8V to 3.3V with 0.1V per step or as an adjustable device with a 0.8V reference voltage. The device comes in various packages.

Applications

- Cellular and Cordless Phones
- Bluetooth Portable Radios and Accessaries
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Appliances

Ordering Information

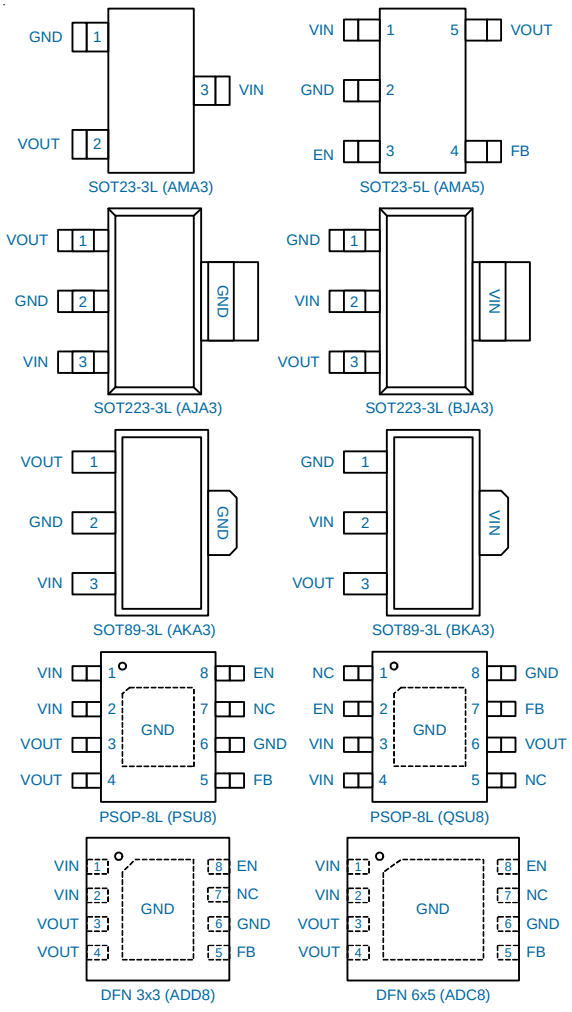
Order Number	Package	Remark
uP0111AMA3-XX	SOT23-3	XX: Voltage Options 00: Adjustable Output Voltage 08: 0.8V; 10: 1.0V; 12: 1.2V 15: 1.5V; 18: 1.8V; etc ... 1D: 1.35V; 1L: 1.34V (00 version is not available for 3-lead packages)
uP0111AMA5-XX	SOT23-5	
uP0111AJA3-XX	SOT223-3	
uP0111BJA3-XX	SOT223-3	
uP0111AKA3-XX	SOT89-3	
uP0111BKA3-XX	SOT89-3	
uP0111ADD8-XX	DFN3x3-8	
uP0111ADC8-XX	DFN6x5-8	
uP0111PSU8-XX	PSOP-8	
uP0111QSU8-XX	PSOP-8	

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Features

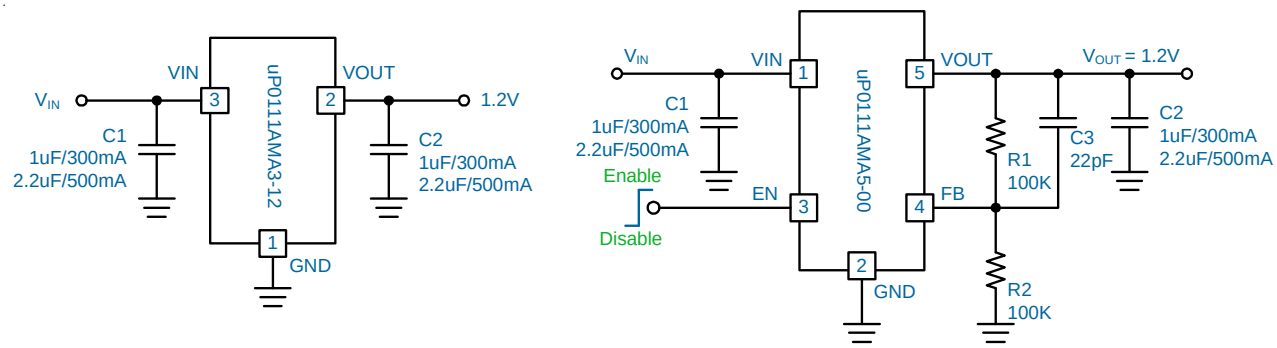
- Wide Input Voltage Range from 2.5V to 5.5V
- Ultra Low Dropout Voltage: 300mV @ 600mA
- Ultra Fast Response in Line/Load Transient
- Stable with 1uF Ceramic Output Capacitor
- Low Ground Current: 70uA Typical
- Low Shutdown Current: < 1uA
- Foldback Output Current Limit
- High Output Accuracy
  - 1.5% Initial Accuracy
  - Fixed Output Voltages: 0.8V to 3.3V
  - Adjustable Output Voltage from 0.8V to 4.5V
- Over-Temperature Protection
- RoHS Compliant and Halogen Free

Pin Configuration



Note: The figures are not to scale

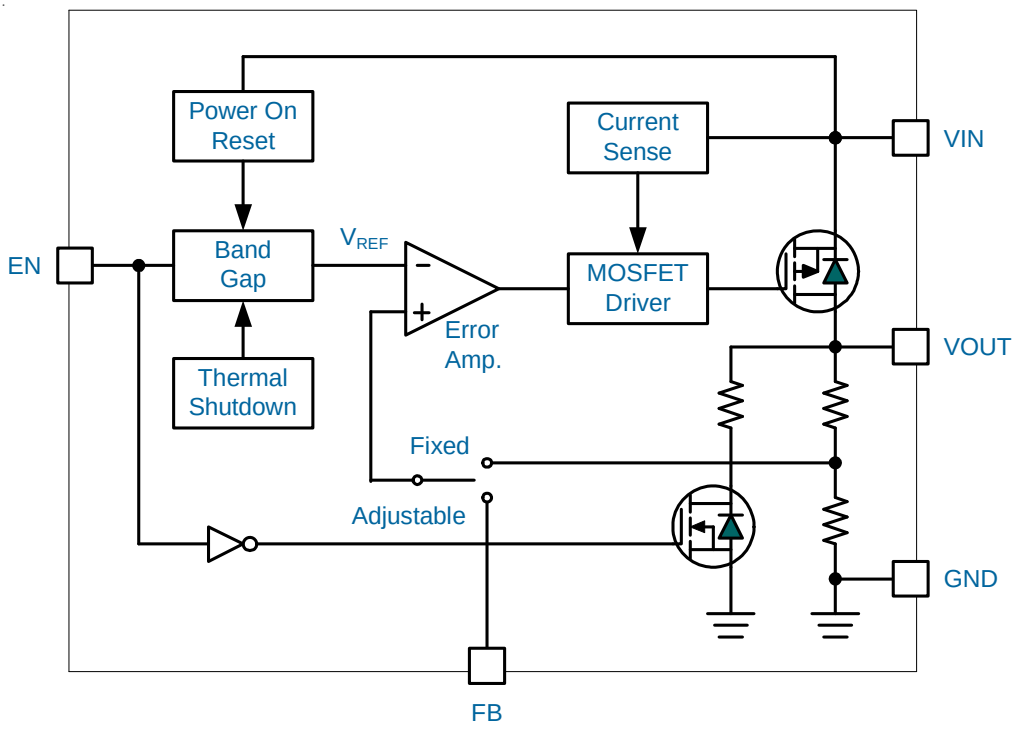
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	**Input Voltage.** This pin connects to the source of the internal pass transistor that supplies current to the output pin. Bypass VIN to GND with a minimum 1uF ceramic capacitor. Place the decoupling capacitor physically as close as possible to the device.
2	GND	**Ground.**
3	EN	**Enable Input.** Pulling this pin below 0.35V turns the regulator off, reducing the quiescent current to a fraction of its operating value. This pin is not available for 3-pin packages.
4B	F	**Feedback Pin (Adjustable Version).** This pin is the non-inverting input of the error amplifier. The FB pin voltage is regulated to 0.8V reference voltage. Set the output voltage according to V_{OUT} = 0.8 x (R1 + R2)/ R1 (V). This pin is not internally connected for the fixed output version.
5T	VOU	**Output Voltage.** This pin is power output of the device. A pull low resistance exists when the device is disabled by pulling low the EN pin. To maintain adequate transient response to large load change, a minimum 1uF ceramic capacitor is required to reduce the effects of current transients on VOUT.

Functional Block Diagram



Functional Description

Definitions

Some important terminologies for LDO are specified below.

Dropout Voltage

The input/output Voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 2% below its nominal value, dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation

The change in output voltage for a change in load current at constant chip temperature. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Maximum Power Dissipation The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Bias Current

Current which is used to operate the regulator chip and is not delivered to the load. The quiescent current I_Q is defined as the supply current used by the regulator itself that does not pass into the load. It typically includes all bias currents required by the LDO and any drive current for the pass transistor.

The uP0111 is a compact fast transient response low dropout regulator specifically designed to continuously deliver up to 600mA output current for space-limited applications. Designed with a P-channel MOSFET series pass transistor, the uP0111 yields extremely low dropout voltage (e.g. 300mV at 600mA) and maintain very low ground current (70uA). The uP0111 does not require a bypass capacitor, hence achieving the smallest PCB area. The uP0111 is designed and optimized to work with low-value, low-cost ceramic capacitors. Only a 1uF ceramic output capacitor is required for stable operation for any load conditions. Other features include foldback overcurrent protection, quick soft start, and overtemperature protection. The uP0111 is available in fixed output voltages from 0.8V to 3.3V with 0.1V increments.

As shown in the *Functional Block Diagram*, the uP0111 consists of a bandgap for reference voltage, error amplifier, P-channel MOSFET pass transistor and internal feedback

connected to the inverting input of error amplifier. The error amplifier compares this reference voltage with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled low. This allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled high, allowing less current to pass to the output. The output voltage is fed back through an internal or external resistor voltage-divider connected to the VOUT pin. Additional blocks include a current limiter, thermal sensor, and shutdown logic.

Supply Input Power On Reset

The input voltage supplies current to the output voltage and supplies current for control circuit. The input voltage is monitored for power on reset (POR) to ensure the regulator is not enabled until the input voltage is high enough for normal operation. The POR threshold level is typical 2.1V at V_{IN} rising.

Enable/Shutdown

The uP0111 features an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin lower than 0.35V shuts down the regulator and reduces its quiescent current less than 1uA. The voltage reference, error amplifier, gate-driver circuit and pass transistor are disabled in the shutdown state. When the regulator is in shutdown mode, an internal 600Ω resistor is connected between VOUT and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 600Ω has no adverse effect on device turn-on time.

Forcing the enable pin higher than 1.2V enables the output voltage (once the input voltage is higher than its POR threshold level). If the enable function is not needed in a specific application, it may be tied to VIN to keep the regulator in an always on state. The enable pin uses CMOS technology and cannot be left floating, as this may cause an indeterminate state on the output.

Current Limit and Short-Circuit Protection

The uP0111 includes a current limiter that monitors and controls the gate voltage of pass transistor to limit the output current to 1500mA typically. A short circuit protector monitors the output voltage and asserts output short circuit if V_{OUT} is lower than 40% of V_{NOM}. The current limiting level is reduced to 800mA. The output voltage is rebuilt after short circuit is removed.

Overtemperature Protection

The overtemperature protection limits total power dissipation in the uP0111. When the junction temperature exceeds T_J = 170 °C, the thermal sensor signal the shutdowns logic, turning off the pass transistor and allows the device to cool down. The thermal sensor turns on the pass transistor again after the device junction temperature drops by 40 °C, resulting in a pulsed output during continuous during continuous thermal-overload conditions. The overtemperature protection is designed to protect the device in the event of a fault condition. For continual operation, do not exceed the recommended temperature of T_J = 125 °C for maximum reliability.

Absolute Maximum Rating

Supply Input Voltage V_{IN} (Note 1) ---------- -0.3V to +6V
Other Pins ---------- -0.3V to (V_{IN} + 0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- SOT23-3L θ_{JA} ---------- 250 °C/W
- SOT23-5L θ_{JA} ---------- 250 °C/W
- SOT89-3L θ_{JA} ---------- 125 °C/W
- SOT223-3L θ_{JA} ---------- 62.5 °C/W
- DFN3x3-8L θ_{JA} ---------- 60 °C/W
- DFN6x5-8L θ_{JA} ---------- 45 °C/W
- PSOP-8L θ_{JA} ---------- 55 °C/W
- SOT23-3L θ_{JC} ---------- 140 °C/W
- SOT23-5L θ_{JC} ---------- 140 °C/W
- SOT89-3L θ_{JC} ---------- 15 °C/W
- SOT223-3L θ_{JC} ---------- 23 °C/W
- DFN3x3-8L θ_{JC} ---------- 5 °C/W
- DFN6x5-8L θ_{JC} ---------- 4 °C/W
- PSOP-8L θ_{JC} ---------- 5 °C/W

Power Dissipation, P_D @ T_A = 25°C
- SOT23-3L ---------- 0.4W
- SOT23-5L ---------- 0.4W
- SOT89-3L ---------- 0.8W
- SOT223-3L ---------- 1.6W
- DFN3x3-8L ---------- 1.8W
- DFN6x5-8L ---------- 2.2W
- PSOP-8L ---------- 2.0W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -20 °C to +125°C
Operating Ambient Temperature Range ---------- -20°C to +85°C
Supply Input Voltage, V_{IN} ---------- +2.5V to +5.5V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input Voltage						
Supply Input Voltage	V_{IN}		2.5	-	5.5	V
POR Threshold	V_{PORTH}		-	2.1	-	V
POR Hysteresis	V_{PORHYS}		-	0.4	-	V
Quiescent Current	I_Q	V_{EN} = 5V, I_{OUT} =0mA	40	75	110	uA
Shutdown Current	I_{SHDN}	V_{EN} =0V	-	0.1	1	uA
Output Voltage						
Output Voltage Accuracy	V_{OUT}	V_{IN} = V_{NOM} + 1.0V; I_{OUT} =1mA fixed output voltage version	-1.5	-	1.5	% V_{NOM}
Reference Voltage Accuracy	V_{FB}	V_{IN} = 3.3V, I_{OUT} = 1mA, VOUT = FB, adjustable output voltage version	0.788	0.8	0.812	
Output Line Regulation	$\Delta V_{REF(LINE)}$	2.5V < V_{IN} < 5.5V, and V_{IN} > V_{OUT} + 1.0V, I_{OUT} = 1mA	-	0.02	0.2	%/V
Output Load Regulation	$\Delta V_{REF(LOAD)}$	1mA < I_{OUT} < 500mA, V_{IN} = V_{NOM} +-1.0V	-5	0	1	%/A
Dropout Voltage	V_{DROP}	I_{OUT} = 300mA, 2.5V < V_{IN} <-2.7V	-	180	240	mV
		I_{OUT} = 600mA, 2.7V < V_{IN} <-5.5V	-	300	400	
Power Supply Rejection Ratio	PSRR	Frequency = 10Hz, I_{OUT} =-10mA	-8	6-	-	dB
		Freequency = 1kHz, I_{OUT} =-10mA	-5	6-	-	
		Frequency = 100kHz, I_{OUT} =-10mA	-0	5-	-	
		Frequency = 10Hz, I_{OUT} =-300mA	-8	4-	-	
		Freequency = 1kHz, I_{OUT} =-300mA	-2	6-	-	
		Frequency = 100kHz, I_{OUT} =-300mA	-5	6-	-	
Enable						
Enable High Level	V_{EN}		1.2	--	-	V
Disable Low Level	V_{SD}		--	-	0.3	V
EN Input Current	I_{EN}	V_{IN} = 5.5V, V_{EN} =5.5V or 0V	--	-1		uA
Enable Delay Time	T_{DELAY}	form V_{EN} > 1.2V to V_{OUT} > 10%V_{NOM}, by design	-0	1-	-s	u
Output Ramp Up Time	T_{SS}	from V_{OUT} = 10% to 90% of V_{NOM}, by design	-0	4-	-s	u

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection						
Current Limit Threshold	$_{LIM}$		0.9	1.-	-A	
Short Circuit Current			0.6	--	-A	
Thermal Shutdown Temperature	T_{SD}	I_{OUT} = 0mA, V_{IN} = V_{EN} = 5.5V,	-0	17	-	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	I_{OUT} = 0mA, V_{IN} = V_{EN} =-5.5V	-0	4-	-	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operation Characteristics

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Application Information

The uP0111 is specially designed to provide low-noise, high PSRR output voltage without a bypassing capacitor on its reference voltage. However, input and output capacitor should be well considered for optimal performance.

Input Capacitors

The uP0111 requires well-decoupled supply input for optimal performance. A minimum 1uF capacitor is required from-input-to-ground to provide stability. Input capacitors greater than 1uF offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection ratio (PSRR). Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, low-ESR ceramic capacitors provide optimal performance at a minimum of space and are highly recommended due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices. Additional high frequency capacitors, such as small-valued NPO dielectric type capacitors, help filter out high-frequency noise and are good design practice in any RF-based circuit. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Output Capacitors and Stability

For proper load voltage regulation and operational stability, a capacitor is required between VOUT and GND pins. The uP0111 is designed and optimized to work with low-value, low-cost ceramic capacitors in space saving and performance consideration. Typical output capacitor values for maximum output current conditions range from 1uF to 10uF. Larger capacitors are recommended for applications expecting low output noise and optimum power supply ripple rejection characteristics. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R type capacitors loss capacitance by 15% over their operating temperature rand and are the most stable type of ceramic capacitors. Z5U or Y5V dielectric capacitors loss their capacitance by 50% and 60% respectively over their operating temperature ranges. If Y5V or Z5U capacitors are used as output capacitors, the capacitance must be much higher than that of X7R capacitors to ensure the same minimum capacitance over the operating temperature range.

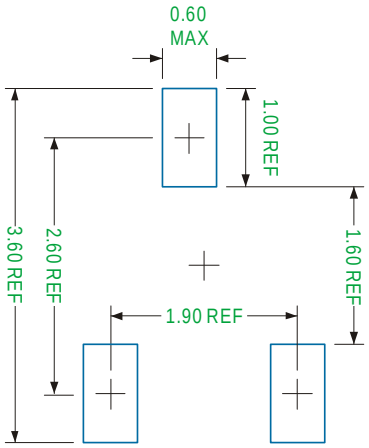
ESR of output capacitors should be well considered to ensure stable operation of the device. High ESR capacitors may cause high frequency oscillation. Figure 1 shows the acceptable ESR range of output capacitor for stability.

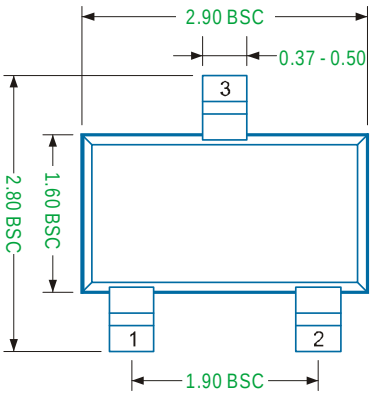
No Load Stability

The uP0111 is designed to maintain output voltage regulation and stability under operational no load conditions. This is important characteristic for CMOS RAM keep-alive applications where the output current may drop to zero.

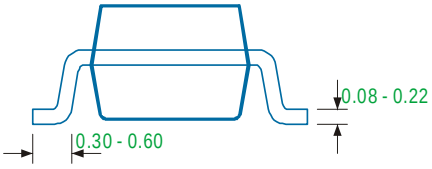
Package Information

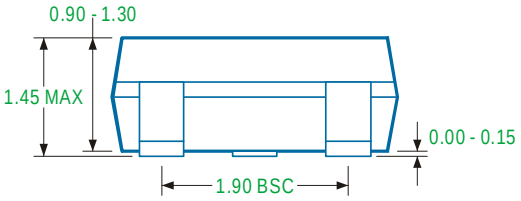
SOT23-3L



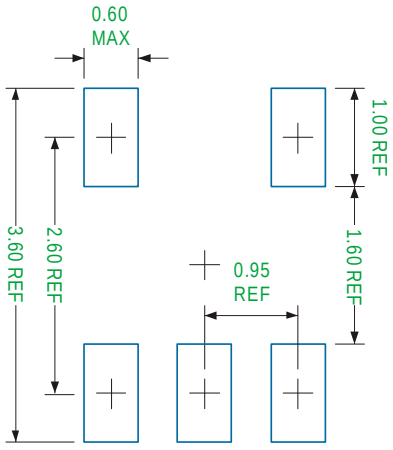


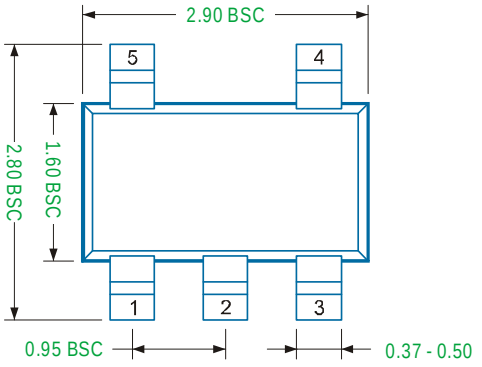
Recommended Solder Pad Layout





SOT23-5L





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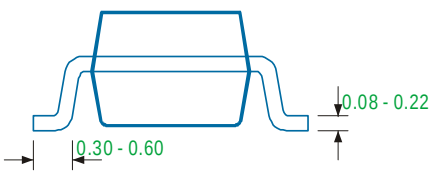
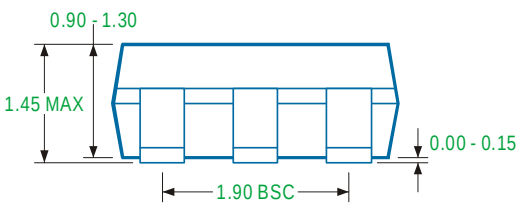
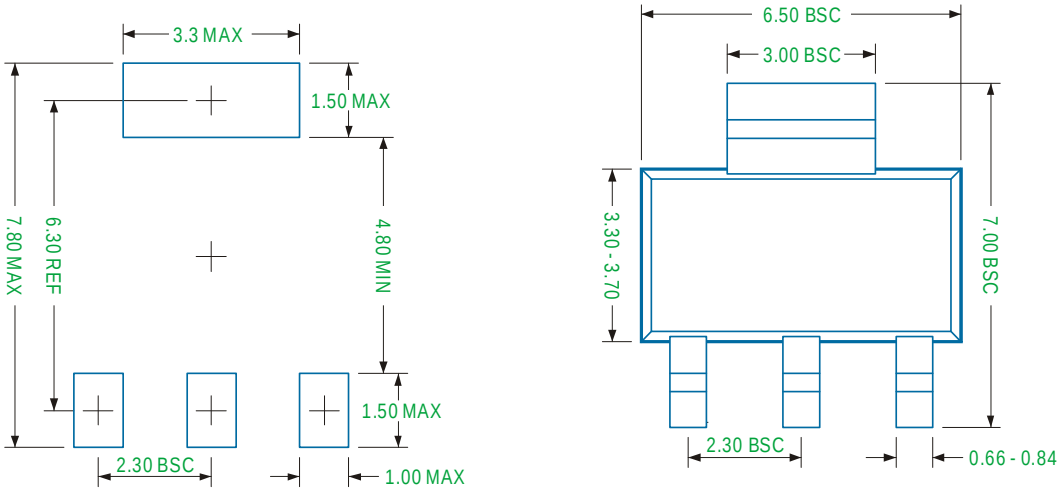


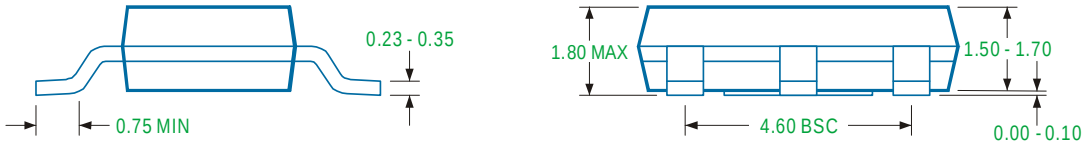


Package Information

SOT223 - 3L



Recommended Solder Pad Layout



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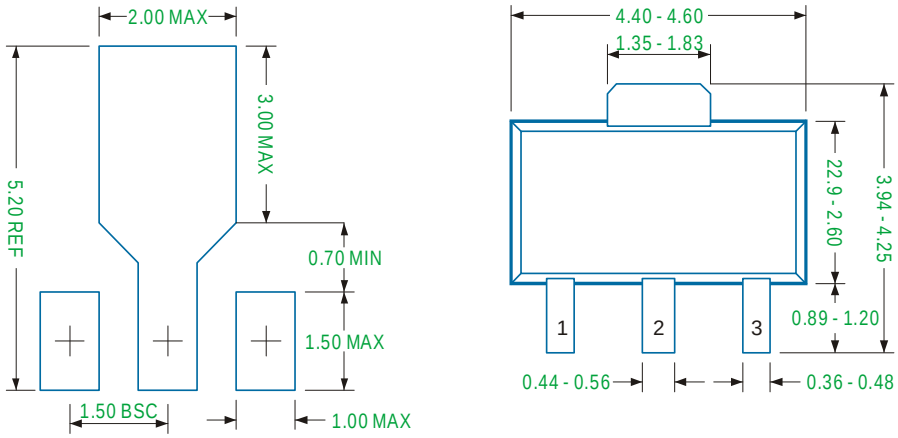
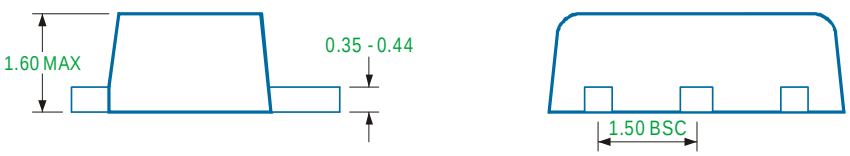
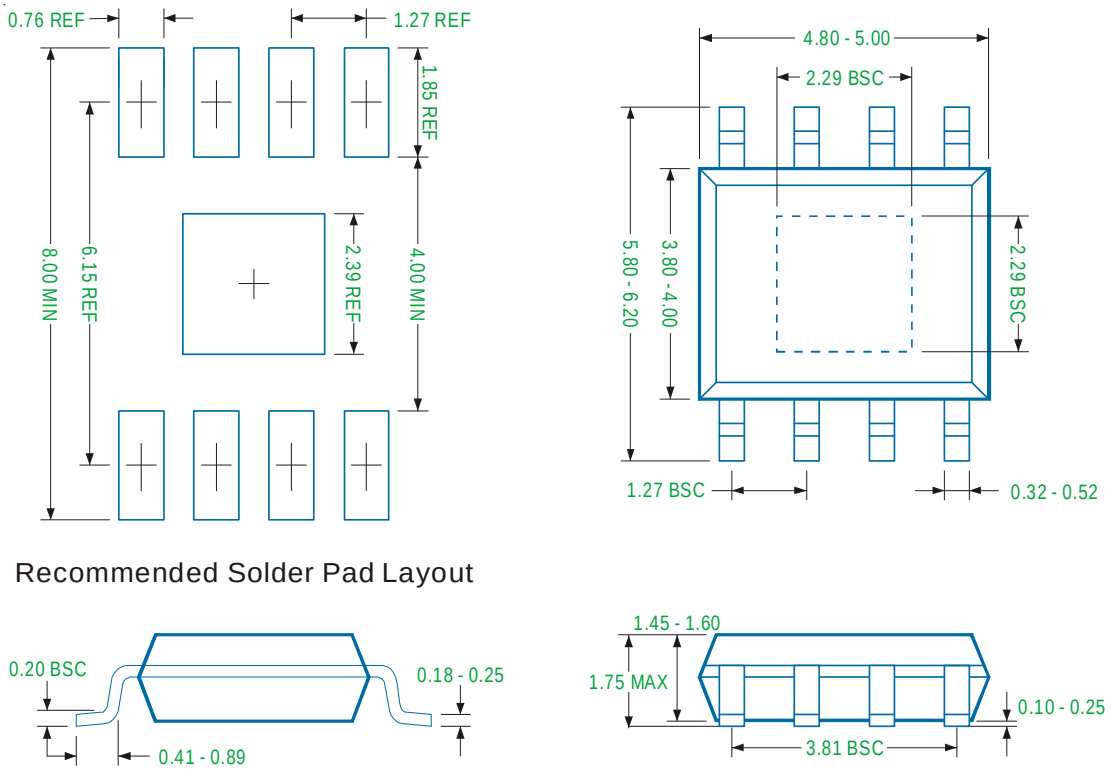


Recommended Solder Pad Layout



Package Information

PSOP - 8L

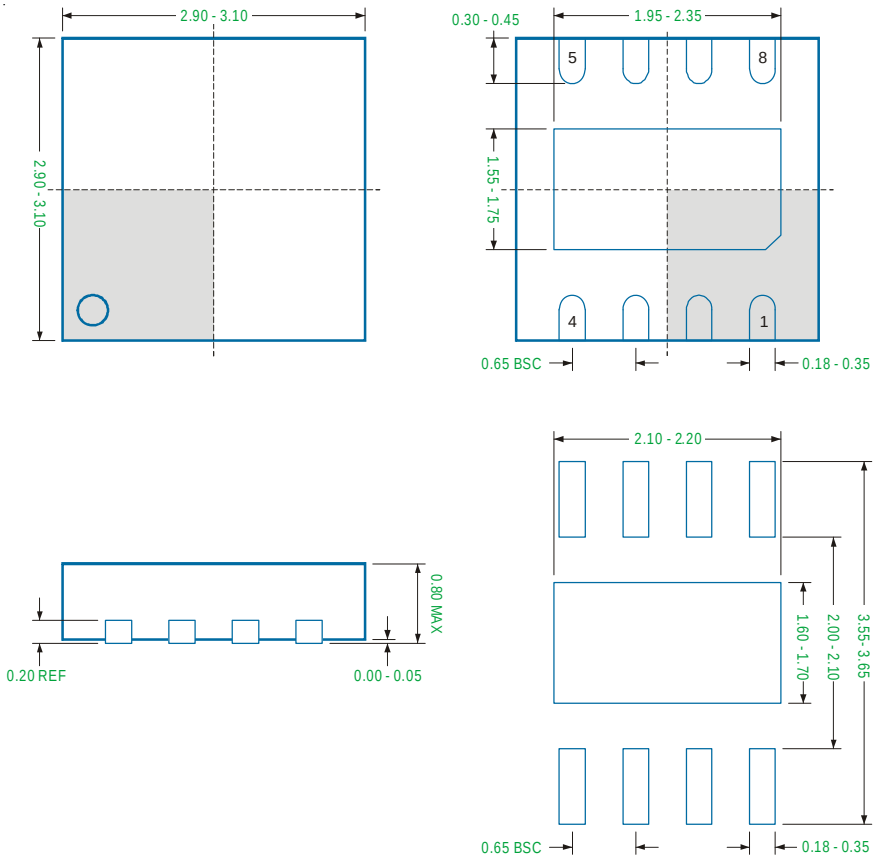


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

Package Information

DFN3x3 - 8L



Recommended Solder Pitch and Dimensions

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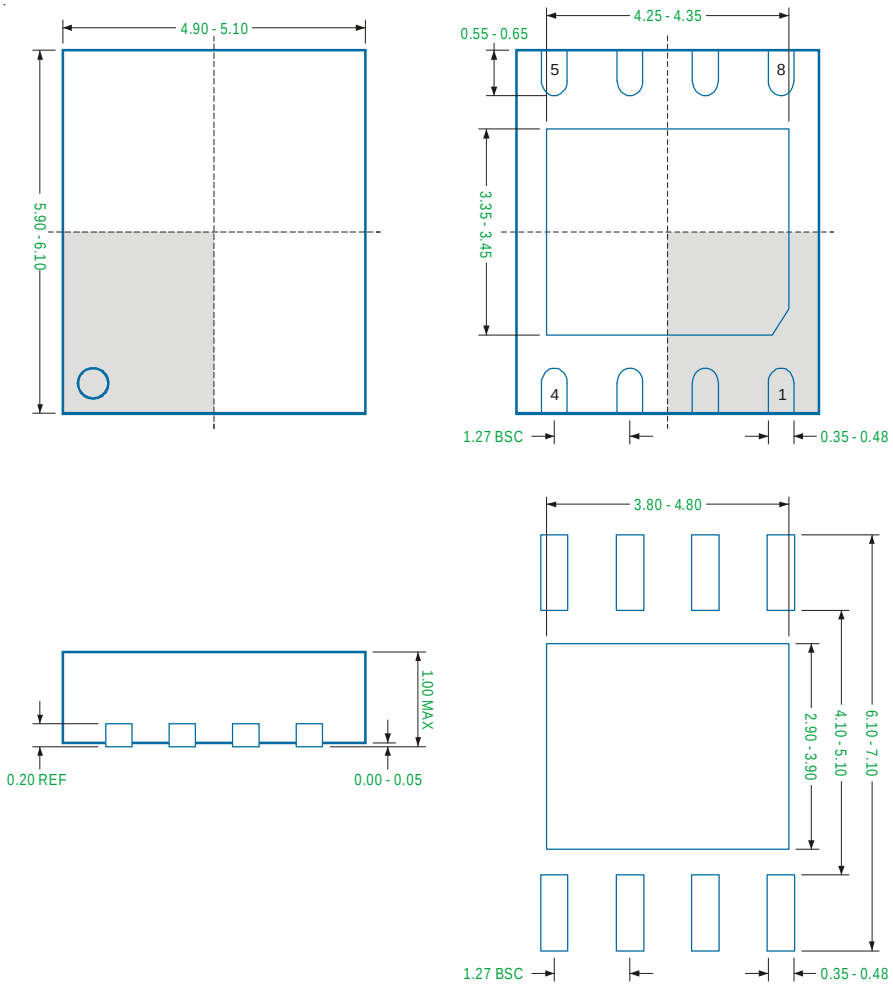
Package Information

DFN6x5 - 8L



Recommended Solder Pitch and Dimensions

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