Dual Synchronous Buck Controller with 5V/3.3V 100mA LDOs for Notebook System Power

General Description

The uP6182 is a dual synchronous buck controller with 5V/3.3V 100mA LDOs for notebook system power supply solution. A 250kHz VCLK output can be used for external charge pump to generate gate drive voltage for load switches.

The uP6182 supports high efficiency, fast transient response and a combined power-good signal. The out of audio mode maintains the switching frequency above audio frequency, which eliminates noise in audio applications. The adaptive on-time control provides a convenient and efficient operation.

The uP6182 has internal soft-start to control the inrush current. The soft-stop feature avoids negative output voltage for undervoltage protection, overcurrent protection, and shutdown by discharging output through an internal switch, and by damping the inductor current.

Supply input voltages ranging from 5.5V to 26V and output voltages from 2V to 5.5V. Other features include overcurrent protection, overvoltage protection, power-up sequencing, power OK output, and thermal shutdown. The uP6182 is available in the space saving package VQFN4x4-24L, specified from -40 °C to 85 °C.

Applications

- **Notebook and Subnotebook System Power Supplies**
- **3-4 Cell Li-Ion Battery-Power Devices**
- **Dual Output Supplies for DSP, Memory, Logic and Microprocessor**

Ordering Information

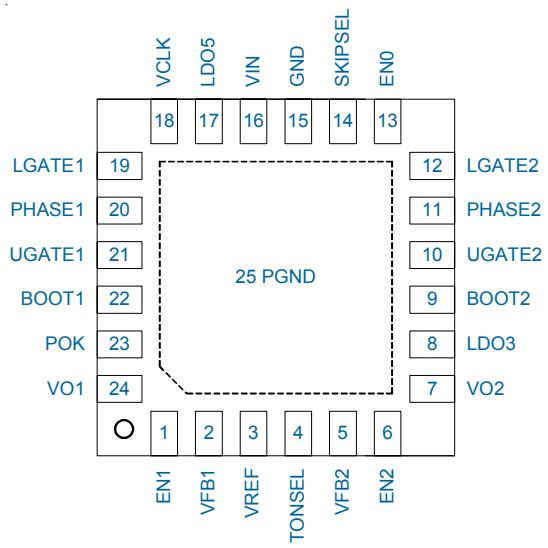
Order Number	Package Type	Remark
uP6182AQAG	VQFN4x4 - 24L	

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

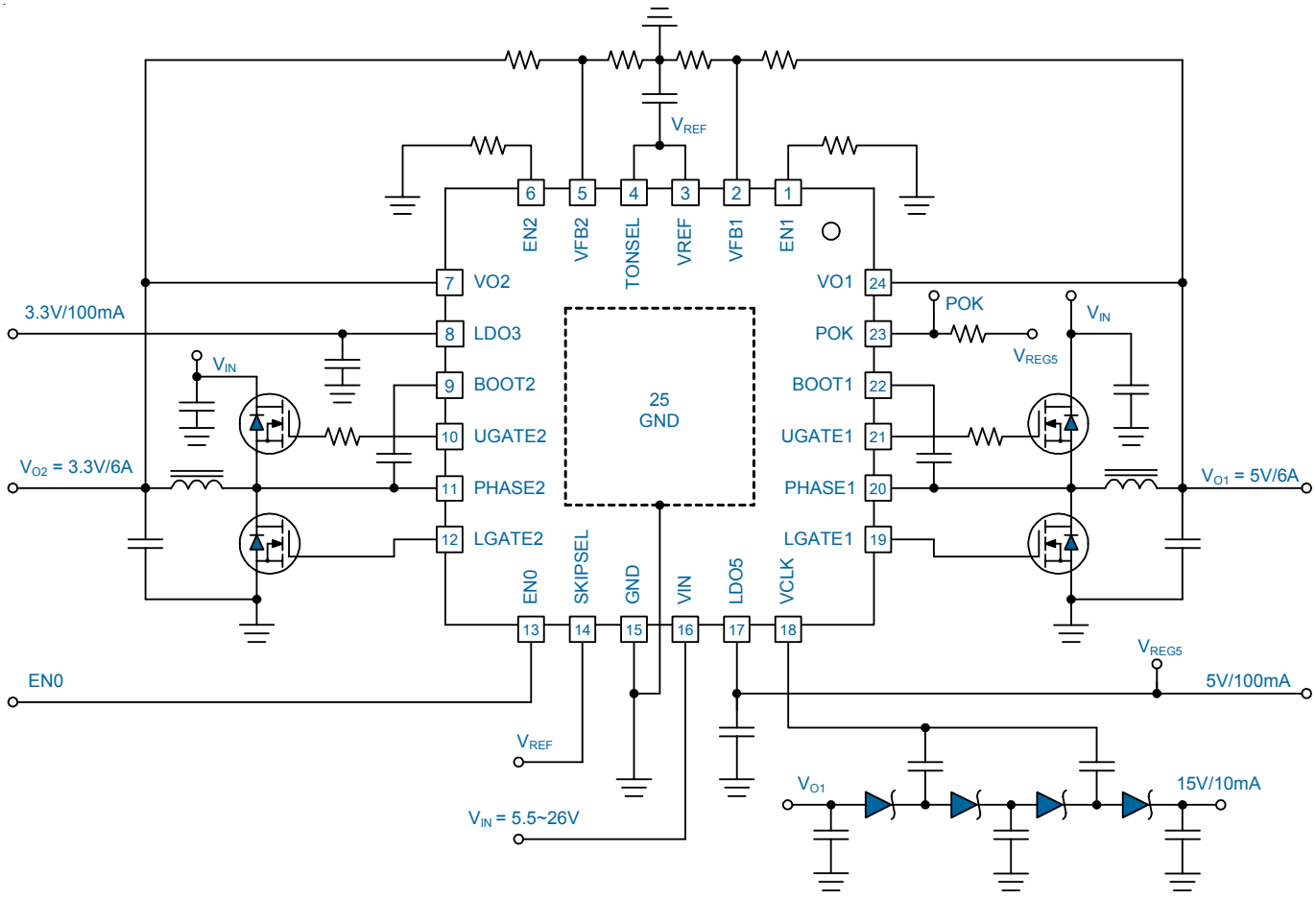
Features

- **Wide Input Voltage Range: 5.5V to 26V**
- **Two Synchronous Buck Controllers**
  - **Output Voltage Range: 2V to 5.5V**
  - **Selectable Audio Mode in Light Load**
  - **Internal 1.6ms Output Voltage Softstart**
  - **Adaptive On Time Control Architecture**
  - **4500ppm/°C $R_{DS(ON)}$ Current Sensing**
- **100mA 5V/3.3V LDO with Switches**
- **1% 2V Reference Voltage Output**
- **Power Good Output**
- **OVP/UVP/OCP**
- **Thermal Shutdown**
- **VQFN4x4-24L**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Pin Configuration



Typical Application Circuit



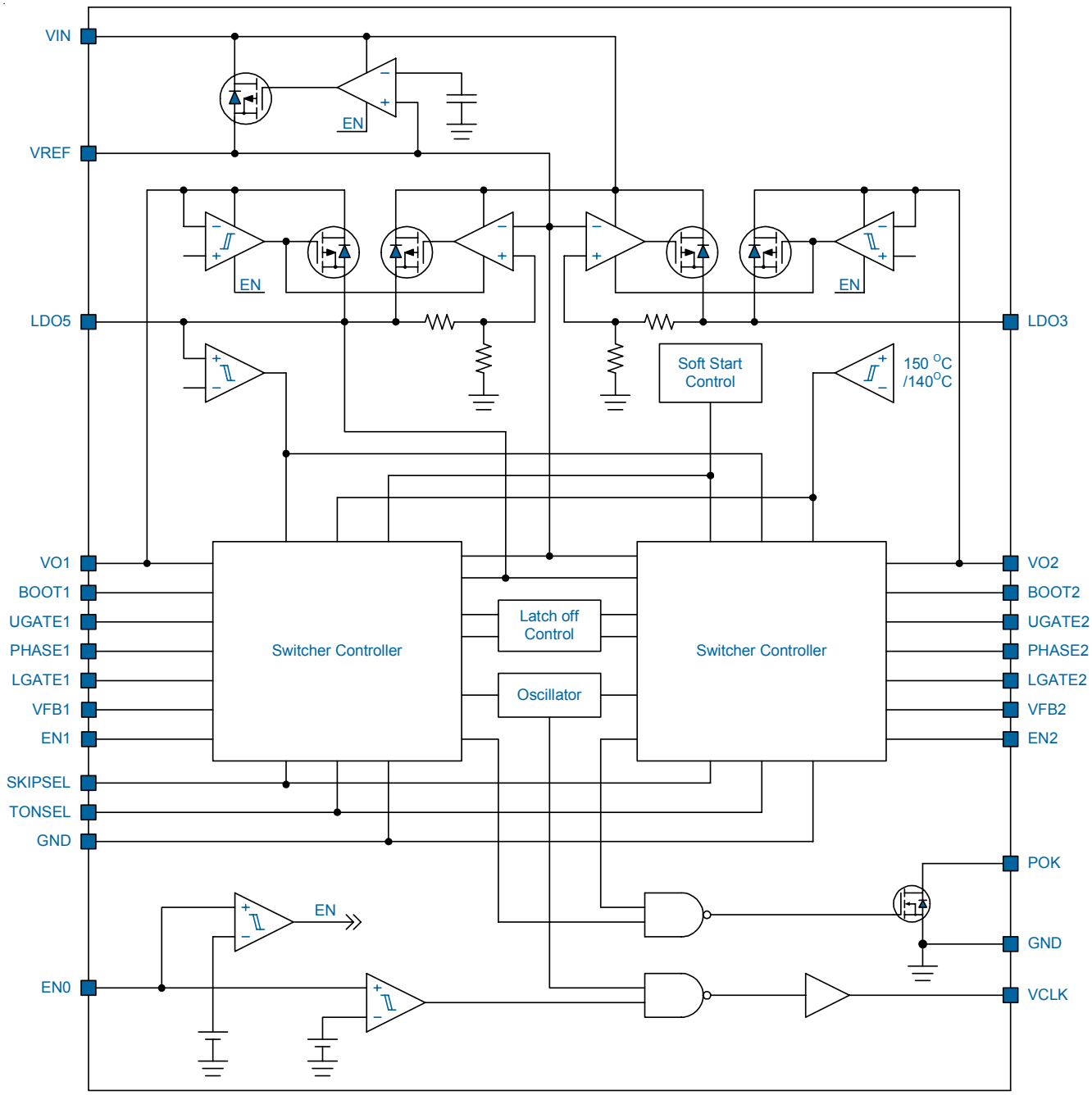
Functional Pin Description

No.	Name	Pin Function
1	EN1	**Synchronous Buck Converter 1 Enable and OCP Setting.** Connect resistor from this pin to GND to set threshold for synchronous buck 1 $R_{DS(ON)}$ OCP. Short to ground to shutdown a switcher channel.
2	VFB1	**Synchronous Buck Converter 1 Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.
3	VREF	**2V Reference Voltage Output.** Bypass this pin with a 0.22uF ceramic capacitor to GND. This pin is capable of sourcing up to 100uA current for external loads.
4	TONSEL	**On-Time Adjustment Pin.** 365k/460k: Connect this pin to LDO5. 300k/375k: Connect this pin to LDO3. 245k/305k: Connect this pin to VREF 200k/250k: Connect this pin to GND
5	VFB2	**Synchronous Buck Converter 2 Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage
6	EN2	**Synchronous Buck Converter 2 Enable and OCP Setting.** Connect resistor from this pin to GND to set threshold for synchronous buck 2 $R_{DS(ON)}$ OCP. Short to ground to shutdown a switcher channel.
7	VO2	**Output of Synchronous Buck 2.**This pin works as Fixed Voltage Inputs and output discharge inputs. VO1 also work as 3.3V switch over return power input respectively.
8	LDO3	**Output of Internal 3.3V LDO.** The LOD3 is capable of sourcing 100mA output current for external loads. Bypass this pin with a minimum 4.7uF.
9	BOOT2	**Bootstrap Supply** for the floating upper gate driver of synchronous buck 2 connect the bootstrap capacitor C_{BOOT} between BOOT2 pin and the PHASE2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
10	UGATE2	**Upper Gate Driver Output for Synchronous Buck 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
11	PHASE2	**Switch Node for Synchronous Buck 2 .**Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE1driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
12	LGATE2	**Lower Gate Driver Output for Synchronous Buck 2.**Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.
13	EN0	**LDO, VCLK Enable:** Open: enable both LDOs, VCLK on and ready to turn on switcher channels. 680kΩ to GND: enable both LDOs, VCLK off and ready to turn on switcher channels. GND: disable all circuit.
14	SKIPSEL	**Operation Mode Selection Pin:** Out of Audio: Connect this pin to LDO3 or LDO5. Auto Skip: Connect this pin to VREF. PWM only: Connect this pin to GND.
15	GND	**Signal Ground for the IC.** All voltages levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Pin Description

No.	Name	Pin Function
16	VIN	**Supply Input.** This pin is the input of the internal 5V and 3.3V LDO regulators. Connect VIN to the battery or AC adapter output.
17	LDO5	**Output of Internal 5V LDO.** The LOD5 is capable of sourcing 100mA output current for external loads. Bypass this pin with a minimum 4.7uF.
18	VCLK	**Clock Output** for 250kHz 15V charge pump.
19	LGATE1	**Lower Gate Driver Output for Synchronous Buck 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.
20	PHASE1	**Switch Node for Synchronous Buck 1.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE1driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
21	UGATE1	**Upper Gate Driver Output for Synchronous Buck 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
22	BOOT1	**Bootstrap Supply** for the floating upper gate driver of synchronous buck 1 connect the bootstrap capacitor C_{BOOT} between BOOT1 pin and the PHASE1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Typical values for C_{BOOT} range from 0.1uF to 0.47uF. Ensure that C_{BOOT} is placed near the IC.
23	POK	**Open Drain Output for PowerOK Indication.** This pin is set to high impedance with adequate time delay after softstart cycle completes and both switcher outputs are above 105% of the regulated voltages. It is pulled low immediately when either output is below 105% of the regulated output.
24	VO1	**Output of Synchronous Buck 1.** These terminals work as fixed voltage inputs and output discharge inputs. VO1 also work as 5V switch over return power input respectively.
25	Exposed Pad	**Ground.** The exposed pad is the dominate heat conduction path and should be well soldered to PCB for optimal thermal performance.

Functional Block Diagram



Functional Description

The uP6182 is a dual synchronous buck converter with 100mA 3.3V/5V LDOs is ideal for high-voltage, low-power supplies for notebook computers. A 250kHz VCLK output can be used for external charge pump to generate gate drive voltage for load switches. The uP6182 supports high efficiency, fast transient response and a combined power-good signal. The out of Audio mode maintains the switching frequency above audio frequency, which eliminates noise in audio applications. The adaptive on-time control provides a convenient and efficient operation. The uP6182 has internal soft-start to control the inrush current. The soft-stop feature avoids negative output voltage for undervoltage protection, overcurrent protection, and shutdown by discharging output through an internal switch, and by damping the inductor current. Other features include overcurrent protection, overvoltage protection, power-up sequencing, power OK output, and thermal shutdown.

Enable and Soft Start

EN0 is the control pin of VREG5, VREG3 and VREF regulators. Connect this node to GND disables

three regulators and decrease the shutdown supply current to 10uA. Connect this node to 3.3V or 5V will turn the three regulators on to standby mode. Two SMPSs become ready to enable at this standby mode. The uP6182 has an internal 1.6 ms output voltage softstart for each channel. When the ENx pin becomes high level, an internal SS begins ramping up the reference voltage to the reference voltage of PWMs. The uP6182 shares one SS with both channels, if ENx pin becomes high level while another channel is starting up, soft start is postponed until another channel soft start has completed. If both of EN1 and EN2 become high level at a same time (within 60us), both channels start up at 1.6ms soft start time.

Table 1. Enabling State

EN0	EN1	EN2	VREF	LDO5	LDO3	CH1	CH2	VCLK
GND	X	X	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On

On Time Control and PWM Frequency

The uP6182 runs with constant frequency by feed-forwarding the input and output voltage into the on-time, one-shot timer. The on-time is controlled proportional to VOUT/VIN so that the duty ratio will be kept as technically as with the same cycle time. The frequencies are set by TONSEL terminal connection as Table 2.

Table 2. TONSEL Connection and Switching Frequency

TONSEL Connection	Switching Frequency	
	CH1	CH2
GND	200KHz	250KHz
VREF	245KHz	305KHz
LDO3	300KHz	375KHz
LDO5	365KHz	460KHz

Auto Skip and Ultra-Sonic Mode (USM)

The uP6182 automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreased, the rectifying MOSFET is turned off when zero inductor current is detected, the converter runs in discontinuous conduction mode and it takes long time to discharge the output capacitor to next ON cycle.

Ultra sonic mode is a technique that keeps the switching frequency above audible frequencies while maintaining best of the high conversion efficiency. When the ultra sonic mode is selected, USM control circuit monitors both MOSFET and force to change into the ON state if both of MOSFETs are off for more than 32 μs. USM control circuit detects the over-voltage condition and begins to modulate the on time to keep the output voltage regulated.

LDO3/LDO5 Linear Regulators

The uP6182 has two sets of 100-mA linear regulators which outputs 5V and 3.3V, The LDO5 provides the main power supply for the circuitry of the device and provides the current for gate drivers.The LDO3 is intended mainly for 3.3V supply for the notebook system during standby mode. The 10uF and 22uF ceramic capacitors are placed close to regulators pins for stability.

LDO3/LDO5 Switcher

When the VO1 voltage becomes higher than 4.7V /3.15V AND internal POK flag is tiggered, internal 3.3V/5V LDO regulators are turned off shut off and the 3.3V/5V outputs are connected to VO1/VO2 . The 510us POK delay helps a switcher without glitch.

Output Discharge Control

When ENx is low, the uP6182 discharges outputs using internal MOSFET which is connected to VOx.

The current capability of these MOSFETs is limited to discharge slowly.

POK

The uP6182 has one POK output indicator, when both SMPS outputs are within the targets. The POK function is activated with 2ms delay after ENx goes high. If the

output voltage is within +/-5% of the target value, internal comparators detect power good state and the POK signal becomes high after 510μs delay. Therefore POK goes high around 2.5ms after ENx goes high. If the output voltage goes outside of +/-10% of the target value, the POK signal becomes low after 2μs delay. The POK output is an open drain output and is needed to be pulled up to output voltage source.

VCLK Charge Pump

270kHz clock signal is used for charge pump circuit to generate a 15V dc voltage. The clock signal becomes available when EN0 becomes higher than 2.4V or open state. The clock driver uses VO1 as its power supply. Regardless of enable or disable of VCLK, power consumption of the uP6182 is almost the same. Therefore even if VCLK is not used, one can let EN0 pin open or supply logic high and let VCLK pin open.

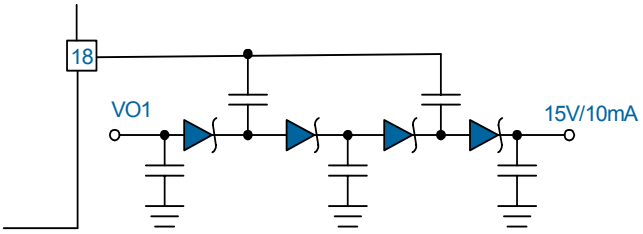


Figure 2. Charge Pump Configuration

Over Current Protection

The uP6182 has cycle-by-cycle over current limiting control. The inductor current is monitored during the off state and the controller keeps the off state when the inductor current is larger than the over current trip level.

In order to provide both good accuracy and cost effective solution, uP6182 supports temperature compensated MOSFET RDS(on) sensing. ENx pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. ENx terminal sources I_{TRIP} current, which is 10 μA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as below. Note that the V_{TRIP} is limited up to about 205 mV internally.

$$V_{TRIP}(mV) = \frac{R_{TRIP}(k\Omega) \times I_{TRIP}(uA)}{9} - 24(mV)$$

The voltage between GND pin and PHASEx pin monitors the inductor current so that PHASEx pin should be connected to the drain terminal of the bottom MOSFET properly. I_{TRIP} has 4500 ppm/°C temperature slope to compensate the temperature dependency of the RDS(on). GND is used as the positive current sensing node so that GND should be connected to the proper current sensing device, i.e. the source terminal of the bottom MOSFET.

When the comparison is done during the off state, V_{TRIP} sets valley level of the inductor current. Therefore, the load current at over current threshold, I_{LIM}, can be calculated as follows:

$$I_{LIM} = \frac{V_{TRIP}}{R_{DSON}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{V_{TRIP}}{R_{DSON}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

In an over current condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it ends up with crossing the under voltage protection threshold and shutdown both channels.

Over/Under Voltage Protection

The uP6182 monitors the feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 115% target voltage, the OVP circuit latches as the upper MOS off and the lower MOS on. The uP6182 monitors VOx voltage directly and if it becomes higher than 5.75V, the uP6182 turns off the top MOSFET driver. When the feedback voltage becomes lower than 60% target voltage, the UVP occurs and after 32us UVP delay, the uP6182 latches off both side MOSFETs, and shut off both drivers of another channel. This function is enabled after 2ms following ENx has become high.

UVLO Protection

uP6182 has LDO5 under voltage lock out protection (UVLO). When the LDO5 voltage is lower than UVLO threshold voltage both SMPS are turned off. This is non-latch protection. When the LDO3 voltage is lower than (VO2 - 1 V), both switch mode power supplies are also turned off.

Over Temperature Protection

The uP6182 monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP6182 is turned off including LDOs. This is a non-latch protection.

Absolute Maximum Rating

Supply Input Voltage, VIN (Note1) ---------- -0.3V to +28V
BOOT to PHASE ---------- -0.3V to (LDO5 + 0.3V)
PHASE to GND
DC ---------- -0.3V to 28V
< 100ns ---------- -5V to 40V
LGATE to GND
DC ---------- -0.3V to (LDO5 + 0.3V)
< 100ns ---------- -2V to (LDO5 + 2V)
EN0, EN1, EN2, VFB1, VFB2, VO1, VO2,TONSEL, SKIPSEL ---------- -0.3V to +6V
POK, VCLK, LDO3, LDO5, VREF, to GND ---------- -0.3V to 6V
Storage Junction Temperature Range ---------- -65°C to +150°C
Lead Temperature Range(Soldering 10sec) ---------- 260°C
ESD Rating (Note2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN4x4 - 24L θ_{JA} ---------- 40°C/W
VQFN4x4 - 24L θ_{JC} ---------- 6°C/W
Power Dissipation, P_D @ TA = 25°C
VQFN4x4 - 24L ---------- 2.5W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, VIN ---------- 5.5V to +26V

Electrical Characteristics

Electrical characteristics over recommended free-air temperature range, V_{IN}=12V. (Unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Current						
VIN Supply Current1	I_{VIN1}	VIN current, T_A=25°C, No Load, VO1=0V, VO2=0V, ENx=5V, VFB1=VFB2=2.05V	--	0.55	1	mA
VIN Standby Current	$I_{VINSTBY}$	VIN current, T_A=25°C No Load, EN0=1V, ENx=0V	--	--	250	uA
VIN Shutdown Current	I_{VIN1}	VIN current, T_A=25°C, No Load, EN0=ENx=0V	--	--	28	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VREF Output						
VREF Output Voltage	V_{VREF}	I_{VREF} = 0A	1.98	2.00	2.02	V
		-5uA < I_{VREF} < 100uA	1.97	2.00	2.03	V
LDO5 Output						
LDO5 Output Voltage	V_{VLDO5}	VO1 = 0V, I_{LDO5} < 100mA, TA = 25 °C	4.8	5.0	5.2	V
		VO1 = 0V, I_{LDO5} < 100mA, 6.5V < VIN < 26V	4.75	5.0	5.25	V
		VO1 = 0V, I_{LDO5} < 50mA, 5.5V < VIN < 26V	4.75	5.0	5.25	V
LDO5 Output Current	I_{VLDO5}	VO1 = 0V, LDO5 = 4.5V	200	300	400	mA
Switch Over Threshold	V_{TH5VSW}	Turns on	4.55	4.7	4.85	V
		Hysteresis	--	0.25	--	V
5V SW Ron	R_{5VSW}	VO1 = 5V, I_{VLDO5} = 100mA	--	1	3	Ω
LDO3 Output						
LDO3 Output Voltage	V_{LDO3}	VO2 = 0V, I_{LDO3} < 100mA, TA = 25 °C	3.20	3.33	3.46	V
		VO2 = 0V, I_{LDO3} < 100mA, 6.5V < VIN < 26V	3.13	3.33	3.50	V
		VO2 = 0V, I_{LDO3} < 50mA, 5.5V < VIN < 26V	3.13	3.33	3.50	V
LDO3 Output Current	I_{LDO3}	VO2 = 0V, LDO3 = 3V	100	175	250	mA
Switch Over Threshold	V_{TH3VSW}	Turns on	2.82	2.88	2.94	V
		Hysteresis	--	0.25	--	V
3V SW Ron	R_{3VSW}	VO2 = 3.3V, I_{LDO3} = 100mA	--	1.5	4	Ω
Output						
Internal Reference Voltage	V_{IREF}	I_{VREF}=0A, beginning of ON state	1.95	1.98	2.01	V
VFB Regulation Voltage	V_{VFB}	FB voltage, I_{VREF} = 0A, continuous conduction	--	2.00	--	V
VFB Input Current	I_{VFB}	VFBx = 2.0 V, T_A = 25 °C	-20	--	20	nA
VOUT Discharge Current	I_{Dischg}	ENx = 0V, VOx = 0.5V	10	60	--	mA
Output Drivers						
UGATE Resistance	R_{UGATE}	Source, $V_{BOOTx-UGATEx}$ = 100mV	--	4	8	Ω
		Sink, $V_{UGATE-PHASE}$ = 100mV	--	1.5	4	Ω
LGATE Resistance	R_{LGATE}	Source, $V_{LDO5-LGATE}$ = 100mV	--	4	8	Ω
		Sink, V_{LGATEx} = 100mV	--	1.5	4	Ω
Dead time	T_D	UGATEx-low toLGATEx-on	--	10	--	ns
		LGATEx-off toUGATEx-on	--	30	--	ns

Electrical Characteristics

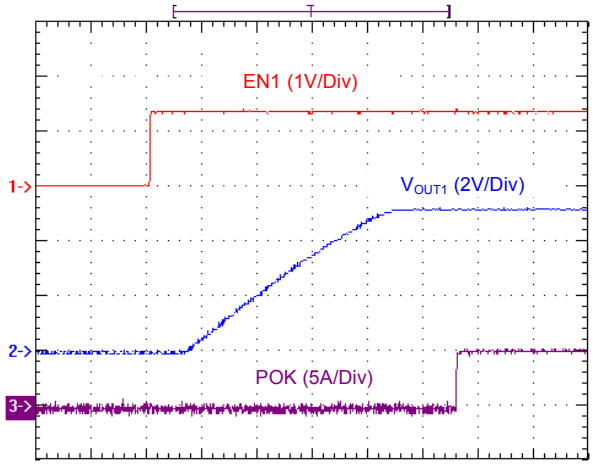
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Clock Output						
High Level Voltage	V_{CLKH}	I_{out}= 10mA, VO1=5V	4.84	4.92	--	V
Low Level Voltage	V_{CLKL}	I_{out} = 10mA, VO1=5V	--	0.06	0.12	V
Clock Frequency	f_{CLK}	f_{CLK}	180	240	300	kHz
Internal Bootstrape Diode						
Forward Voltage	V_{FBOOT}	$V_{LDO5-BOOTx}$, I_F = 10mA	0.7	0.8	0.9	V
VBOOT Leakage Current	$I_{VBOOTLK}$	VBOOT=36V, PHASE=28V, VOUTx=5.5V	--	0.1	1	uA
Duty and Frequency Control						
CH1 On Time 1	T_{ON11}	V_{IN}=12V, VO1=5V, 200kHz setting	--	2080	--	ns
CH1 On Time 2	T_{ON12}	V_{IN}=12V, VO1=5V, 245kHz setting	--	1700	--	ns
CH1 On Time 3	T_{ON13}	V_{IN}=12V, VO1=5V, 300kHz setting	--	1390	--	ns
CH1 On Time 4	T_{ON14}	V_{IN}=12V, VO1=5V, 365kHz setting	--	1140	--	ns
CH2 On Time 1	T_{ON21}	V_{IN}=12V, VO2=3.3V, 250kHz setting	--	1100	--	ns
CH2 On Time 2	T_{ON22}	V_{IN}=12V, VO2=3.3V, 305kHz setting	--	900	--	ns
CH2 On Time 3	T_{ON23}	V_{IN}=12V, VO2=3.3V, 375kHz setting	--	730	--	ns
CH2 On Time 4	T_{ON24}	V_{IN}=12V, VO2=3.3V, 460kHz setting	--	600	--	ns
Minimum Off Time	T_{OFFMIN}	T_A = 25 °C	--	300	--	ns
Softstart						
Internal SS Time	Tss	Internal Soft Start	1.1	1.6	2.1	ms
Power OK Indication						
POK threshold	V_{THPOK}	POK in from lower	82.5	85	87.5	%
		POK in from higher	116.5	119	121.5	%
		POK hysteresis	2.5	5	7.5	%
POK sink Current	I_{POKMAX}	POK = 0.5V	5	12	--	mA
POK Delay	T_{POKDEL}	Delay for POK in	350	510	670	us
Logic threshold and setting conditions						
EN0 Voltage	V_{EN0}	Shutdown	--	--	0.4	V
EN0 Voltage	V_{EN0}	Enable, VCLK = off	0.8	--	1.6	V
EN0 Voltage	V_{EN0}	Enable, VCLK = on	2.4	--	--	V
Logic threshold and setting conditions						
EN0 Current		V_{EN0} = 0.4V	0.8	1.1	1.4	uA
EN1, EN2	V_{ENx}	Shutdown	350	400	450	mV

Electrical Characteristics

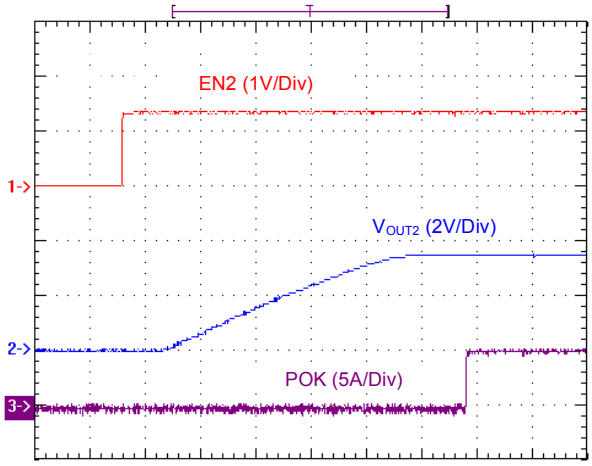
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Logic threshold and setting conditions						
EN1, EN2	V_{ENx}	Hysteresis	10	30	60	mV
TON Logic Setting Voltage	V_{TON}	200kHz/250kHz	--	--	1.5	V
		245kHz/305kHz	1.9	--	2.1	V
		300kHz/375kHz	2.7	--	3.6	V
		365kHz/460kHz	4.7	--	--	V
SKIP Logic Setting Voltage	V_{SKIP}	PWM only	--	--	1.5	V
		Auto Skip	1.9	--	2.1	V
		Out of Audio Auto Skip	2.7	--	--	V
Protection: Current Sense						
ENx Source Current	I_{EN}	V_{ENx} = 920mV, TA= 25 °C	9.2	10	10.8	uA
ENx Current Temp. Coef	TC_{IEN}	On the basis of 25 °C	--	4500	--	ppm /°C
OCP Comp. Offset	V_{OCLoff}	(($V_{ENx-GND}$-0.2)/9 -$V_{GND-LLx}$) Voltage, $V_{ENx-GND}$ = 920mV	-5	0	5	mV
Maximum OCL setting	V_{OCLmax}	V_{ENx} = 5V	185	205	225	mV
Zero cross detection comparator Offset	V_{ZC}	$V_{GND-LLx}$ voltage	-5	0	5	mV
Current limit threshold setting range	V_{TRIP}	$V_{ENx-GND}$ Voltage	0.515	--	2	V
Protection: UVP & OVP						
OVP Trip Threshold	V_{OVP}	OVP detect	110	115	120	%
OVP Prop Delay	T_{OVPDEL}	UVP detect	--	2.0	--	us
Output UVP Trip Threshold	V_{UVP}	Hysteresis	55	60	65	%
Output UVP Prop Delay	T_{UVPDEL}		--	10	--	%
Output UVP Enable Delay	T_{UVPEN}		25	32	40	us
UVLO						
LDO5 UVLO Threshold	V_{UVLDO5}	Wake up	4.1	4.2	4.3	V
		Hysteresis	0.22	0.32	0.42	V
LDO3 UVLO Threshold	V_{UVLDO3}	Shutdown	--	VO2-1	--	V
Thermal Shutdown						
Thermal SDN Threshold	T_{SDN}	Shutdown temperature	--	150	--	°C
		Hysteresis	--	10	--	°C

Typical Operation Characteristics

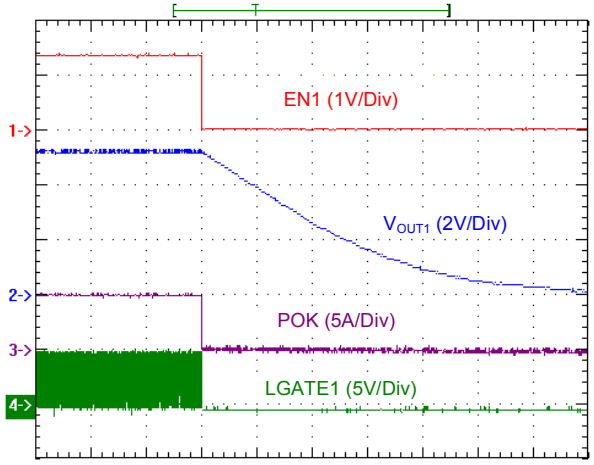
5-V Turn On Waveforms



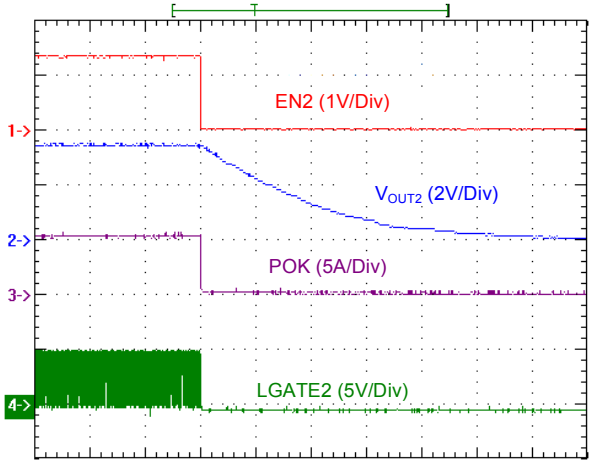
3-V Turn On Waveforms



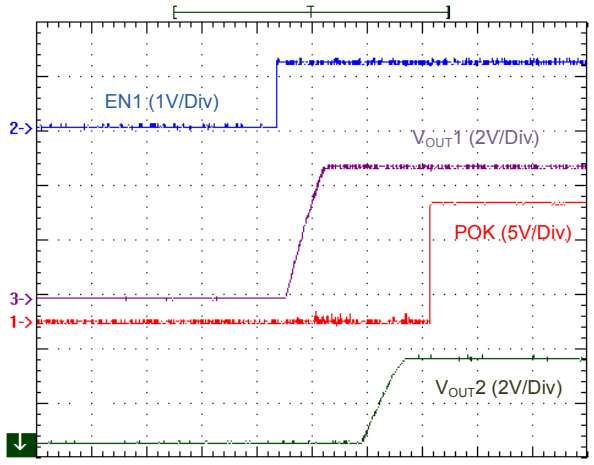
5-V Turn Off Waveforms



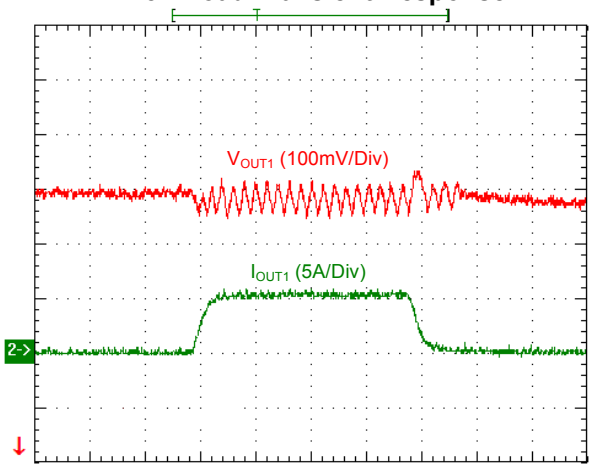
3-V Turn Off Waveforms



Power Sequence

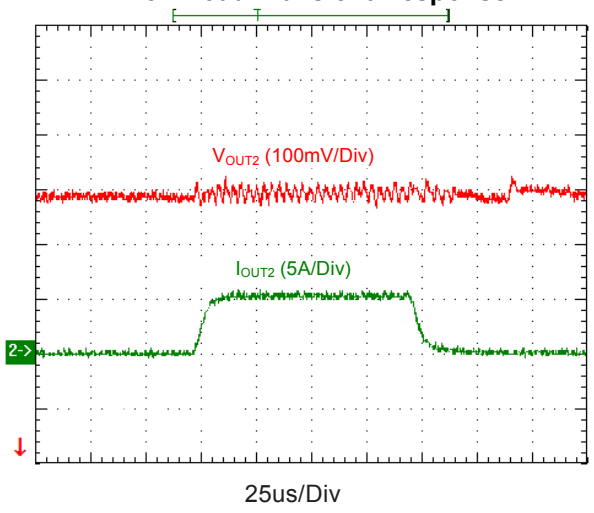


5V Load Transient Response

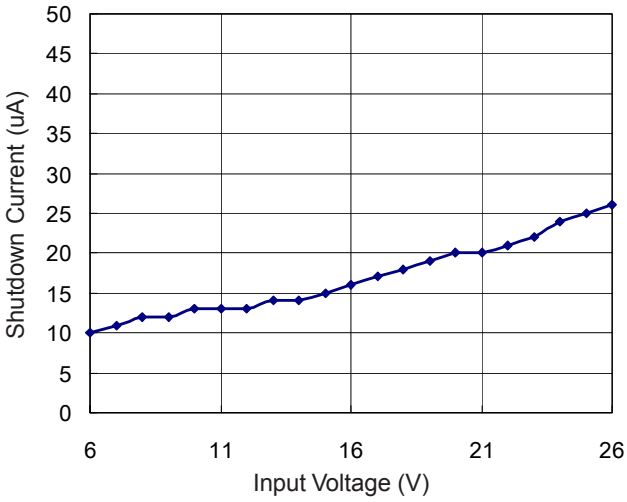


Typical Operation Characteristics

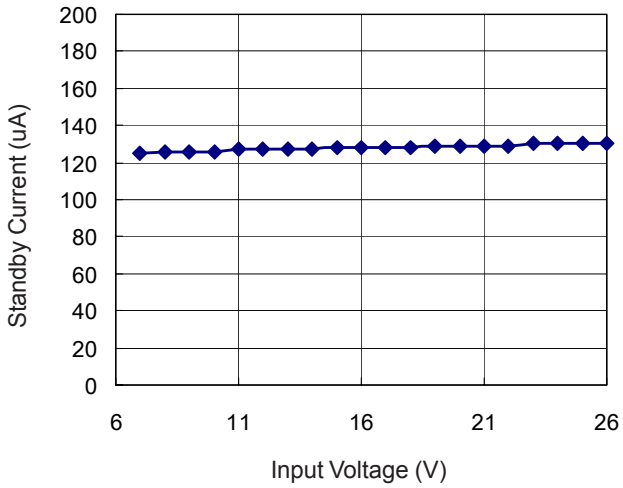
3V Load Transient Response



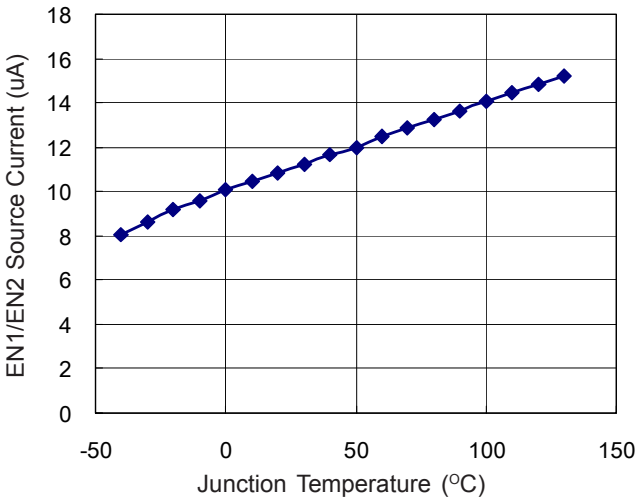
Shutdown Current vs. Input Voltage



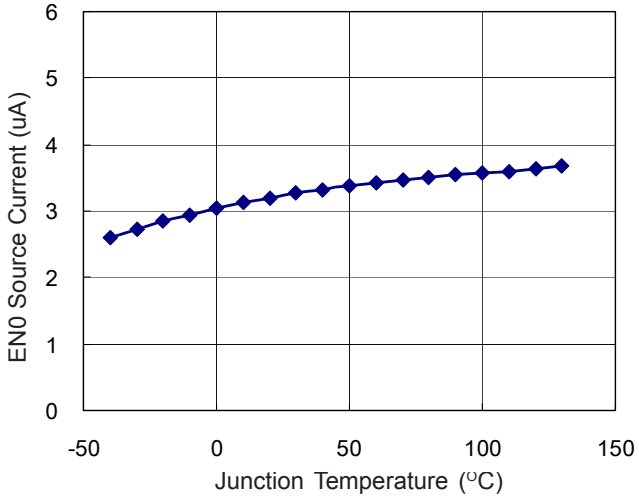
Standby Current vs. Input Voltage



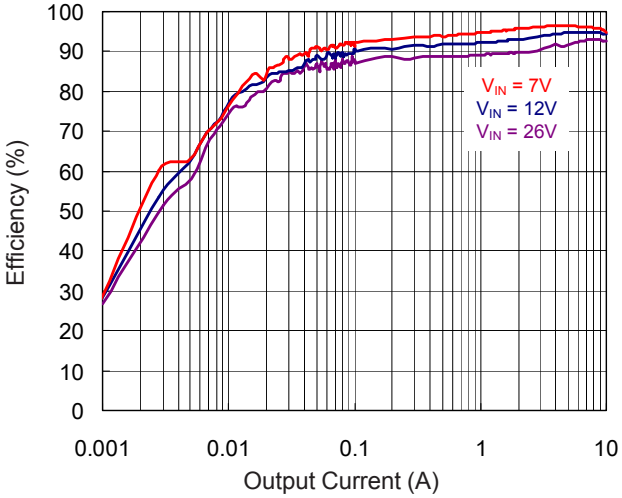
EN1/EN2 Current vs. Temperature



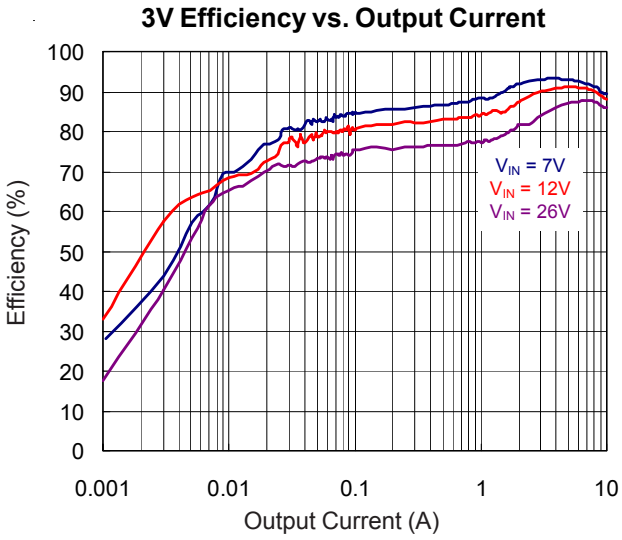
EN0 Current vs. Temperature



5V Efficiency vs. Output Current



Typical Operation Characteristics



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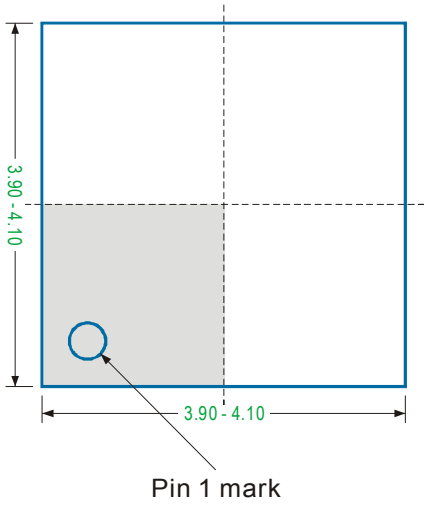
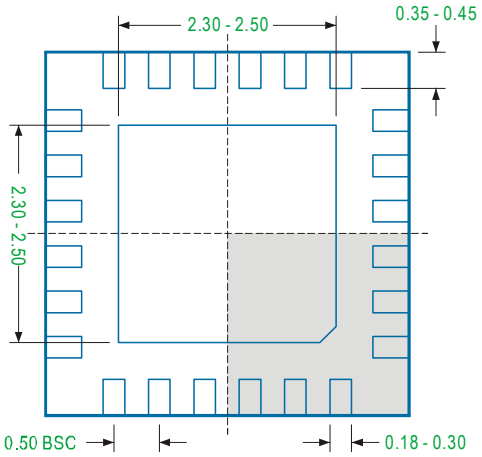
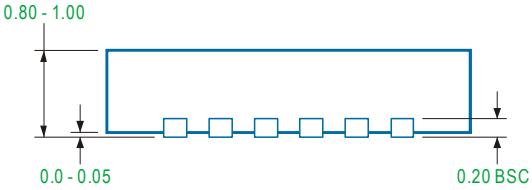
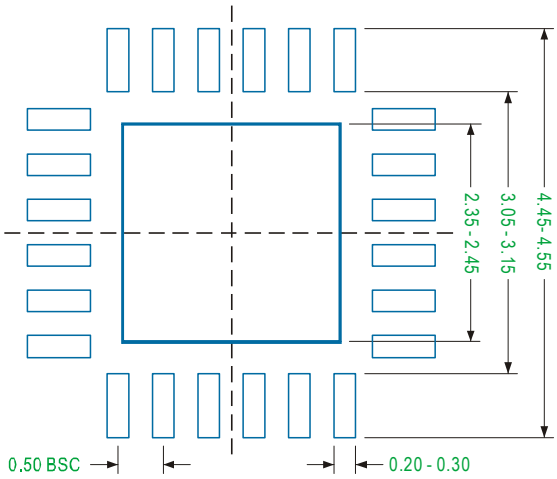
Package Information





Bottom View - Exposed Pad





Recommended Solder Pad Pitch and Dimensions

Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions no not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.