Compact Dual-Phase Synchronous-Rectified Buck Controller

General Description

The uP6205 is a compact dual-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high power applications. This part is capable of delivering up to 60A output current owing to its embedded bootstrapped drivers that support 12V + 12V driving capability. The uP6205 features configurable gate driving voltage for maximum efficiency and optimal performance. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to internal 0.6V or external reference voltage from 0.4V to 2.5V. The uP6205 adopts lossless $R_{DS(ON)}$ current sensing technique for channel current balance and over current protection.

A MODE pin programs single- or dual- phase operation making the uP6205 ideally suitable for dual power input applications such as PCIE interfaced graphic cards. When programmed as automatic mode, the uP6205 operates in single phase at light load condition and maintains high efficiency over a wide range of the output current.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation phase, and quick response to step load transient. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part is available in spacing-saving VQFN4x4-24L or VQFN3x3-16L package.

Features

- **Operate with 4.5V ~13.2V Supply Voltage**
- **Support Single- and Two- Phase Operation**
- **±2.0% Over Line Voltage and Temperature**
- **Simple Single-Loop Voltage-Mode Control**
- **12V Bootstrapped Drivers with Internal Bootstrap Diode**
- **Lossless $R_{DS(ON)}$ Current Sensing**
- **Adjustable Operation Frequency form 50kHz to 1MHz Per Phase**
- **External Compensation**
- **Adjustable Over Current Protection**
- **Adjustable Soft Start**
- **VQFN4x4 - 24L or VQFN3x3 - 16L Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

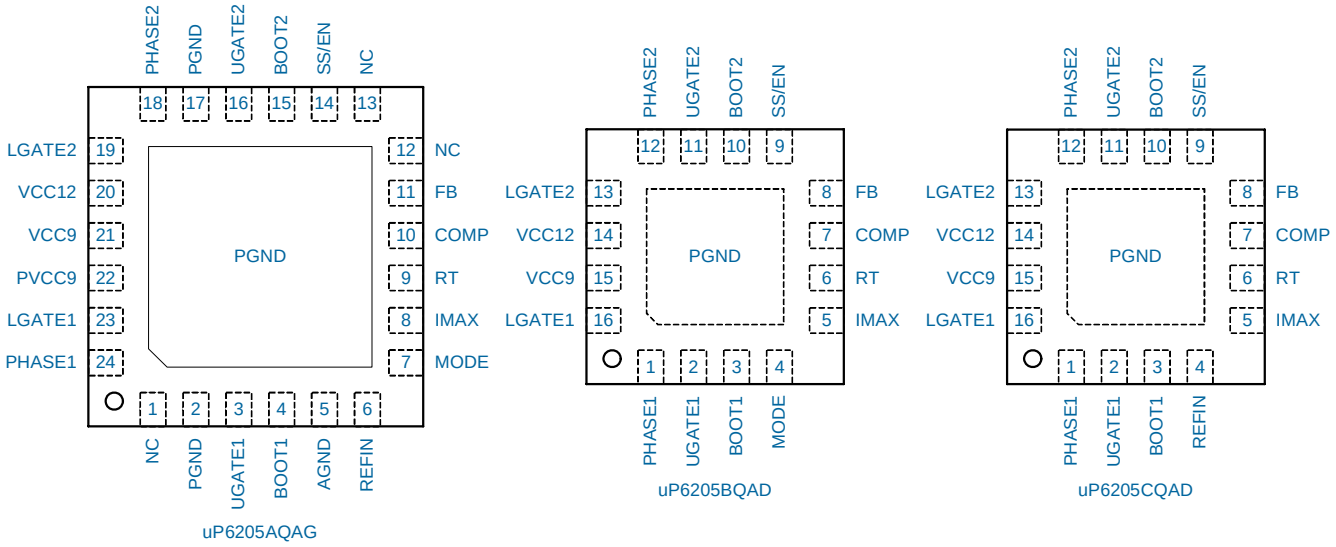
- **Middle-High End GPU Core Power**
- **High End Desktop PC Memory Core Power**
- **Low Output Voltage, High Power Density DC-DC Converters**
- **Voltage Regulator Modules**

Ordering Information

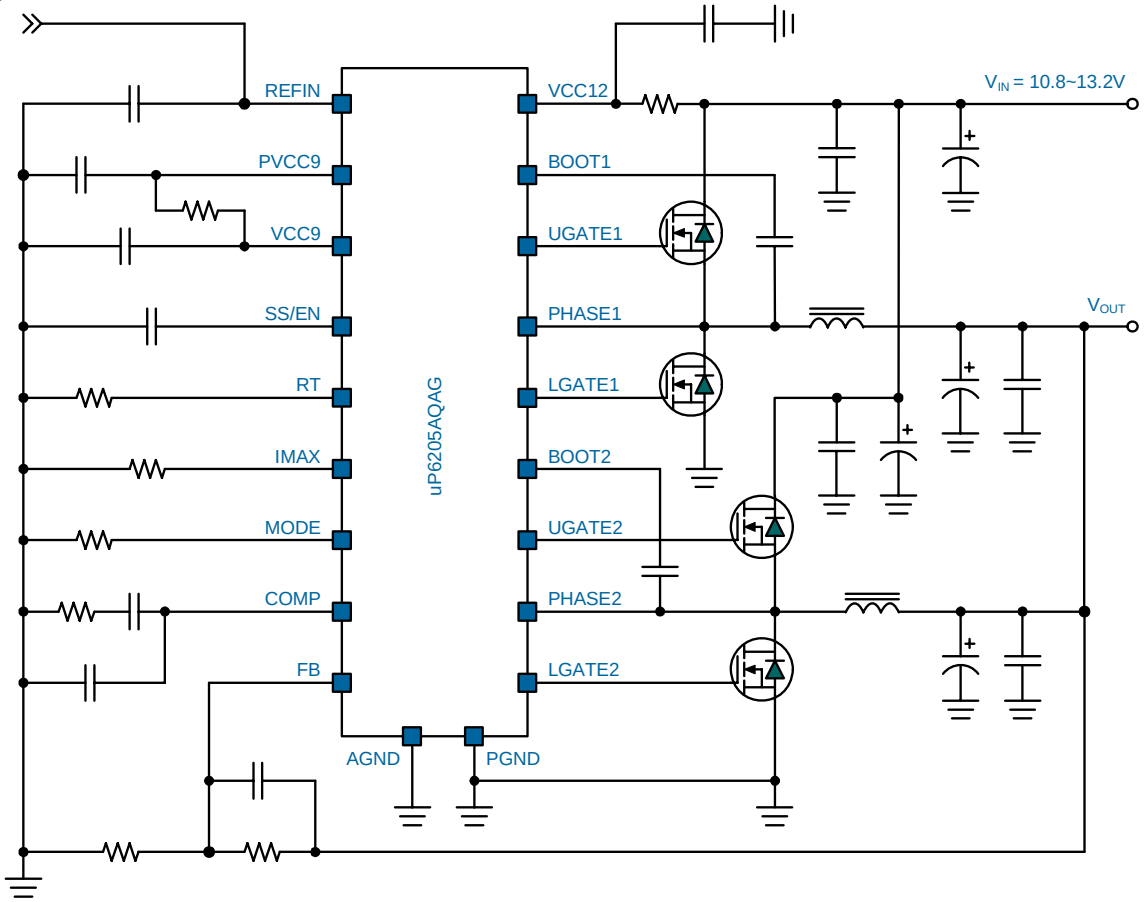
Order Number	Package Type	Remark
uP6205AQAG	VQFN4x4 - 24L	
uP6205BQAD	VQFN3x3 - 16L	Without REFIN Pin
uP6205CQAD	VQFN3x3 - 16L	Without MODE Pin

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 and RoHS requirements. They are 100% matte tin (Sn) plating and suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



Typical Application Circuit



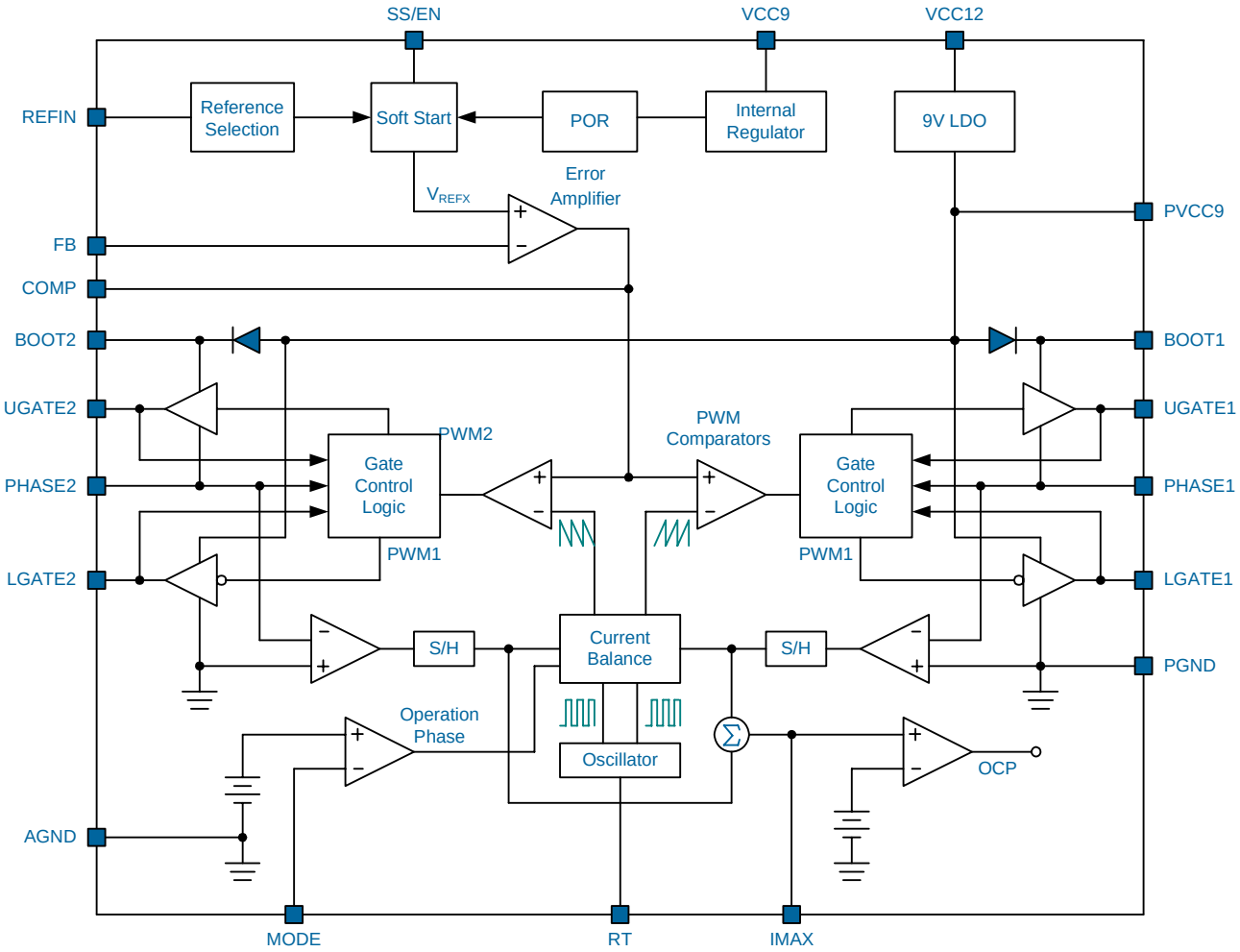
Functional Pin Description

No.	Name	Pin Function
1, 12, 13	NC	**Not Internally Connected.**
2, 17	PGND	**Power Ground for the IC.** These pins are ground returns for the gate drivers. Tie these pins to the ground island/plane through the lowest impedance connection available.
3	UGATE1	**Upper Gate Driver Output for Channel 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
4	BOOT1	**Bootstrap Supply** for the floating upper gate driver of channel 1. Connect the bootstrap capacitor C_{BOOT} between BOOT1 pin and the PHASE1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
5	AGND	All voltages levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.
6	REFIN	**External Reference Input.** This is the input pin of external reference voltage. If external reference voltage is not available, let this pin open for internal 0.6V reference.
7	MODE	**Operation Phase Control Input.** Connect a resistor R_{MODE} from this pin to GND to set the threshold current level for single and dual phase operations. The uP6205 operates in dual phase if the output current is higher than the threshold current level; in single phase if the output current is lower than the threshold current level; see the related sections for detail. Tie this pin to GND for always single phase operation. Let this pin open for always dual phase operation. Both upper and lower switches of Phase2 are turned off when operating in single phase.
8	IMAX	**Output Current Indication.** Connect this pin to ground with a resistor to set the output over current protection level.
9	RT	**Operation Frequency Setting.** Connect a resistor between this pin and AGND to set the operation frequency.
10	COMP	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparators. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
11	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage.
14	SS/EN	**Soft Start Output.** Connect a capacitor from this pin to AND to set the soft start interval. Pulling low this pin down to 0.5V will shut down the uP6205.
15	BOOT2	**Bootstrap Supply** for the floating upper gate driver of channel 2. Connect the bootstrap capacitor between BOOT2 pin and the PHASE2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET.
16	UGATE2	**Upper Gate Driver Output for Channel 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
18	PHASE2	**Switch Node for Channel 2.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
19	LGATE2	**Lower Gate Driver Output for Channel 2.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.

Functional Pin Description

No.	Name	Pin Function
20	VCC12	**Supply Voltage.** This pin is the input pin of the internal 9V LDO, providing current for PVCC9 and VCC9 pin. Place a minimum 1uF ceramic capacitor physically near the pin to locally bypass the supply voltage.
21	VCC9	**Supply Input.** This pin receives a well supply voltage form 4.5V to 13.2V and provides bias current for the internal control circuit. Bypass this pin with a minimum 1uF ceramic capacitor physically near it.
22	PVCC9	**Supply Input.** This pin is the output of the internal 9V LDO regulator. This pin provides current for lower gate drivers and bootstrap circuit for upper drivers.
23	LGATE1	**Lower Gate Driver Output for Channel 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turn off.
24	PHASE1	**Switch Node for Channel 1.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
Exposed Pad PGND		**Power Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Block Diagram



Functional Description

The uP6205 is a compact dual-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high power applications. This part is capable of delivering up to 60A output current owing to its embedded bootstrapped drivers that support 12V + 12V driving capability. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to internal 0.6V reference voltage or external reference voltage from 0.4V to 2.5V. The uP6205 adopts $R_{DS(ON)}$ current sensing technique for channel current balance, and over current protection.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include internal soft start, adjustable operation phase number and quick response to step load transient. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part is available in VQFN4x4 - 24L or VQFN3x3 - 16L packages.

Internal 9V and 5V LDO Regulators

The uP6205 integrates 9V and 5V LDO regulators for gate drivers and internal control circuitry respectively as shown in Figure 1.

The 9V LDO receives input voltage at VCC12 pin and outputs a regulated voltage at PVCC9 pin for the lower gate drivers and the bootstrap circuit for the upper gate drivers, providing flexible gate driving voltage for maximum efficiency and optimal performance. When driving with 9V gate voltage, the converter reduces 25% power dissipation in the drivers and maintains high efficiency comparing to 12V driving voltage. This enables the uP6205 to drive MOSFETs with large input capacitors and provides up to 60A output current without overheating the controller itself.

When the VCC12 pin is left open, the VCC9 and PVCC9 pins could receive well decoupled 4.5V~13.2V voltage for gate drivers as shown in Figure 2. Since the uP6205 adopts $R_{DS(ON)}$ current sensing technique for current balance and over current protection, always consider the $R_{DS(ON)}$ with the lowest possible gate driving voltage. If the gate driving voltage is expected to be lower than 7V, special consideration should be paid to the threshold voltage of the MOSFETs.

Bootstrap diodes are embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required. However, if the VCC9 and PVCC9 pins voltage are expected to be lower than 5V, external Schottky diode is highly recommended to get highest gate driving voltage for high side MOSFET.

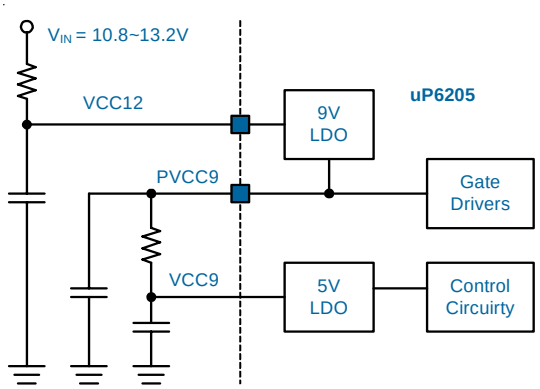


Figure 1. 9V Drive Application

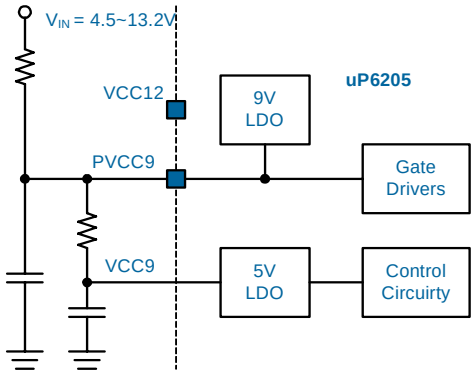


Figure 2. Bypass the Internal 9V LDO Regulator.

The VCC pin should be locally bypassed by a minimum 1uF ceramic. Place the capacitor physically near the VCC pin.

An internal linear regulator regulates VCC input to a 5VCC voltage for internal control logic circuit as shown in Figure 1 and 2. No external bypass capacitor is required for the 5VCC voltage.

Power On Reset and Initialization

The uP6205 continuously monitors VCC9 pin voltage for power on reset (POR) to ensure the supply voltage is high enough for normal operation of the device. The POR threshold level is typically 4.3V at VCC9 rising.

Reference Voltage Selection

The uP6205 features selectable internal or external reference voltage. The REFIN voltage level is checked at POR to select the desired reference voltage. Internal 0.6V reference voltage is selected if V_{REFIN} > 3.3V at POR, otherwise external reference voltage would be selected.

Functional Description

Once selected, the reference source is fixed and can only be programmed at next POR.

The REFIN sources a 1uA current and pulls its voltage to 5V if this pin is left open when POR is granted. This selects the internal 0.6V reference voltage. If the external reference voltage is higher than 2.5V before POR, it may cause uP6205 to select internal 0.6V reference voltage and should be avoided.

The REFIN pin is not available for uP6205BQBD. It supports only internal 0.6V reference voltage.

Oscillation Frequency Programming

A resistor R_{RT} connected to RT pin programs the oscillation frequency as:

$$f_{OSC} = 200 \times (\frac{30(k\Omega)}{R_{RT}(k\Omega)})^{0.92} \quad (kHz)$$

Figure 3 shows the relationship between oscillation frequency and R_{RT}.

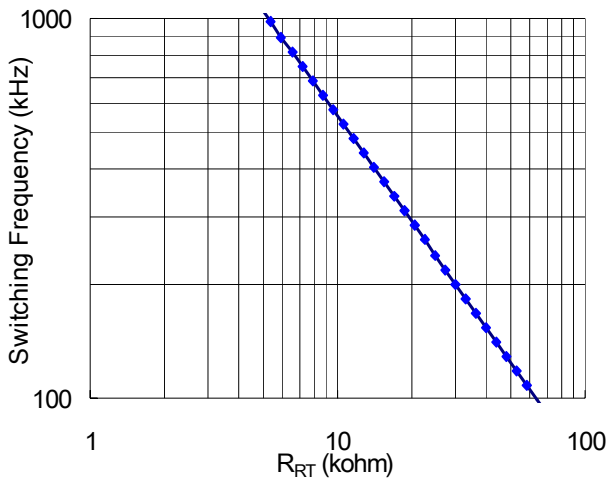


Figure 3. Switching Frequency vs. R_{RT}.

Soft Start

Once POR releases, the uP6205 initiates its soft start cycle. Figure 4 shows the softstart cycle with external reference voltage. A 10uA current charges the soft start capacitor C_{SS} making its voltage V_{SS} linearly ramp up. The V_{SS} clamps reference voltage V_{REF} with a MOSFET threshold voltage at non-inverting input of the error amplifier. Accordingly, the output voltage will softly ramp up and draw minimum inrush current from the power bus.

The uP6205 features pre-bias start-up capability. If the output voltage is pre-biased with a voltage, say V_{BIAS}, that accordingly makes V_{FB} higher than reference voltage ramping V_{REF}. The error amplifier keeps V_{COMP} lower than the valley of the sawtooth waveform and makes PWM comparators output low until the ramping V_{REF} catches up the feedback voltage. The uP6205 keeps both upper and lower MOSFETs off until the first pulse takes place.

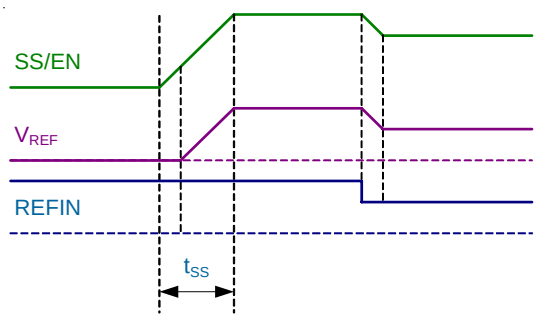


Figure 4. Timing Diagram of Soft Start Interval.

The uP6205 claims soft start end when V_{REF} catches up $V_{REFIN.}$ The total soft start time with external reference voltage is about

$$t_{SS} = \frac{C_{SS}(V_{REFIN} + 0.8V)}{10uA}$$

where 0.8V accounts for the delay time caused by the MOSFET threshold voltage. When external reference voltage changes, the slew rate of V_{REF} is also limited by the soft start mechanism. Consequently, this results in a smooth output voltage transition during external reference voltage change. The soft start also acts as the timer during OCP and UVP hiccups as described in the later sections.

Channel Current Sensing

The uP6205 extracts phase currents for current balance and over current protection by parasitic on-resistance of the lower switches when turn on as shown in Figure 5.

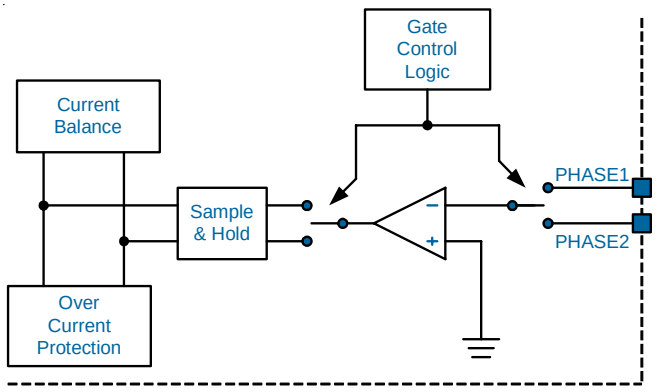


Figure 5. $R_{DS(ON)}$ Current Sensing Scheme

The GM amplifier senses the voltage drop across the lower

Functional Description

switch and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{CSX} = 3.3 \times I_{LX} \times R_{DS(ON)} \times 10^{-4} + 6.6uA$$

where I_{LX} is the phase X current in Ampere, $R_{DS(ON)}$ is the on-resistance of low side MOSFET in mΩ, 6.6uA is a constant to compensate the offset of the current sensing circuit. **Note that the valley inductor current is sampled and held.** The sampled and held is the averaged inductor current minus half of inductor ripple current:

$$I_{LX\_SH} = I_{LX\_AVG} - 1/2 \times \Delta I_{LX}$$

One half of the summation of the sampled and held current signal (I_{CS1} +I_{CS2})/2 is injected to the IMAX pin, that results in a voltage V_{IMAX} across the resistor R_{IMAX} connecting IMAX and AGND.

$$V_{IMAX} = \frac{(I_{CS1} + I_{CS2})}{2} \times R_{IMAX}$$

$$= \frac{[3.3 \times (I_{L1\_SH} + I_{L2\_SH}) \times R_{DS(ON)} \times 10^{-4} + 13.2uA]}{2} \times R_{IMAX}$$

Take I_{LX} = 20A, ΔI_{LX} = 4A, $R_{DS(ON)}$ = 6mΩ , and R_{IMAX} = 20kΩ for example, V_{IMAX} is calculated as:

$$V_{IMAX} = \frac{[3.3 \times (20-4)A \times 2 \times 6m\Omega \times 10^{-4} + 13.2uA]}{2} \times 30k\Omega$$

$$= 1.27V$$

Over Current Protection

V_{IMAX} is compared with a 3.0V reference voltage for over current protection. If V_{IMAX} is higher than 3.0V, OCP is activated. Take above setting for example, the output current for OCP is calculated as:

$$3.0V = \frac{[3.3 \times (I_{OUT} - 4)A \times 6m\Omega \times 10^{-4} + 13.2uA]}{2} \times 30k\Omega$$

$$I_{OUT} = 98.3A$$

The uP6205 features hiccup and shutdown mode OCP. If OCP takes place after soft start end, the uP6205 turns off both upper and lower MOSFETs and discharges the C_{SS} with a constant current of 10uA. When V_{SS} touches down 0.4V, the uP6205 initiates another soft start cycle. The uP6205 shuts down after 3 times hiccups. If the OCP takes place during soft start cycle, the uP6205 turns off both upper and lower MOSFETs but keeps charging the C_{SS} with a constant current of 10uA until the soft start end. The shutdown status can only be reset by POR function. Figure 6, and Figure 7 illustrate the OCP behaviors during soft start and after soft start end respectively.

Note that on-resistance of a MOSFET is highly dependent of gate voltage and temperature. Always consider the highest temperature and lowest gate voltage.

Note that the valley value of the inductor is sampled and held just before the lower switch is to turn off. The ripple current of the inductor should be considered when calculating over current protection level.

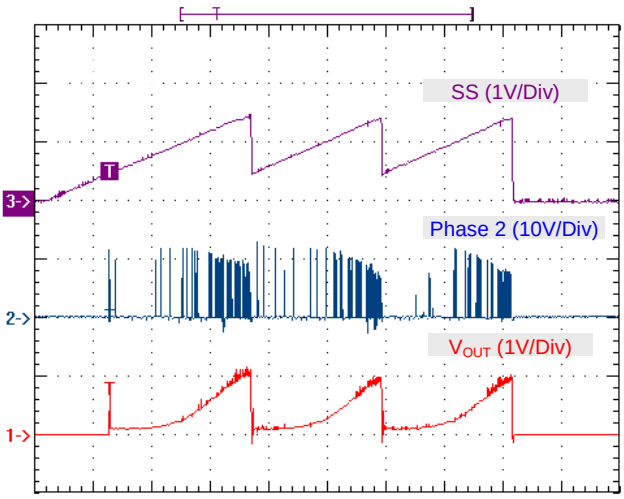


Figure 6. OCP during Soft Start

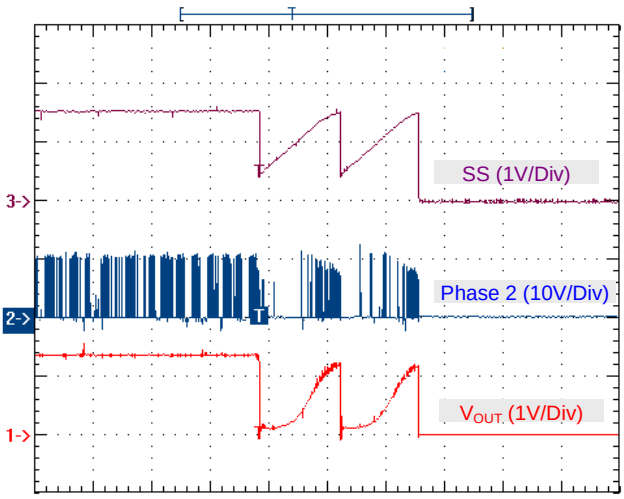


Figure 7. OCP after Soft Start End.

Current Balance

The uP6205 fine tunes the duty cycle of each channel for current balance according to the sensed inductor current signals as shown in Figure 8. If the current of channel 1 is smaller than the current of channel 2, the uP6205 increases the duty cycle of the corresponding phase to increase its phase current accordingly, vice verse.

Functional Description

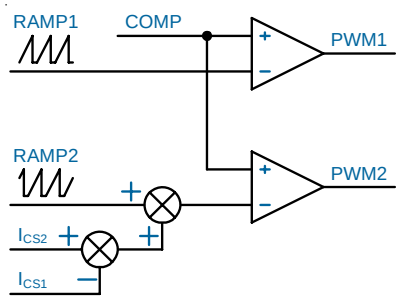


Figure 8. Current Balance Scheme of uP6205

Automatic Phase of Operation Selection

The uP6205 features automatic phase of operation selection according to load current. A current I_{MODE} flows through the resistor R_{MODE} connecting MODE pin and AGND.

$$I_{MODE} = 0.6V / R_{MODE}$$

If the I_{IMAX} is smaller than 2/5 of I_{MODE}, the uP6205 operates in single phase by turning off phase 2. If the I_{IMAX} is higher than 3/5 of I_{MODE}, the uP6205 operates in dual phase.

Take ΔI_{LX} = 4A, $R_{DS(ON)}$ = 6mΩ , and R_{MODE} = 30kΩ for example, I_{MODE} is calculated as 0.6V/30kΩ = 20uA. The threshold level of output current for entering single phase operation is calculated as:

$$\frac{2 \times I_{MODE}}{5} = \frac{[3.3 \times (I_{OUT} - 4)A \times 6m\Omega \times 10^{-4} + 13.2uA]}{2}$$

$$I_{OUT} = 5.4A$$

The threshold level of output current for entering dual phase operation is calculated as:

$$\frac{3 \times I_{MODE}}{5} = \frac{[3.3 \times (I_{OUT} - 2)A \times 6m\Omega \times 10^{-4} + 6.6uA]}{2}$$

$$I_{OUT} = 10.8A$$

Note that when operated in single phase, the rated current is reduced to ***80 percents*** of normal level. Continuous demanding high current may damage the converter.

Manual Phase of Operation Selection

The uP6205 supports manual selecting single- or dual-phase operation. If I_{MODE} is higher than 150uA, the uP6205 operates in forced single phase mode. If I_{MODE} is smaller than 4uA, the uP6205 operates in forced dual phase mode. This feature is important for PCIE interfaced graphic cards where neither bus power nor external power is capable of delivering full load current. Configure the converter as shown in Figure 9. Power the phase 1 converter by PCIE bus power and power the phase 2 converter by external power. If the external power code is not plugged into the socket, the External Power Detection, I_{MODE} = 0.6V/3kohm >150uA and the uP6205 operates in single phase mode. The uP6205 could provide limited current to GPU for required operation when external power is not plugged.

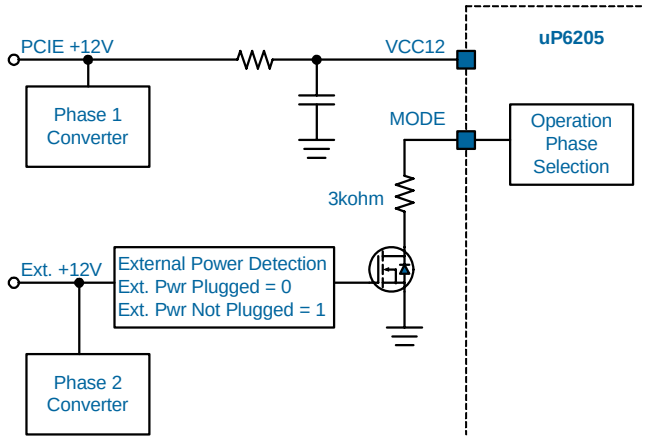


Figure 9. Single/Two Phase Operation

Two-phase operation will make the phase 2 converter act like a boost converter if the external power is not available, boosting the output voltage to the input voltage. The relationship between input voltage and output voltage is governed by conventional boost converter equation. Offset of the current balance function may make the duty cycle of phase 2 converter smaller than that of phase 1 converter. This results in external power higher than 15V that may damage the input capacitors and other devices. Figure 9 configuration turns off phase 2 converter when the external power is not available, thus eliminates the possibility of over voltage on input capacitors and other devices of the phase 2 converter.

Note that when operating in forced single phase mode, the uP6205 starts up with single phase operation. When operating in automatic selection mode, the uP6205 starts up with dual phase operation, no matter what level the load current is. The mode selection is enabled only after the uP6205 claims soft start end.

The MODE pin is not available for uP6205CQBD. It supports only two phase operation.

Absolute Maximum Rating

Supply Input Voltage, VCC12 (Note 1) ---------- -0.3V to +15V
PHASE to GND
DC ---------- -5V to 15V
< 200ns ---------- -10V to 30V
BOOT to PHASE ---------- -0.3V to +15V
UGATE to PHASE ---------- -0.3V to (BOOT - PHASE +0.3V)
PVCC9, VCC9 ---------- -0.3V to VCC12 + 0.3V
LGATE ---------- -0.3V to + (PVCC9 + 0.3V)
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN4x4 - 24L θ_{JA} ---------- 40°C/W
VQFN3x3 - 16L θ_{JA} ---------- 60°C/W
VQFN4x4 - 24L θ_{JC} ---------- 3°C/W
VQFN3x3 - 16L θ_{JC} ---------- 5°C/W
Power Dissipation, P_D @ TA = 25°C
VQFN4x4 - 24L ---------- 2.5W
VQFN3x3 - 16L ---------- 1.67W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC12} ---------- 10.8V to 13.2V

Electrical Characteristics

(VCC12 = 12V, VCC9 = PVCC = 9V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Input Voltage	V_{CC12}		10.8	--	13.2	V
Bias Voltage	V_{CC9}		4.5	--	13.2	V
Regulated Bias Voltage	V_{PCC9}	V_{IN} = 12V, V_{FB} = 0.7V, No Switching	8	9	10	V
Supply Current	I_{CC12}	UGATE and LGATE Open; Switching	--	5	--	mA
Quiescent Supply Current	I_{CC9_Q}	V_{FB} = 0.7V, No Switching	--	4	--	mA
VCC POR Threshold	V_{CC9RTH}	V_{CC9} Rising.	4.2	4.3	4.4	V
VCC POR Hysteresis	V_{CC9HYS}		--	0.2	--	V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Oscillator						
Free Running Frequency	f_{OSC}	R_{RT} = 30kΩ	180	200	220	kHz
Frequency Variation		R_{RT} = 30kΩ	-10	--	10	%
Frequency Range			50	--	1000	kHz
Maximum Duty Cycle			75	80	85	%
Minimum Duty Cycle			--	0	--	%
Ramp Amplitude	ΔV_{OSC}		--	4	--	V_{P-P}
Reference Voltage						
Nominal Feedback Voltage	V_{FB}	V_{CC12} = 12V, V_{COMP} = 1.2V	0.59	0.6	0.61	V
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	60	70	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	6	10	--	MHz
Slew Rate	SR	Guaranteed by Design	3	6	--	V/us
Trans-conductance	GM	R_{LOAD} = 20kΩ	1200	1700	--	uA/V
Maximum Current (Source & Sink)	I_{COMP}	V_{COMP} = 1.6V	220	280	--	uA
Current Sense						
Current Sense Trans-conductance	GM	$\Delta I_{IMAX}/(\Delta V_{PHASE1} + \Delta V_{PHASE2})$ @ R_{IMAX} = 30kΩ	--	660	--	uA/V
Over Current Threshold	V_{IMAX}	R_{IIMAX} = 30kΩ	2.7	3.0	3.3	V
Mode Pin Voltage	V_{MODE}		--	0.6	--	V
Forced Single Phase Operation Threshold	I_{IMODE}		150	--	--	uA
Forced Dual Phase Operation Threshold	I_{IMODE}		--	--	4	uA
Gate Driver (P_{VCC9} = 12V)						
Upper Gate Source	I_{UG_SRC}	V_{BOOT} - V_{UGATE} = 6V	--	-1.5	--	A
Upper Gate Sink	R_{UG_SNK}	V_{UGATE} - V_{PHASE} = 1V	--	2	4	Ω
Lower Gate Source	I_{LG_SRC}	V_{CC} - V_{LGATE} = 6V	--	-1.5	--	A
Lower Gate Sink	R_{LG_SNK}	V_{LGATE} = 1V	--	2	4	Ω
Dead Time	T_{DT}		--	30	--	ns
Gate Driver (P_{VCC9} = 9V)						
Upper Gate Source	I_{UG_SRC}	V_{BOOT} - V_{UGATE} = 6V	--	-1.4	--	A
Upper Gate Sink	R_{UG_SNK}	V_{UGATE} - V_{PHASE} = 1V	--	2.2	--	Ω
Lower Gate Source	I_{LG_SRC}	V_{CC} - V_{LGATE} = 6V	--	-1.4	--	A
Lower Gate Sink	R_{LG_SNK}	V_{LGATE} = 1V	--	2.2	--	Ω

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Soft Start						
Soft Start Current	I_{SS}	V_{SS} = 0V	7	10	13	uA
Re-Soft Start Threshold Level	V_{SS_HICCUP}		--	0.5	--	V
Protection						
Over Temperature Protection				150		°C
Over Temperature Hysteresis				20		°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

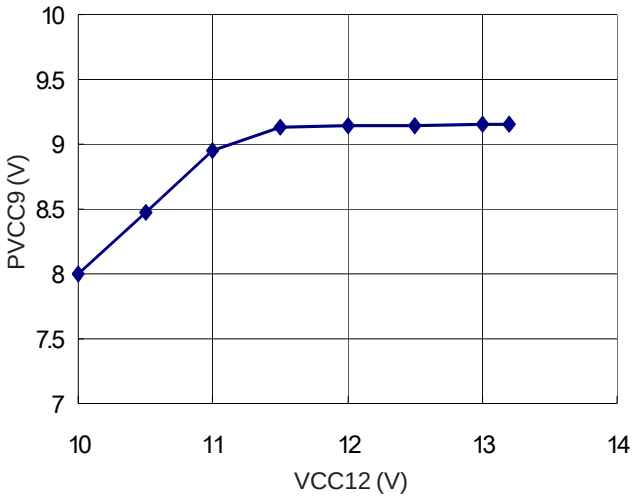
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

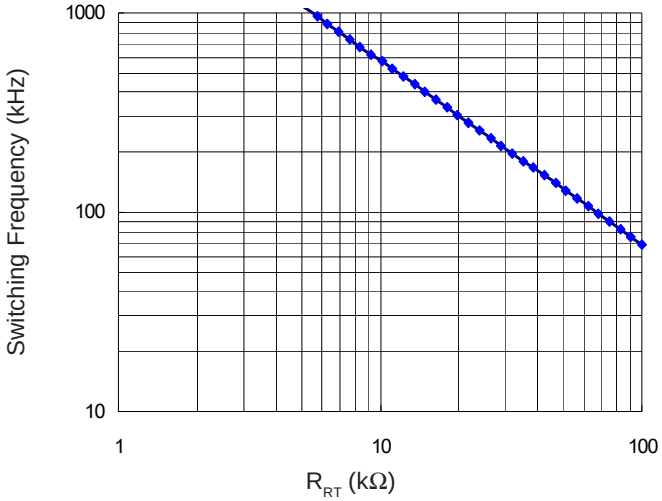
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operation Characteristics

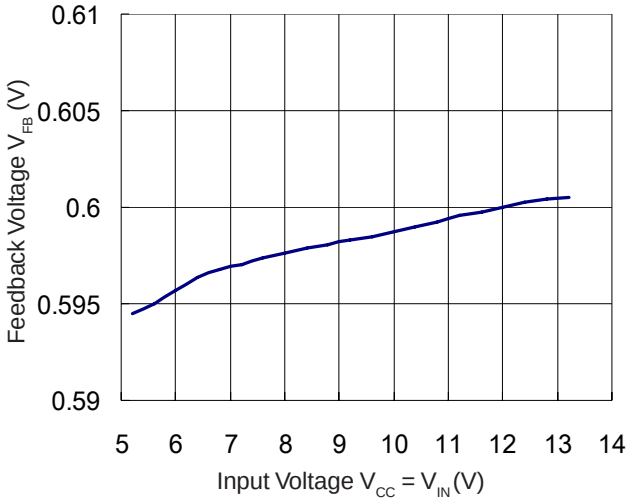
PVCC9 Line Regulation



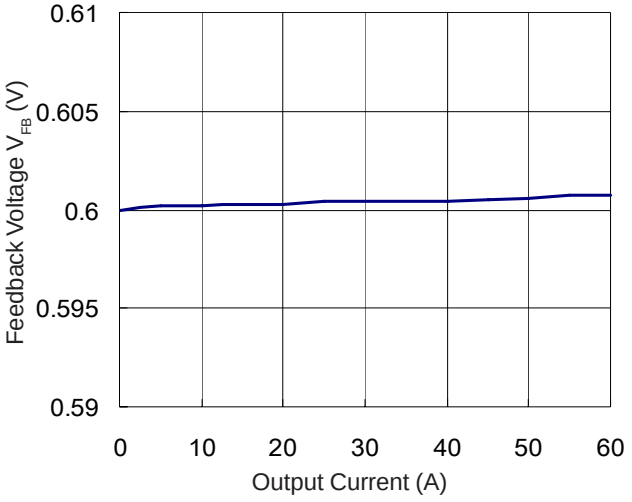
Switching Frequency vs. R_{RT}



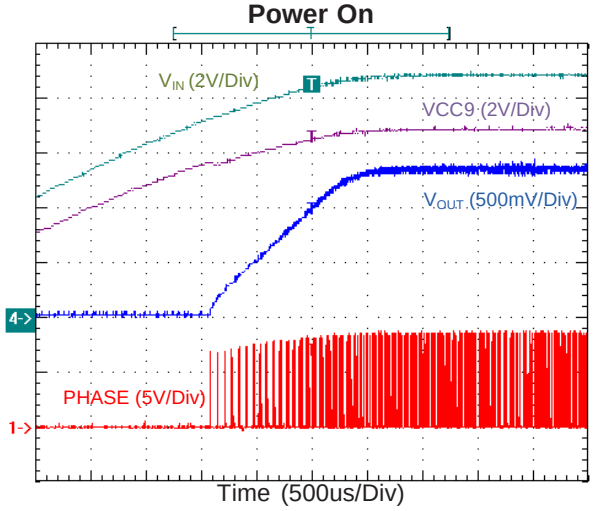
Output Voltage Line Regulation (V_{CC} = V_{IN})



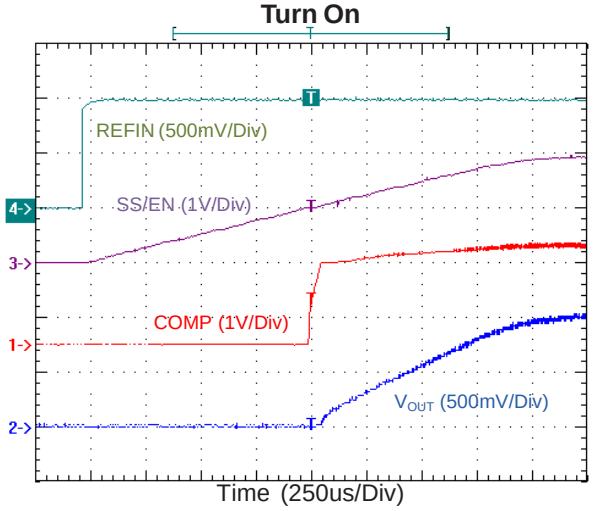
Output Voltage Load Regulation



Power On

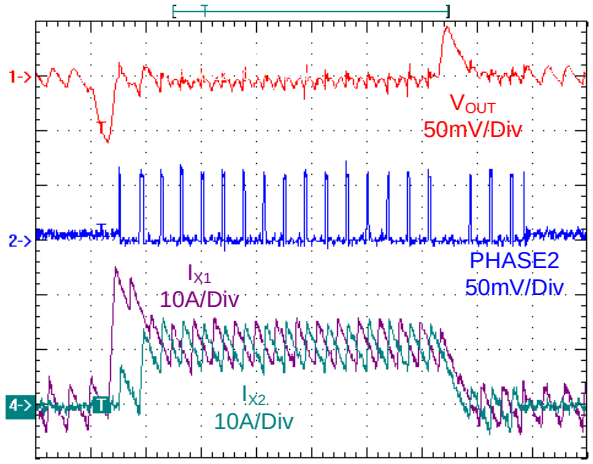


Turn On



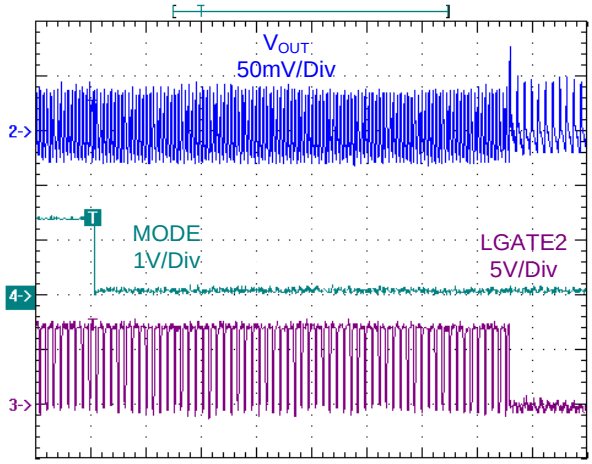
Typical Operation Characteristics

Load Transient Response



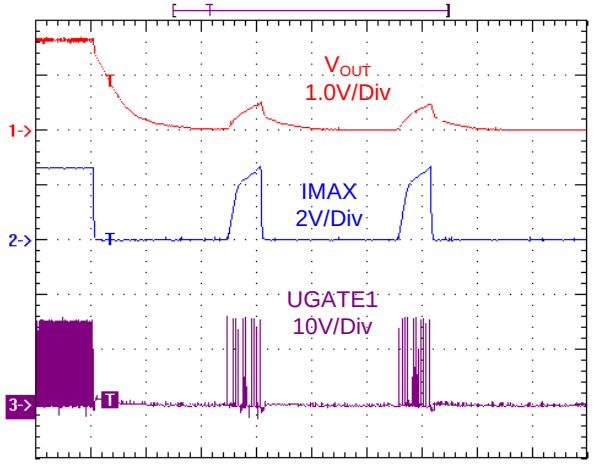
Time (10us/Div)
R_{MODE} = 30kΩ

MODE Transition



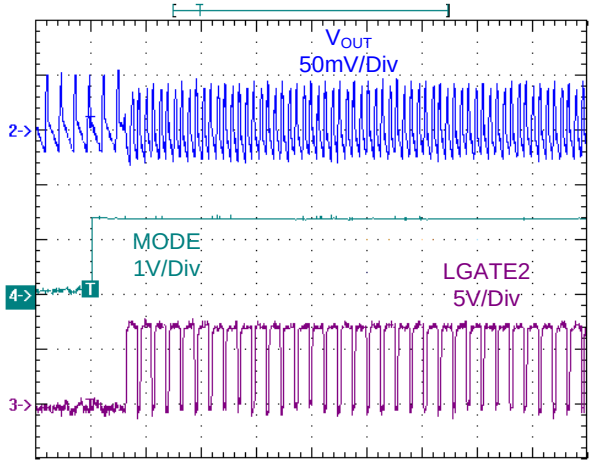
Time (10us/Div)
dual phase to single phase transition

OCP During Normal Operation



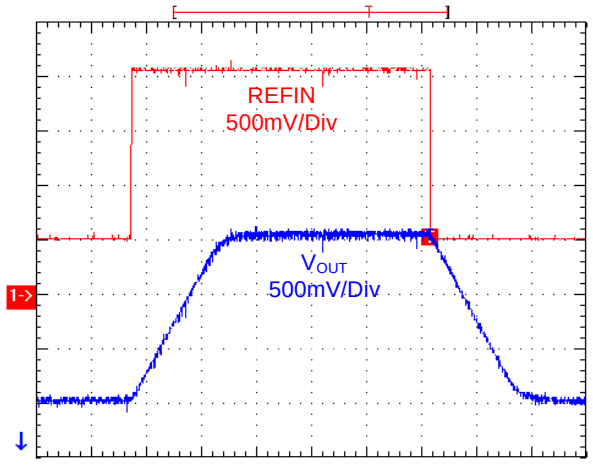
Time (250us/Div)

MODE Transition



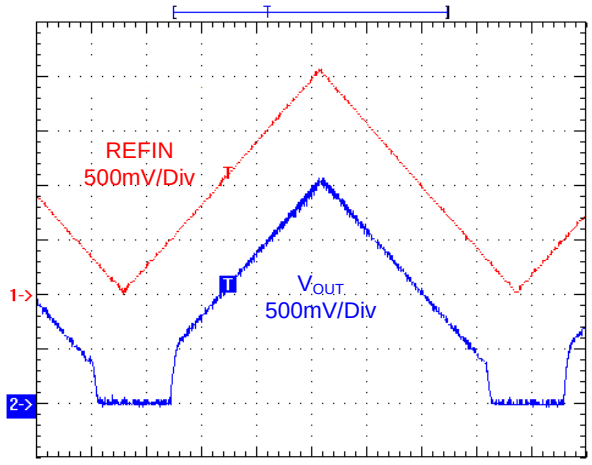
Time (5us/Div)
sigle phase to dual phase transition

REFIN Step Change



Time (1ms/Div)
REFIN 0.5V to 2.0V Step Change

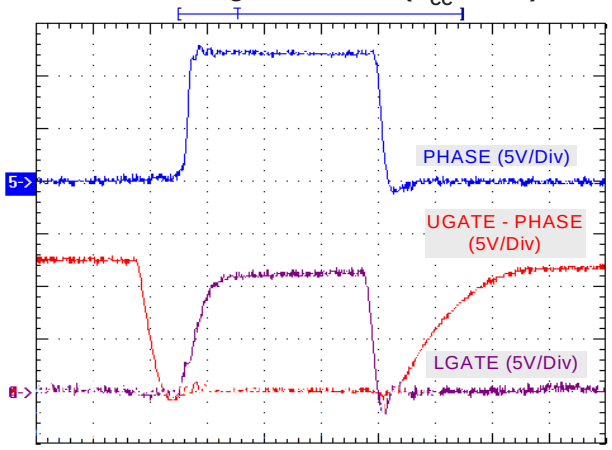
ON/OFF from REFIN



Time (5ms/Div)
REFIN 0V to 2.0V Triangle Wave

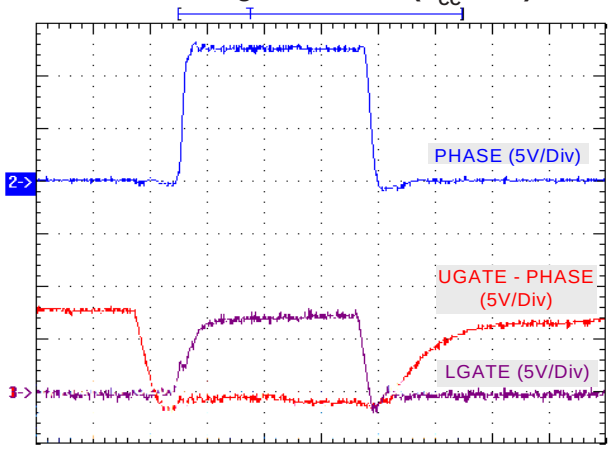
Typical Operation Characteristics

Switching Waveforms (V_{CC} = 12V)



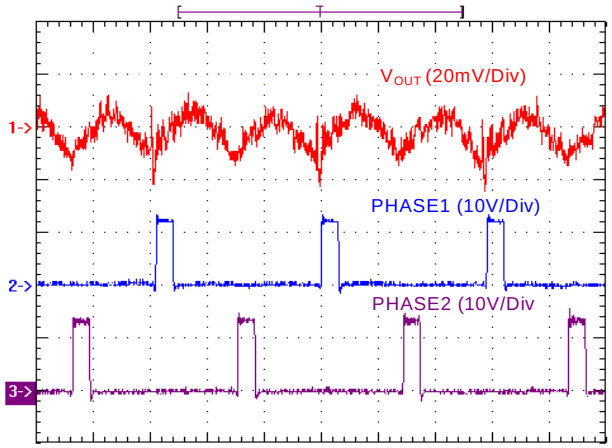
Time (100ns/Div)
V_{CC} = 12V, 20MHz bandwidth limited

Switching Waveforms (V_{CC} = 9V)



Time (100ns/Div)
V_{CC} = 8V, 20MHz bandwidth limited

Steady State Operation



Time (1us/Div)
V_{IN} = 12V, V_{OUT} = 1.2V

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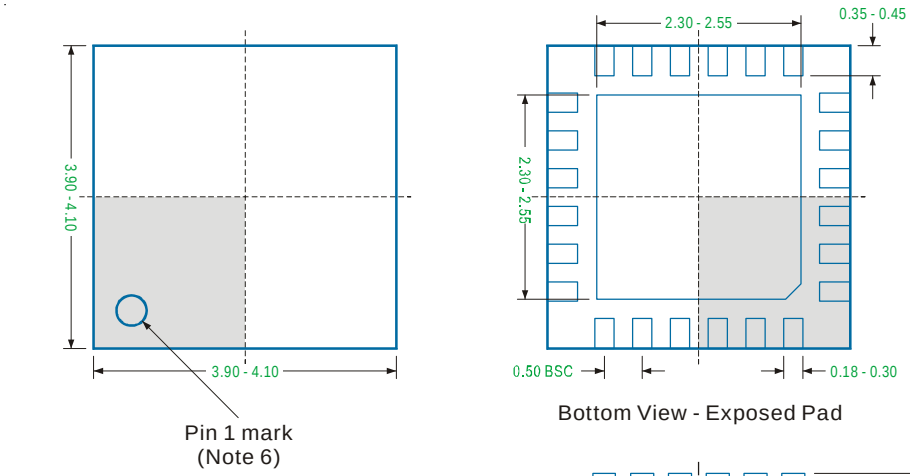
Package Information

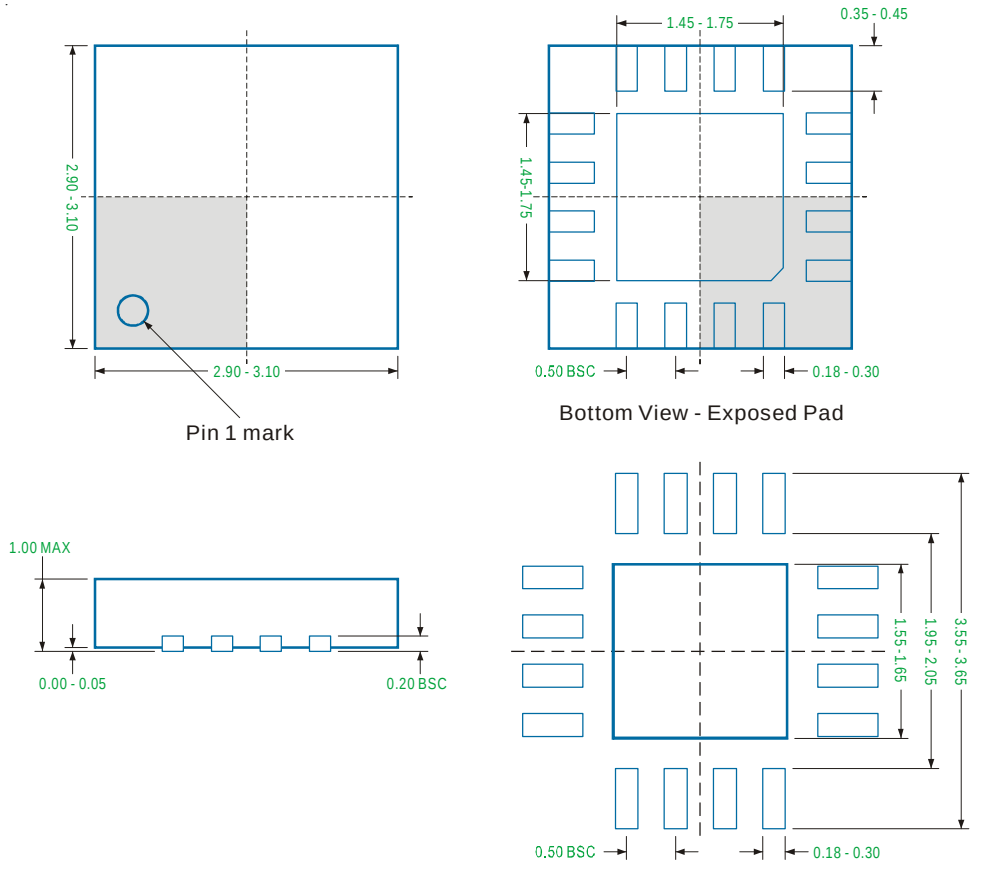
VQFN4x4-24L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

VQFN3x3-16L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.