Current-Limited, Power Distribution Switches

General Description

The uP7534 is a current limited high-side switch designed for applications where heavy capacitive loads and short-circuits are likely to be met. This device operates with inputs from 2.7V to 5.5V for both 3V and 5V systems. Its low quiescent current (25uA) and standby current (<1uA) conserve battery power in portable.

The power switch is controlled by a logic enable input and driven by an internal charge pump circuit. When the output load exceeds the current-limit threshold or a short is present, the uP7534 asserts overcurrent protection and limits the output current to a safe level by driving the power switch into saturation mode.

The uP7534 features glitch-blank fault flag that is asserted by overcurrent, overtemperature, or input undervoltage lockout. The 8ms glitch-blanking time allows momentary faults to be ignored, thus preventing false alarms to the host system.

Other features include soft-start to limit inrush current during plug-in, thermal shutdown to prevent catastrophic switch failure from high-current loads, under-voltage lockout (UVLO) to ensure that the device remains off unless there is a valid input voltage present. The uP7534 is available in SOP-8 , SOT23-5, MSOP-8, and PMSOP-8 packages.

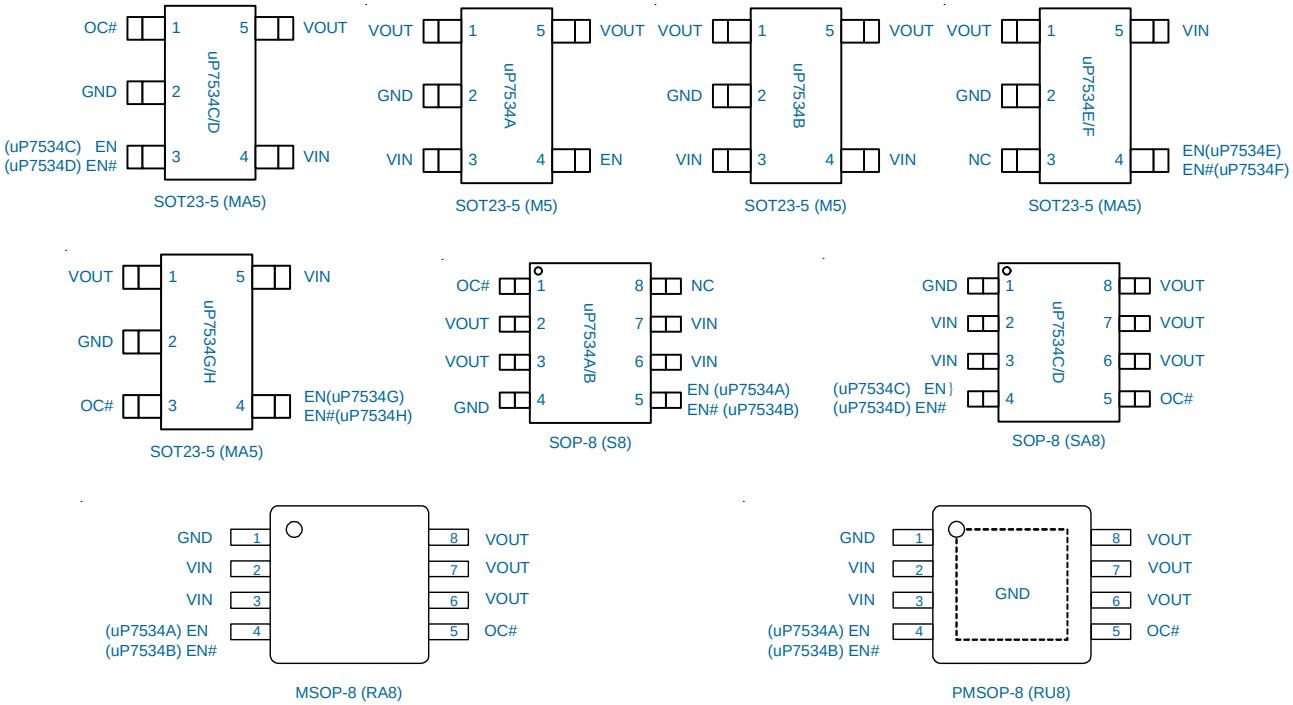
Features

- Compliant to USB Specifications
- Operating Range: 2.7 V to 5.5 V
- 75mΩ (5VIN MSOP) High Side MOSFET Switch
- 25uA Typical Quiescent Current
- <1uA Typical Shutdown Current
- Over Current/ Short Circuit Protect
- Thermal Shutdown Protection
- Deglitched Open Drain Fault Flag
- Slow Turn On and Fast Turn Off
- Enable Active-High or Active-Low
- UL Approved-E316940
- TuV EN60950-1 Certification
- CB IEC60950-1 Certification
- RoHS Compliant and Halogen Free

Applications

- Notebook and Desktop PCs
- USB Power Management
- ACPI Power Distribution
- Hot-Plug Power Supplies
- Battery-Powered Equipments
- Battery-Charger Circuits

Pin Configuration

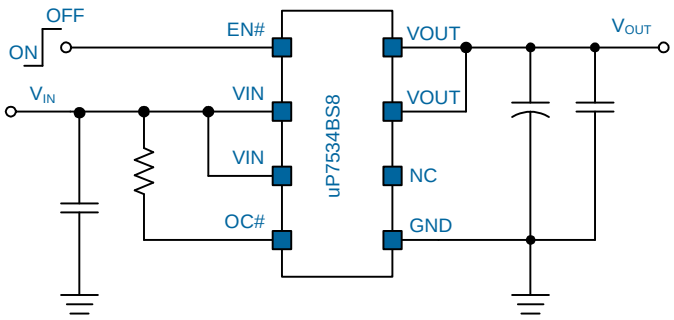


Ordering Information

Order Number	Package	Top Marking	Remark
uP7534AS8-XX	SOP-8L	S14-A-XX	Enable Acitve High
uP7534BS8-XX	SOP-8L	S14-B-XX	Enable Acitve Low
uP7534CSA8-XX	SOP-8L	uP7534CS8-XX	Enable Acitve High
uP7534DSA8-XX	SOP-8L	uP7534DS8-XX	Enable Acitve Low
uP7534AM5-XX	SOT23-5L	S14-A-XX	Enable Active High
uP7534BM5-XX	SOT23-5L	S14-B-XX	Without Enable Pin
uP7534CMA5-XX	SOT23-5L	S14-C-XX	Enable Active High
uP7534DMA5-XX	SOT23-5L	S14-D-XX	Enable Acitve Low
uP7534ARA8-XX	MSOP-8L	7534AXX	Enable Acitve High
uP7534BRA8-XX	MSOP-8L	7534BXX	Enable Acitve Low
uP7534ARU8-XX	PMSOP-8L	7534AXX	Enable Acitve High
uP7534BRU8-XX	PMSOP-8L	7534BXX	Enable Acitve Low
uP7534EMA5-XX	SOT23-5L	S14-E-XX	Enable Acitve High
uP7534FMA5-XX	SOT23-5L	S14-F-XX	Enable Acitve Low
uP7534GMA5-XX	SOT23-5L	S14-G-XX	Enable Acitve High
uP7534HMA5-XX	SOT23-5L	S14-H-XX	Enable Acitve Low

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

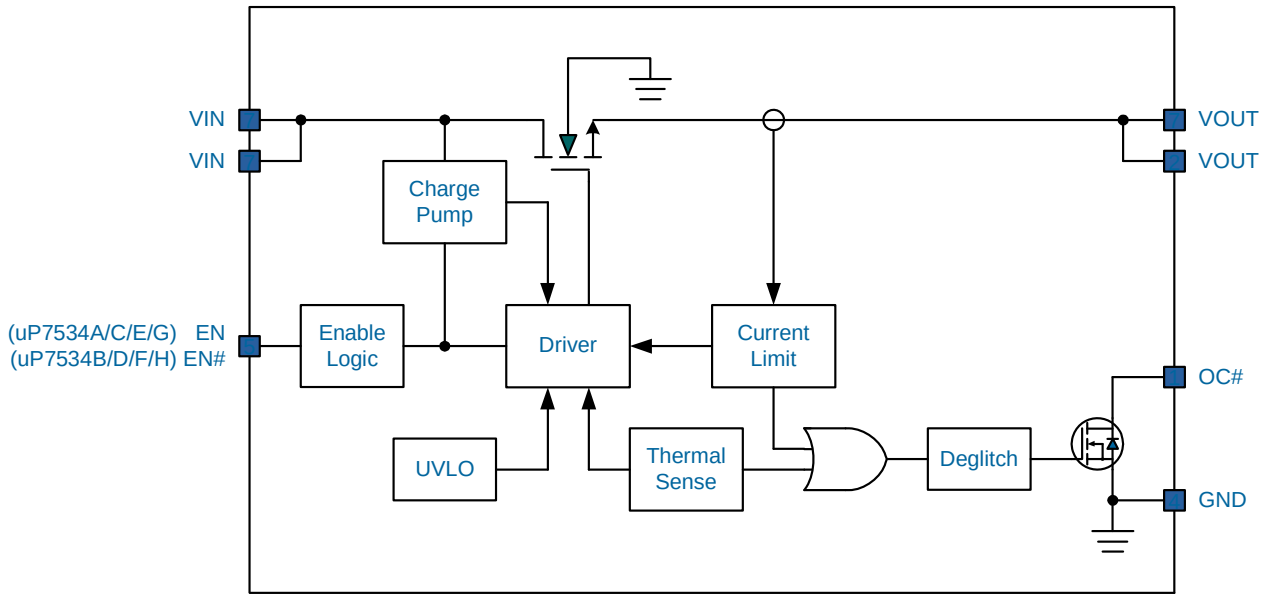
Typical Application Circuit



Functional Pin Description

Pin Name	Pin Function
OC#	**Fault Flag.** This is an active-low, open-drain fault flag output for p the power switch. The uP7534 asserts this pin low when fault occurs with typical 8ms deglitching time delay.
VOUT	**Output Voltage.** These pins are output from N-Channel MOSFET Source. Bypass this pin with a minimum 10uF capacitor to ground.
GND	**Ground.**
EN/EN#	**Enable Input.** This is the enable input to turn on/off the power switch. Active high for uP7534A/C/E/G and active low for uP7534B/D/F/H
VIN	**Supply Input.** This is the input pin to N-Channel MOSFET Drain and supply to control circuit. Bypass this pin with a 22uF capacitor to ground.
NC	**Not Internally Connected.**

Functional Block Diagram



Functional Description

Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from VOUT to VIN and VIN to VOUT when disabled. The power switch is controlled by a logic enable input (active high for uP7534A/C/E/G and active low for uP7534B/D/F/H) and driven by an internal charge pump circuit. When the output load exceeds the current-limit threshold or a short is present, the uP7534 asserts overcurrent protection and limits the output current to a safe level by driving the power switch into saturation mode.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Chip Enable (for uP7534A/C/E/G)

The EN pin receives a TTL or CMOS compatible input to enable/disable the uP7534A/C/E/G Logic low disables the power switch, charge pump, gate driver and other circuitry and reduces the supply current down to less than 1uA. Logic high restores bias to the drive and control circuits and turns the switch on.

Chip Enable (for uP7534B/D/F/H)

The EN# pin receives a TTL or CMOS compatible input to enable/disable the uP7534B/D/F/H. Logic high disables the power switch, charge pump, gate driver and other circuitry and reduces the supply current down to less than 1uA. Logic low restores bias to the drive and control circuits and turns the switch on.

Soft Start

The uP7534 features soft start function to eliminate the inrush current into downstream and voltage droop of upstream when hot-plug-in with capacitive loads. The soft start interval is 0.9ms typically. The input current to charge up the load capacitor is proportional to its capacitance. The uP7534 current limit function may be active during the plug-in of extreme large capacitive load. The fault flag is masked during the softstart interval.

Over Current Limit

The uP7534 continuous monitors the output current for overcurrent protection to protect the system power, the power switch, and the load from damage during output short circuit or soft start interval. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load. The current limit level is typical 1A when the power switch operates in linear region and is typical 0.6A in saturation region (for uP7534A/BS8-06).

The uP7534 asserts fault condition and pulls low OC# when overcurrent, overtemperature, input under voltage lockout condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 8ms deglitch circuit prevents the OC# signal from oscillation or false triggering. If an overtemperature shutdown occurs, the OC# is asserted instantaneously.

Overtemperature Protection

The uP7534 continuously monitor the operating temperature of the power switch for overtemperature protection. The uP7534 asserts overtemperature and turns off the power switch to prevent the device from damage if the junction temperature rises to approximately 135°C due overcurrent or short-circuit conditions. Hysteresis is built into the thermal sense, the switch will not turns back on until the device has cooled approximately 20 degrees. The open-drain false reporting output (OC#) is asserted (active low) when an overtemperature shutdown or overcurrent occurs. If the fault condition is not removed, the switch will pulse on and off as the temperature cycles between these limits.

Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2.2V, a control signal turns off the power switch.

Output Voltage Discharge When Disabled

The output voltage is discharged through an internal 100Ω resistor when the output voltage is disabled.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VIN

- DC ---------- -0.3V to +6V
- < 200us, non-repetitive ---------- -0.3V to +10V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature (Soldering, 10 sec) ---------- 260°C

ESD Rating (Note 2)

- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

- SOP-8 θ_{JA} ---------- 160°C/W
- SOP-8 θ_{JC} ---------- 39°C/W
- SOT23-5 θ_{JA} ---------- 250°C/W
- SOT23-5 θ_{JC} ---------- 50°C/W
- MSOP-8 θ_{JA} ---------- 160°C/W
- MSOP-8 θ_{JC} ---------- 40°C/W
- PMSOP-8 θ_{JA} ---------- 86°C/W
- PMSOP-8 θ_{JC} ---------- 30°C/W

Power Dissipation, P_D @ T_A = 25°C

- SOP-8 ---------- 0.625W
- SOP23-5 ---------- 0.4W
- MSOP-8 ---------- 0.625W
- PMSOP-8 ---------- 1.16W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Supply Input Voltage, V_{IN} ---------- +2.7V to +5.5V

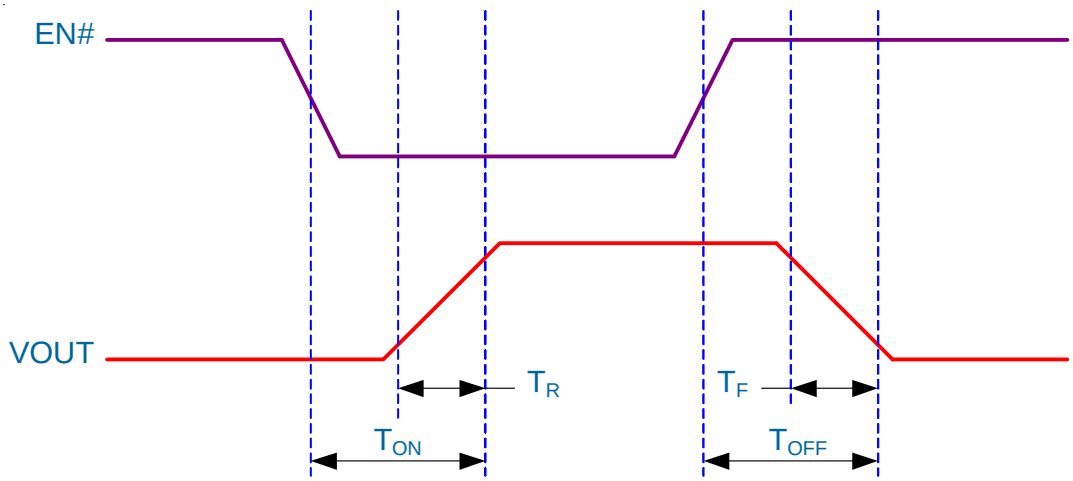
Electrical Characteristics

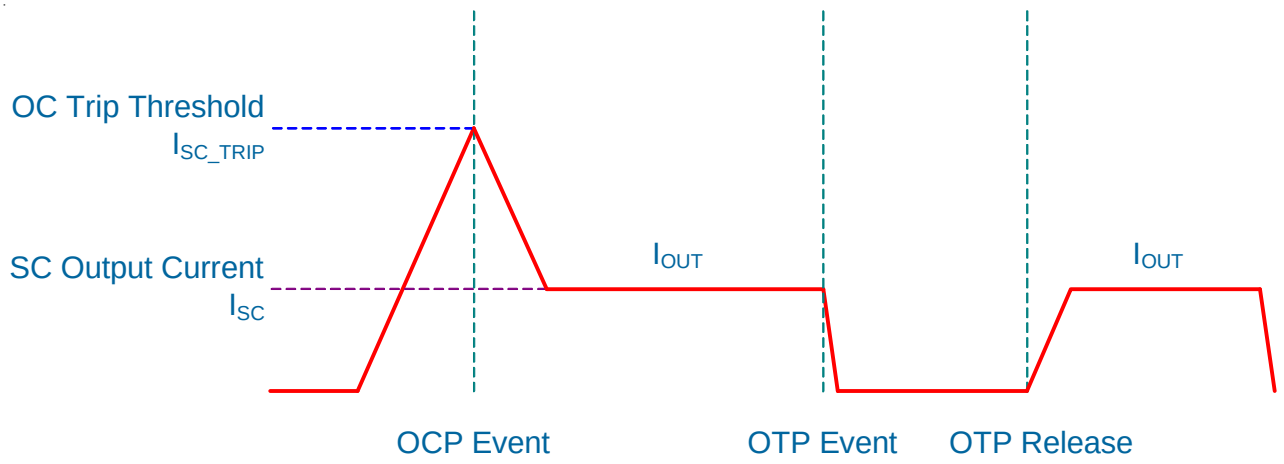
(V_{IN}= 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Suppy Input Voltage			2.7	--	5.5	V
Under Voltage Lockout	V_{UVLO}	V_{IN} rising	--	2.2	2.5	V
UVLO Hysteresis	ΔV_{UVLO}		--	75	--	mV
Shutdown Current	I_{SD}	No load on VOUT, Disabled	--	0.1	1	uA
Quiescent Current	I_Q	No load on VOUT, Enabled	--	25	50	uA

Electrical Characteristics

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Chip Enable							
Logic High Threshold		2.7V < V_{IN} < 5.5V		1.4	--	--	V
Logic Low Threshold		2.7V < V_{IN} < 5.5V		--	--	0.4	V
Enable Input Current		0V < V_{EN}, $V_{EN\#}$ < 5.5V		-0.5	--	0.5	uA
Turn On Time (Note 5)	T_{ON}	C_L = 1uF, R_L = 10Ω		--	1	--	ms
Turn Off Time (Note 5)	T_{OFF}	C_L = 1uF, R_L = 10Ω		--	0.3	--	ms
Output Rise Time	T_R	C_L = 1uF, R_L = 10Ω		0.6	0.9	1.2	ms
Output Fall Time	T_F	C_L = 1uF, R_L = 10Ω		--	0.2	0.5	ms
Output Discharge Resistance when Disabled		Disabled.		--	100	--	Ω
Power Switch							
N-MOSFET ON Restiance	$R_{DS(ON)}$	uP7534ARA8-20, uP7534BRA8-20, V_{IN} = 5.0V , I_{OUT} = 0.5A		--	70	75	mΩ
		uP7534A/B/C/D (Others), V_{IN} = 5.0V , I_{OUT} = 0.5A		--	90	100	
		uP7534E/F/G/H, V_{IN} = 5.0V , I_{OUT} = 0.5A		--	100	110	
Leakage Current		VOUT connected to GND, Disabled		--	--	1	uA
Reverse Leakge Current		V_{OUT} = 5.5V, V_{IN} = 0V		--	--	1	uA
Current Limit							
Short Circuit Output Current	I_{SC}	V_{IN} = 5.0V, VOUT connected to GND, device enabled into short-circuit	uP7534XXXX-06	--	0.6	0.9	A
			uP7534XXXX-10	--	1.0	1.5	
			uP7534XXXX-15	--	1.5	2.3	
			uP7534XXXX-20	--	2.0	3.0	
Overcurrent Trip Threshold	I_{SC_TRIP}	V_{IN} = 5.0V, current ramp < 100A/s on VOUT	uP7534XXXX-06	0.6	1.0	1.5	A
			uP7534XXXX-10	1.1	1.8	1.9	
			uP7534XXXX-15	2.0	2.5	3.8	
			uP7534XXXX-20	2.8	3.3	5.0	
Fault Flag (OC#)							
Output Low Voltage	V_{OL}	$I_{OC\#}$ = 5mA		--	--	0.4	V
Off State Current		$V_{OC\#}$ = 5.5V		--	--	1	uA
OC# Deglitch		OC# assertion delay		5	8	15	ms
Over Current Protection							
Shutdown-Level Threshold		By Design		--	135	--	°C
Thermal Shutdown Hysteresis		By Design		--	20	--	°C





Note 1. Stresses beyond those listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operation Condition* section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

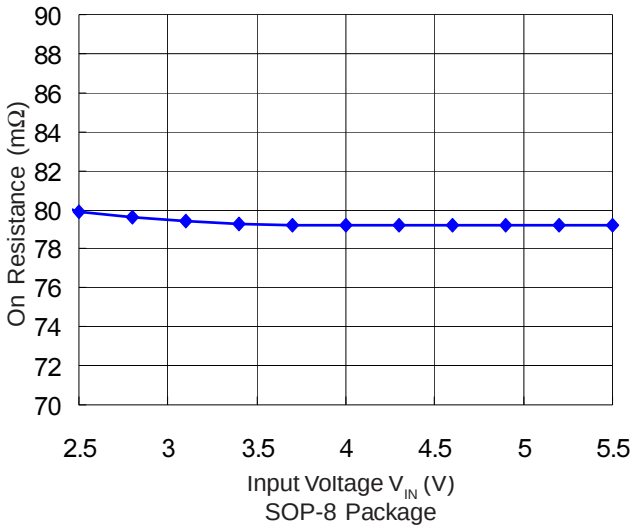
Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

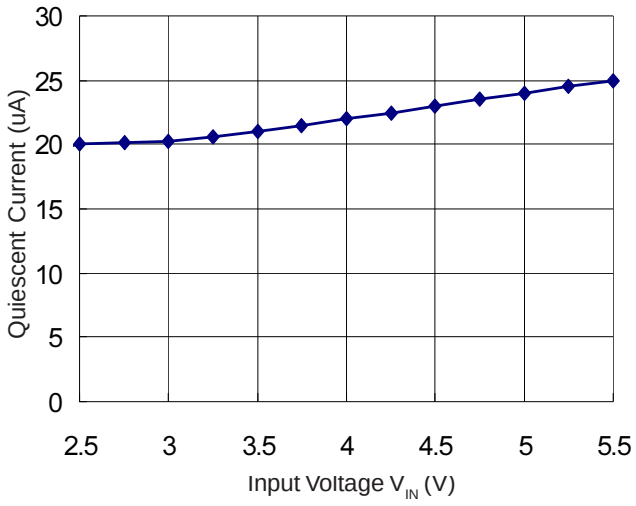
Note 5. These items are not tested in production, specified by design.

Typical Operation Characteristics

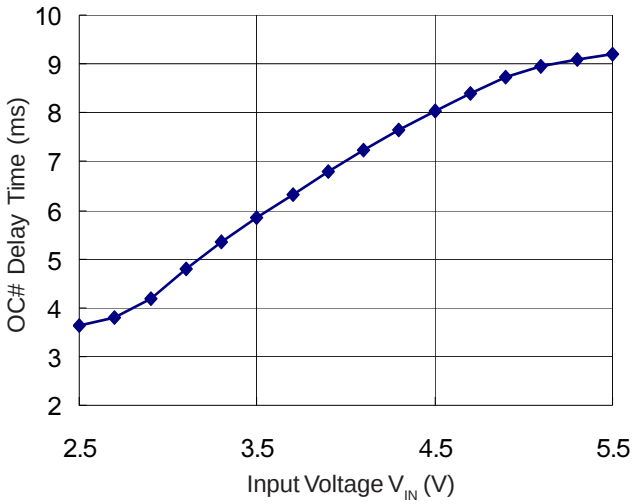
On Resistance vs. Input Voltage



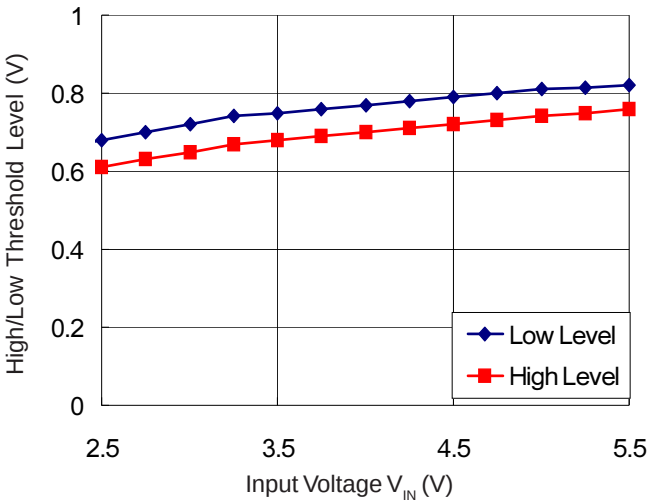
Quiescent Current vs. Input Voltage



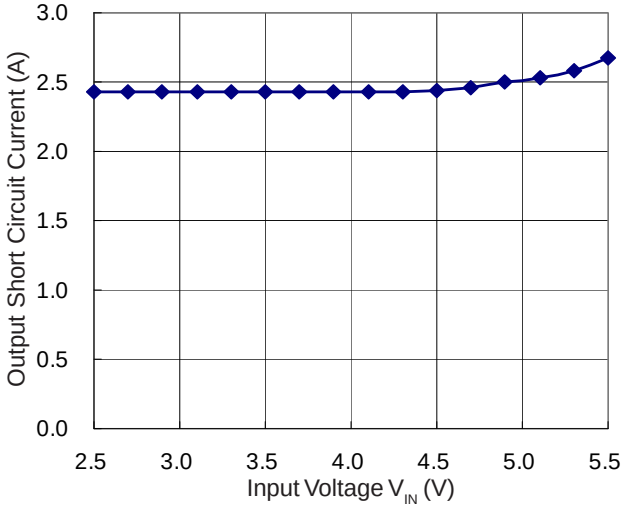
OC# Delay Time vs. Input Voltage



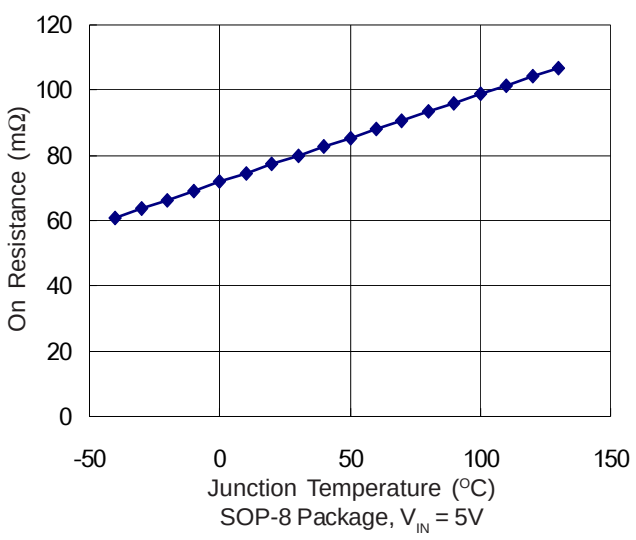
EN/EN# Threshold Level vs. Input Voltage



Short Circuit vs. Input Voltage

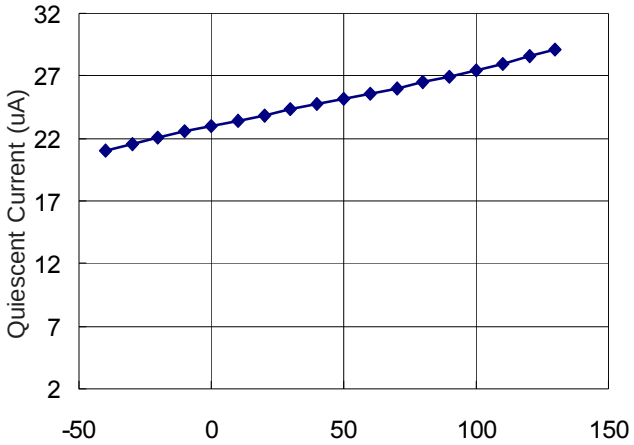


On Resistance vs. Temperature



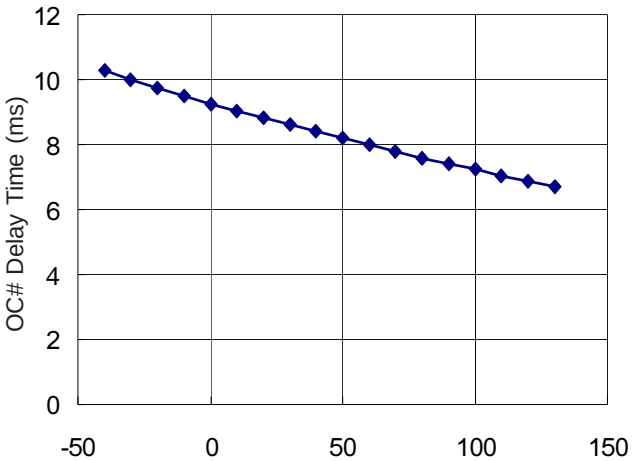
Typical Operation Characteristics

Quiescent Current vs. Temperature



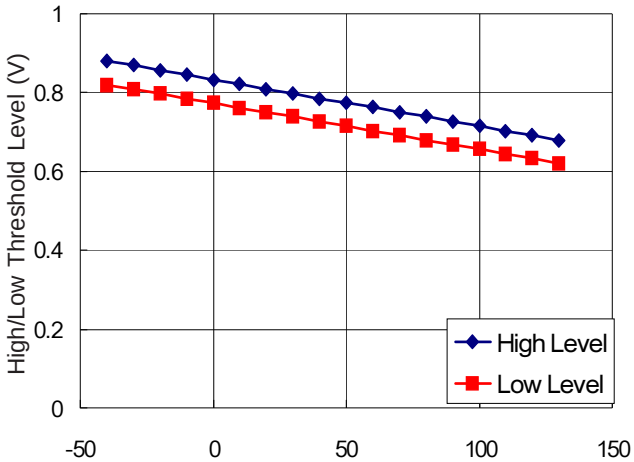
V_{IN} = 5V

OC# Delay Time vs. Temperature



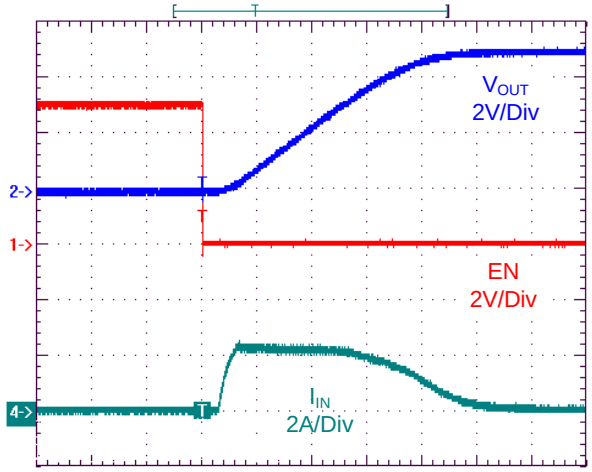
V_{IN} = 5V

EN/EN# Threshold Level vs. Temperature



V_{IN} = 5V

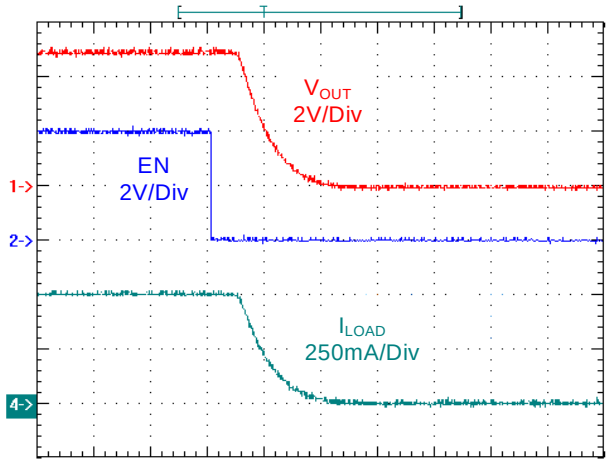
Turn On Waveforms



Time (1ms/Div)

V_{IN} = 5V, C_{OUT} = 1600uF

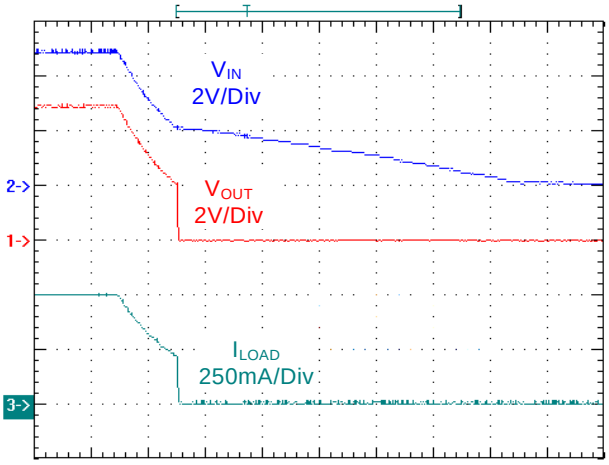
Turn Off Waveforms



Time (100us/Div)

V_{IN} = 5V, C_{OUT} = 1uF, R_{LOAD} = 10Ω

Power Off Waveforms

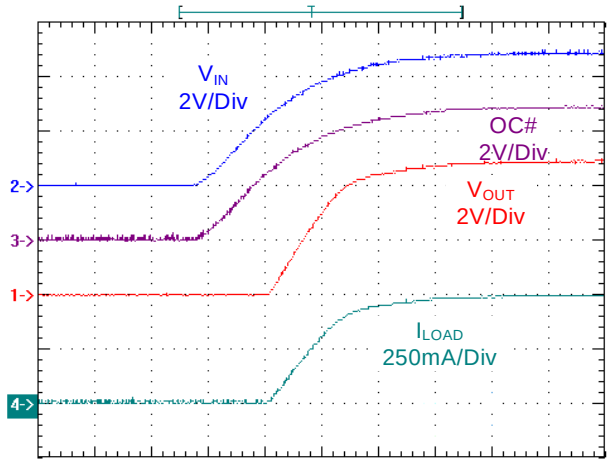


Time (2.5ms/Div)

C_{IN} = C_{OUT} = 1uF, R_{LOAD} = 10Ω

Typical Operation Characteristics

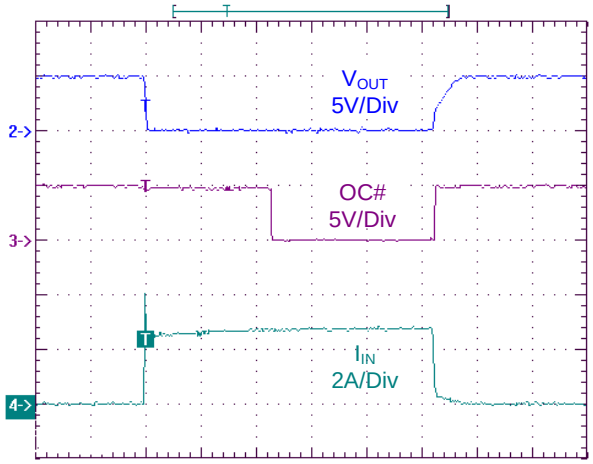
Power On Waveforms



Time (2.5ms/Div)

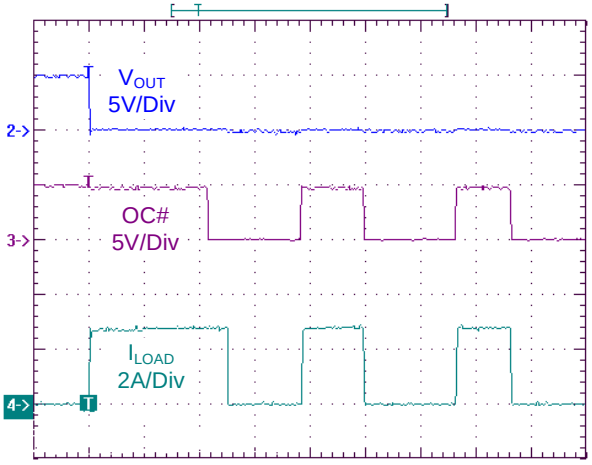
V_{IN} = 5V, C_{OUT} = 1uF, R_{LOAD} = 10Ω

OC# Response



Time (4ms/Div)

Short Circuit Protection and OTP



Time (4ms/Div)

V_{IN} = 5V, C_{OUT} = 470uF, R_{LOAD} = 0Ω

Application Information

Supply Input Filtering

VIN pins supply power to the power switch and internal circuit. Both of them should be connect to upstrem power supply with short and wide trace on the PCB.

Events such as hot-plug/unplug, output short circuit and overtemperature result in step change of input current with sharp edges, which in turn causes voltage transient at supply input due to di/dit effect of parasitic inductance on the current path. A 0.1uF ceramic capacitor from VIN to GND, physically located near the device is strongly recommended to control the supply input transient. Minimizing the parasitic inductance along the current path also alleviate the voltage transient at the supply input.

Output Voltage Filtering

Bypassing the output voltage with a 0.1uF ceramic capacitor improves the immunity of the device against output short circuit and hot plug/unplug of load. A lower ESR capacitor results in lower voltage drop against a step load change. A large electrolytic capacitor from VOUT to GND is also recommended. This capacitor reduces power supply transient that may cause ringing on the input.

USB supports dynamic attachment (hot plug-in) of peripherals. A current surge is caused by the input capacitance of downstream device. Ferrite beads are recommended in series with all power and ground connector pins. Ferrite beads reduce EMI and limit the inrush current during hot-attachment by filtering high-frequency signals. The DC resistance of the ferrite bead should be specially taken care to reduce the voltage drop.

Voltage Drop and Power Dissipation

Temperature effect should be well considered when dealing with voltage drop and power dissipation. The maximum $R_{DS(ON)}$ of the power switch is 100mΩ under 25°C junction temperature. If the device is expected to operate at 125°C junction temperature, the RDS(ON) will become

100mΩ * (1 + (125°C - 25°C) * 0.5%/°C) = 150mΩ

where 0.5%/°C is the approximated temperature coefficient of the $R_{DS(ON)}$.

If the maximum load current is expected to be 1.2A, the maximum voltage will become

1.2A * 150mΩ = 180mV

This in turn will cause power dissipation as

1.2A * 180mV = 215mW

The temperature raise is calculated as

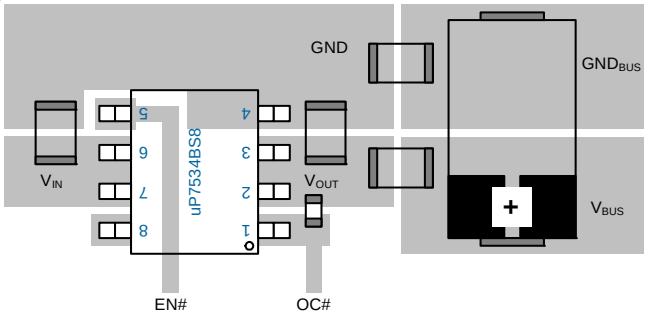
215mW * 160 °C/W = 35°C

The junction temperature is calculated as T_A + 35°C, where T_A is the expected maximum ambient temperature. A few iterations are required until get final solutions.

Layout Consideration

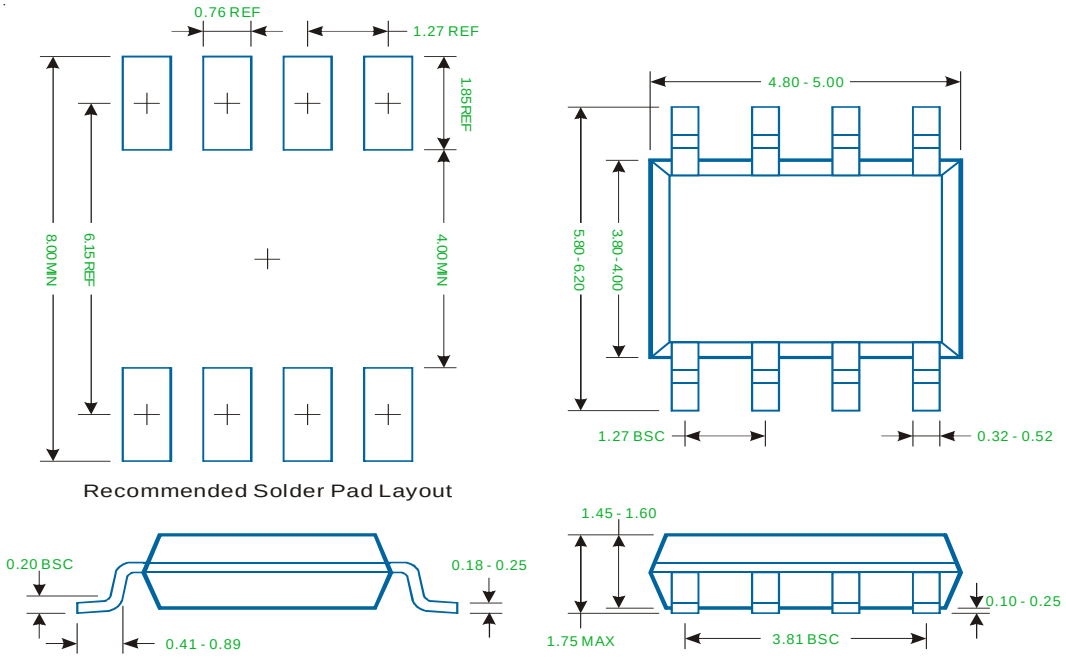
The power circuitry of usb printed circuit boards requires a customized layout to maximize thermal dissipation and to minimized voltage drop and EMI

- Place the device physically as close to the USB port as possible. Keep all traces wide, short and direct to minimized the parasitic inductance. This optimizes the switch response time to output short circuit conditions.
- Place both input and output bypass capacitors near to the device.
- If ferrite beads are used, use wires with minimum resistance and large solder pads to minimize connection resistance.
- All VOUT pins should be connected together on the PCB. All VIN pins should be connected together on the PCB.



Package Information

SOP-8L SMD Package

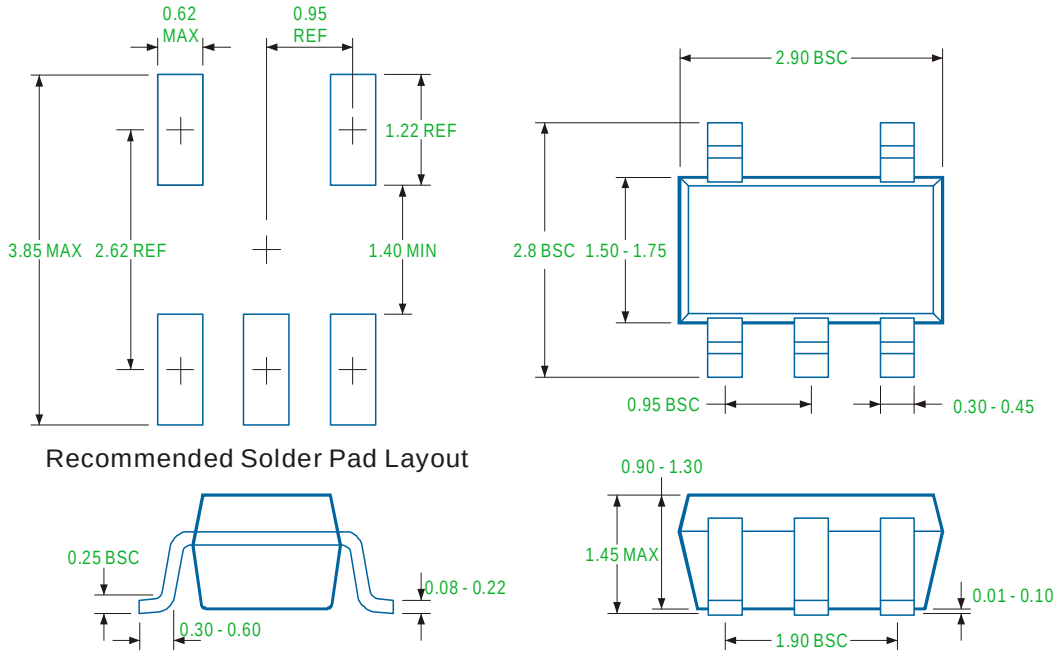


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

SOT23-5L SMD Package

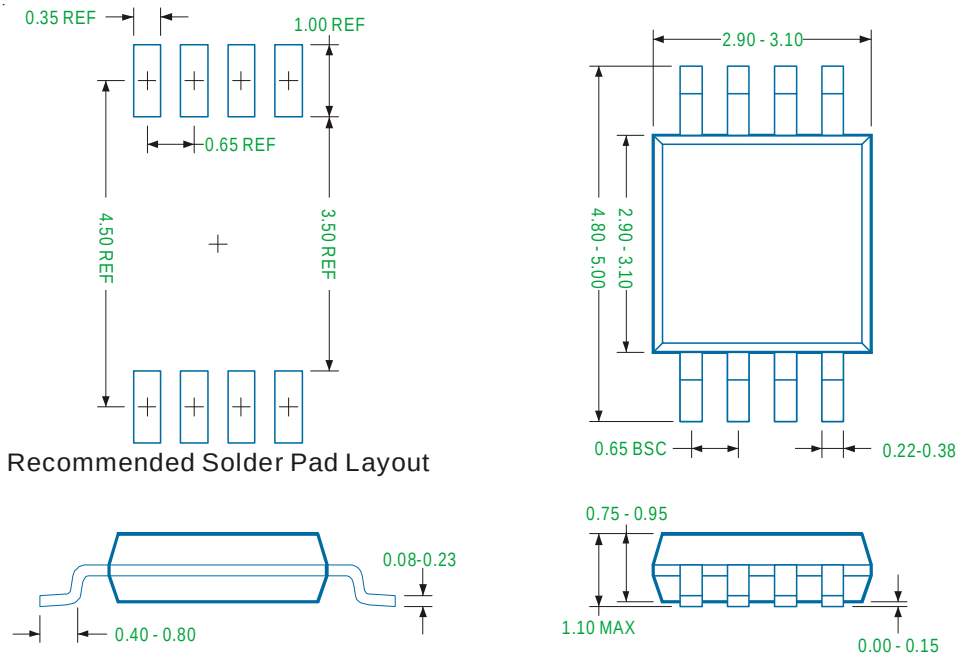


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

MSOP - 8L Package

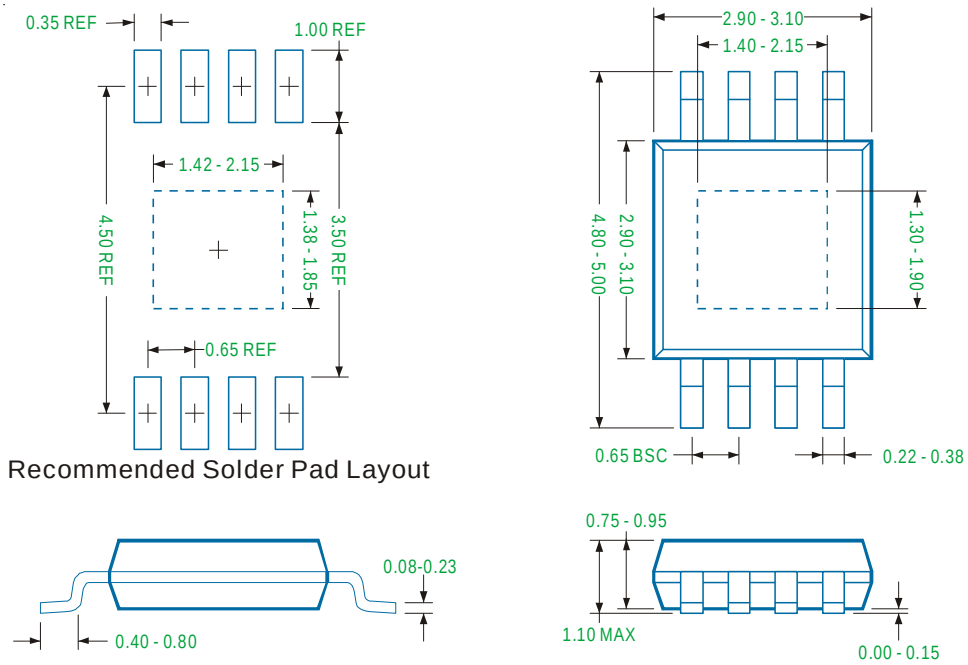


Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Package Information

PMSOP - 8L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

COPYRIGHT (c) 2007, UPI SEMICONDUCTOR CORP.

uPI Semiconductor Corp.

Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064