

## HIGH FREQUENCY NPN TRANSISTOR ARRAY

## FEATURES

- **BUILT-IN ULTRAHIGH FREQUENCY MULTIPLIER:** (Each Transistor has fr 9 GHz)
- **OUTSTANDING  $h_{FE}$  LINEARITY**
- **TWO PACKAGE OPTIONS:**
  - $\mu$ PA101B: Superior thermal dissipation due to studded 14-pin ceramic package
  - $\mu$ PA101G: Reduced circuit size due to 8-pin plastic SOP package for surface mounting

## DESCRIPTION AND APPLICATIONS

This Si bipolar transistor array contains six bipolar transistors which have fr 9 GHz. Applications include a multiplier, double balanced mixer, phase detector, or AGC circuit. The two package options offer a choice of excellent heat dissipation or 35 % size reduction.

## ORDERING INFORMATION

| PART NUMBER     | PACKAGE                     |
|-----------------|-----------------------------|
| $\mu$ PA101B-E1 | 14-pin ceramic package      |
| $\mu$ PA101G-E1 | 8-pin plastic SOP (225 mil) |

ABSOLUTE MAXIMUM RATINGS ( $T_A = +25\text{ }^\circ\text{C}$ )

| SYMBOLS     | PARAMETERS                   | UNITS            | RATINGS     |
|-------------|------------------------------|------------------|-------------|
| $V_{CBO}^*$ | Collector to Base Voltage    | V                | 15          |
| $V_{CEO}^*$ | Collector to Emitter Voltage | V                | 6           |
| $V_{EBO}^*$ | Emitter to Base Voltage      | V                | 2.5         |
| $I_C^*$     | Collector Current            | mA               | 40          |
| $P_T$       | Power Dissipation            |                  |             |
|             | $\mu$ PA101B                 | mW               | 650         |
|             | $\mu$ PA101G                 | mW               | 250         |
| $T_J$       | Junction Temperature         |                  |             |
|             | $\mu$ PA101B                 | $^\circ\text{C}$ | 200         |
|             | $\mu$ PA101G                 | $^\circ\text{C}$ | 125         |
| $T_{STG}$   | Storage Temperature          |                  |             |
|             | $\mu$ PA101B                 | $^\circ\text{C}$ | -55 to +200 |
|             | $\mu$ PA101G                 | $^\circ\text{C}$ | -55 to +125 |

\* Absolute maximum ratings for each transistor.

## Caution electro-static sensitive devices

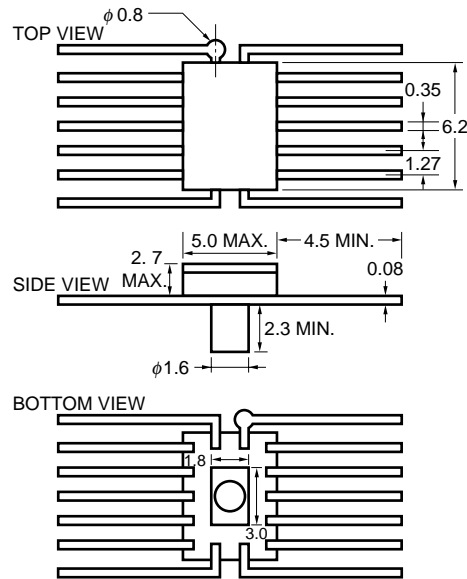
The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PACKAGE DIMENSIONS (UNIT: mm)

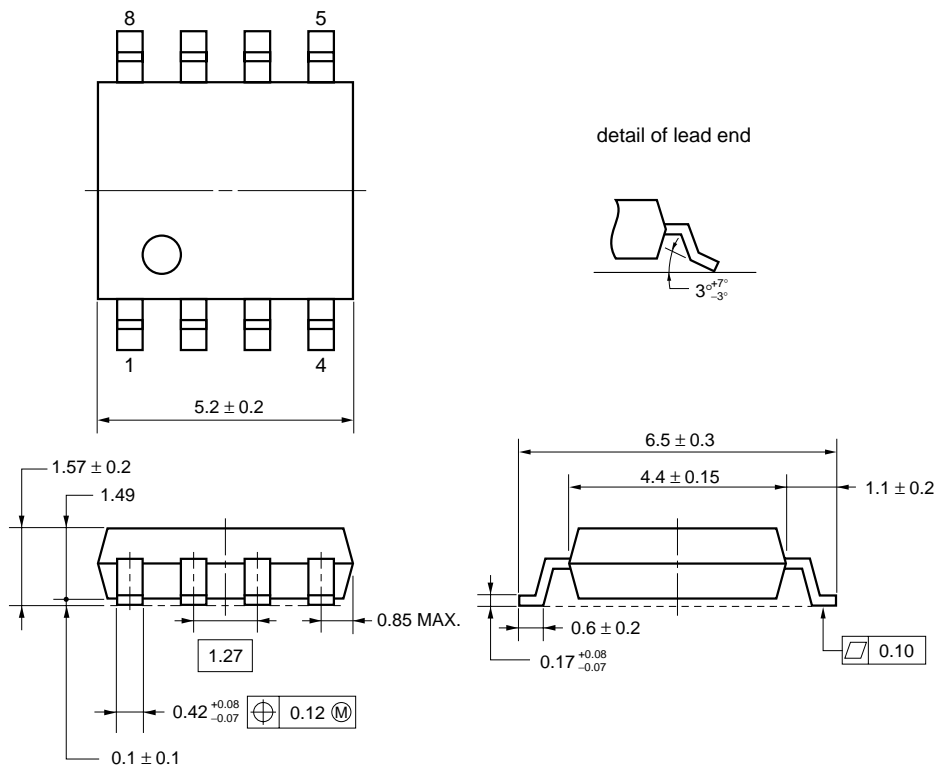
μPA101B

14 PIN CERAMIC PACKAGE



μPA101G

★ 8 PIN PLASTIC SOP (225 mil)



**NOTE** Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

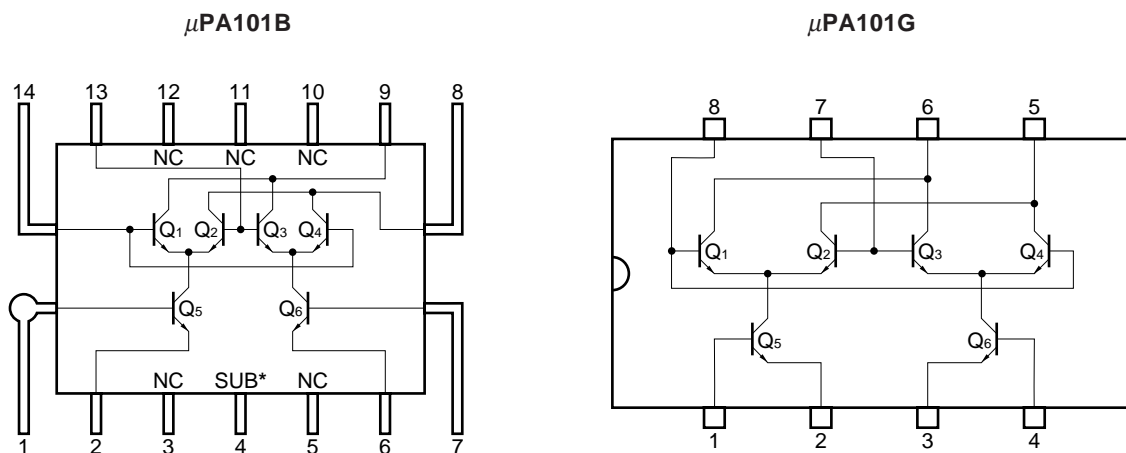
See connection diagram for description of leads.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise specified  $T_A = +25\text{ }^\circ\text{C}$  μPA101B, μPA101G common)

| SYMBOLS           | PARAMETERS AND CONDITIONS   | UNITS | MIN. | TYP. | MAX. |
|-------------------|---|-------|------|------|------|
| $I_{CBO}$         | Collector Cut-off Current at $V_{CB} = 5\text{ V}$ , $I_E = 0$ (Q1 thru Q6)                   | μA    |      |      | 1.0  |
| $I_{EBO}$         | Emitter Cut-off Current at $V_{EB} = 1\text{ V}$ , $I_C = 0$ (Q5 and Q6)                      | μA    |      |      | 1.0  |
| $h_{FE}$          | Direct Current Amplification, $V_{CE} = 3\text{ V}$ , $I_C = 1\text{ mA}$ (Q5 and Q6)         |       | 40   | 100  | 250  |
| $h_{FE1}/h_{FE2}$ | Direct Current Amplification Ratio, $V_{CE} = 3\text{ V}$ , $I_C = 1\text{ mA}$ , (Q5 and Q6) |       | 0.9  | 1.0  | 1.1  |
| $C_{EB}$          | Emitter to Base Capacitance at $V_{EB} = 0$ , $f = 1\text{ MHz}$                              | pF    |      | 1.4  | 2.8  |
| $f_T$             | Gain Bandwidth Product* at $V_{CE} = 3\text{ V}$ , $I_C = 10\text{ mA}$                       | GHz   |      | 9    |      |

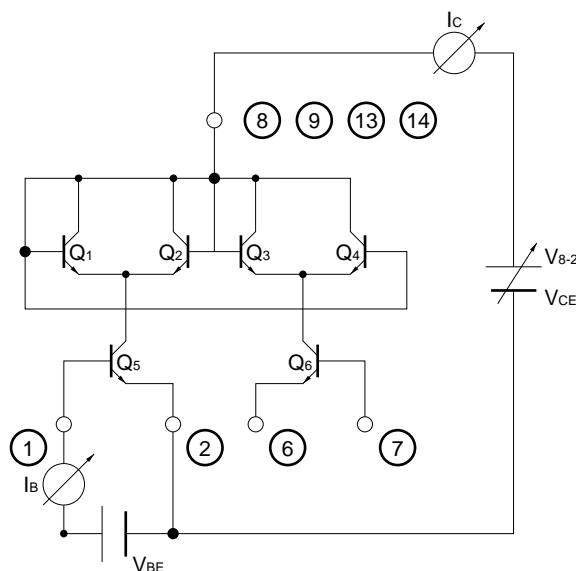
\* Measured by installing a single transistor in a Micro-X package: the value shown is a reference value.

**CONNECTION DIAGRAM** (Top View)



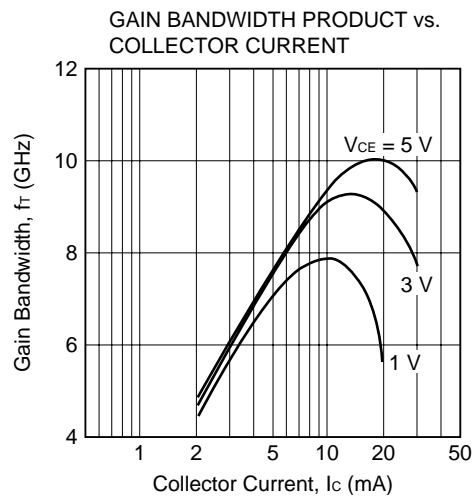
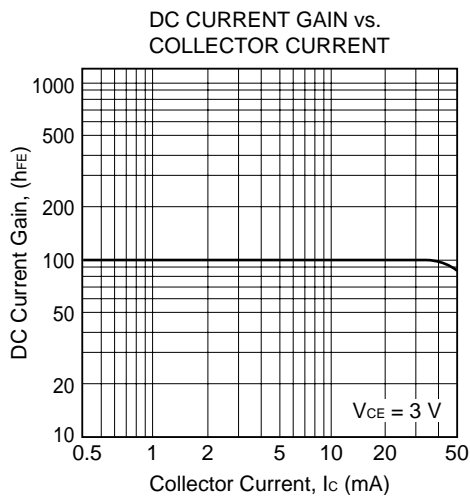
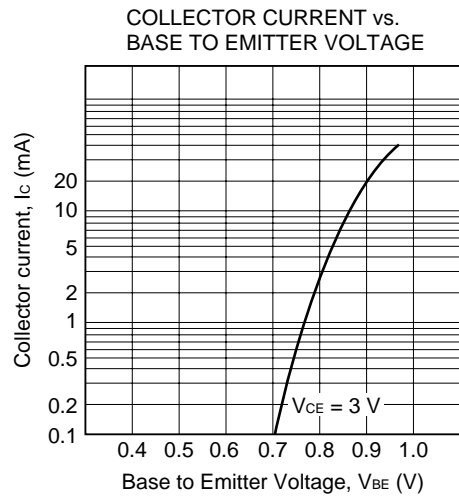
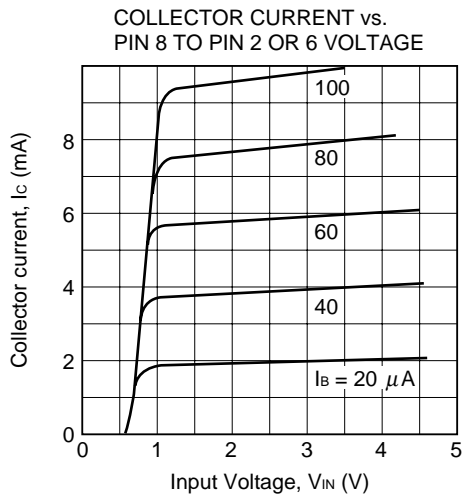
\* Substrate should be connected to the lowest voltage point to prevent latch-up.

**TEST CIRCUIT SCHEMATIC\*** (For Electrical Characteristics Measurements excluding  $f_T$ )



\* See performance characteristics for voltage.

TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = +25\text{ }^\circ\text{C}$ )



**NOTES ON CORRECT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired operation).
- (3) Design circuits connected Subpin to the lowest voltage to prevent latch-up.
- (4) Design circuits as each pin voltage difference within 15 V maximum.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

**μPA101G**

| Soldering process   | Soldering conditions   | Recommended condition symbol |
|---------------------|--|------------------------------|
| Infrared ray reflow | Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C),<br>Time: 2 times, Limited days: no. <sup>Note</sup> | IR35-00-2                    |
| VPS                 | Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C),<br>Time: 2 times, Limited days: no. <sup>Note</sup> | VP15-00-2                    |
| Wave soldering      | Soldering tub temperature: less than 260 °C, Hour: within 10 s.<br>Time: 1 time, Limited days: no. <sup>Note</sup>           | WS60-00-1                    |
| Pin part heating    | Pin area temperature: less than 300 °C, Hour: within 3 s./pin<br>Limited days: no. <sup>Note</sup>                           |                              |

**μPA101B**

| Soldering process      | Soldering conditions   | Symbol |
|------------------------|--|--------|
| Infrared ray reflow    | Peak package's surface temperature: 230 °C or below,<br>Reflow time: 10 seconds or below (210 °C or higher),<br>Number of reflow process: 1, Exposure limit*: None |        |
| Partial heating method | Terminal temperature: 260 °C or below,<br>Flow time: 10 seconds or below,<br>Exposure limit*: None   |        |

**Note** It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

**Caution** The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]

NESAT (NEC Silicon Advanced Technology) is a trademark of NEC Corporation.

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
  - No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
  - NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
  - Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
  - While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
  - NEC devices are classified into the following three quality grades:  
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
    - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
    - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
    - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.
- The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.