

MOS FIELD EFFECT TRANSISTOR μ PA1740TP

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA1740TP is N-channel MOS FET device that features a low on-state resistance and excellent swiching characteristics, and designed for high voltage applications such as DC/DC converter.

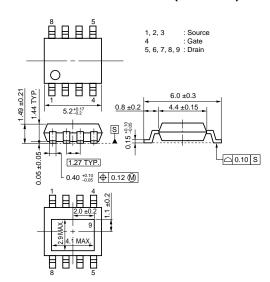
FEATURES

- High voltage: VDSS = 200 V
- Gate voltage rating: ±30 V
- Low on-state resistance
 - $R_{DS(on)}$ = 0.44 Ω MAX. (Vgs = 10 V, Ip = 3.5 A)
- Low input capacitance
 Assart TVP (V)
- Ciss = 420 pF TYP. (VDs = 10 V, VGS = 0 V)
- Built-in gate protection diode
- Small and surface mount package (Power HSOP8)
- Avalanche capability rated

ORDERING INFORMATION

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PART NUMBER	PACKAGE
μPA1740TP	Power HSOP8

PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, Unless otherwise noted, All terminals are connected.)

Drain to Source Voltage (Vos = 0 V)	VDSS	200	V	
Gate to Source Voltage (VDS = 0 V)	Vgss	±30	V	
Drain Current (DC) (Tc = 25°C)	ID(DC)	±7.0	Α	
Drain Current (pulse) Note1	D(pulse)	±21	Α	
Total Power Dissipation (Tc = 25°C)	P _{T1}	22	W	EQUIVALENT CIRCUIT
Total Power Dissipation (T _A = 25°C) ^{Note2}	P _{T2}	1.0	W	Drain
Channel Temperature	Tch	150	°C	
Storage Temperature	Tstg	-55 to + 150	°C	□ ↓ Body
Single Avalanche Current Note3	las	7.0	Α	Gate
Single Avalanche Energy Note3	Eas	4.9	mJ	*
Repetitive Avalanche Current Note4	IAR	7.0	Α	Gate J Protection
Repetitive Avalanche Energy Note4	Ear	2.2	mJ	Diode Source

- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on a glass epoxy board (1 inch x 1 inch x 0.8 mm), PW = 10 sec
 - 3. Starting T_{ch} = 25°C, V_{DD} = 100 V, R_G = 25 Ω , L = 100 μ H, V_{GS} = 20 \rightarrow 0 V
 - **4.** $T_{ch} \le 125^{\circ}C$, $V_{DD} = 100 \text{ V}$, $R_{G} = 25 \Omega$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

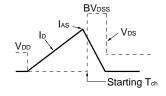
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ELECTRICAL CHARACTERISTICS (TA = 25°C, Unless otherwise noted, All terminals are connected.)

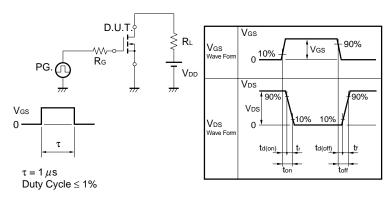
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 200 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±30 V, V _{DS} = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1.0 mA	2.5	3.5	4.5	٧
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 3.5 A	3	4.5		S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, ID = 3.5 A		0.35	0.44	Ω
Input Capacitance	Ciss	V _{DS} = 10 V		420		pF
Output Capacitance	Coss	V _{GS} = 0 V		100		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		45		pF
Turn-on Delay Time	t d(on)	V _{DD} = 100 V, I _D = 3.5 A		5		ns
Rise Time	tr	V _{GS} = 10 V		7.5		ns
Turn-off Delay Time	td(off)	$R_G = 10 \Omega$		21		ns
Fall Time	tf			7		ns
Total Gate Charge	Q _G	V _{DD} = 160 V		12		nC
Gate to Source Charge	Qgs	V _{GS} = 10 V		2		nC
Gate to Drain Charge	Q _{GD}	ID = 7.0 A		6.5		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 7.0 A, VGS = 0 V		1.0	1.5	V
Reverse Recovery Time	trr	IF = 7.0 A, VGS = 0 V		110		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/μs		360		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{RG} = 25 \Omega \\ \text{V} \\ \text{VSS} = 20 \rightarrow 0 \text{ V} \end{array}$



TEST CIRCUIT 2 SWITCHING TIME

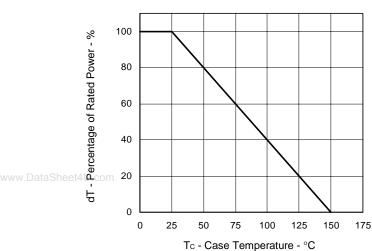


TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T.\\ \hline I_G=2\ mA \\ \hline \hline W. \\ \hline \end{array} \begin{array}{c} RL \\ \hline \end{array}$$

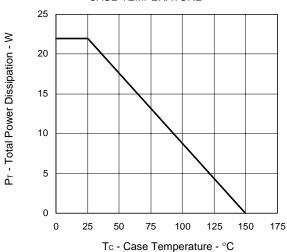
TYPICAL CHARACTERISTICS (TA = 25°C)



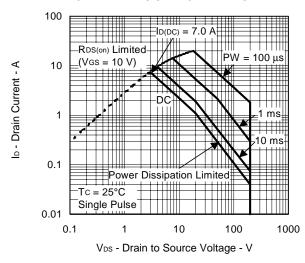


CASE TEMPERATURE 25

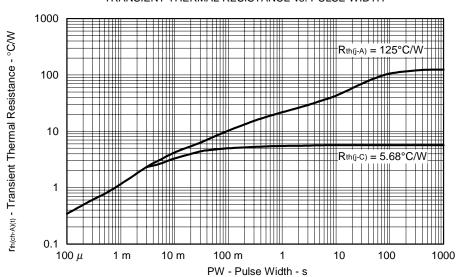
TOTAL POWER DISSIPATION vs.



FORWARD BIAS SAFE OPERATING AREA

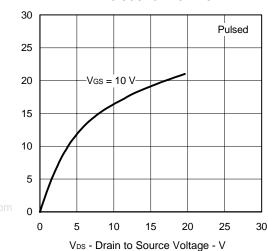


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

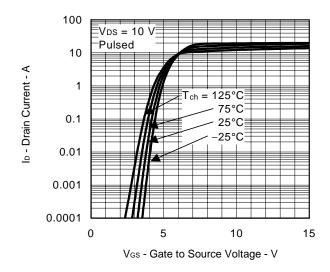


lo - Drain Current - A

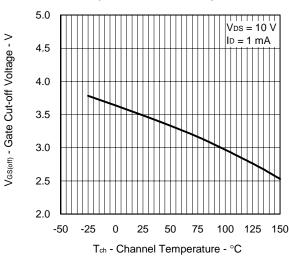
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



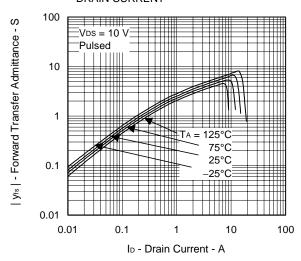
FORWARD TRANSFER CHARACTERISTICS



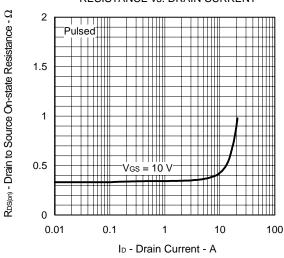
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



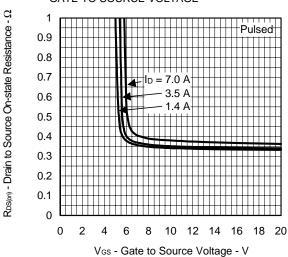
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

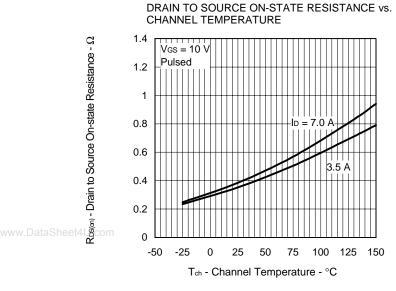


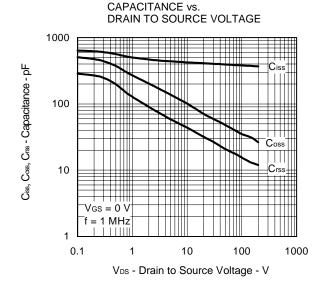
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

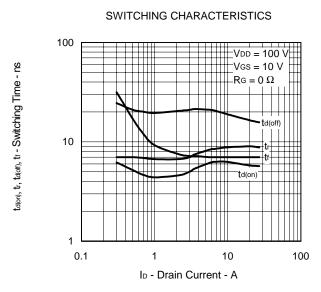


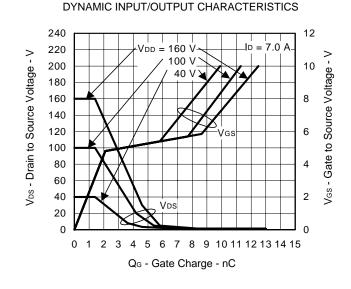
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

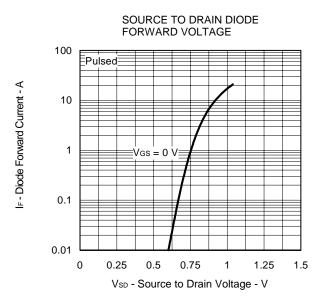


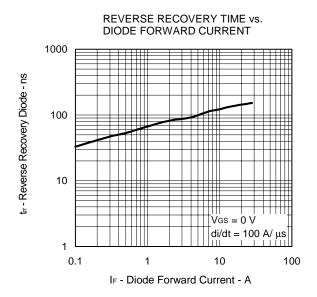


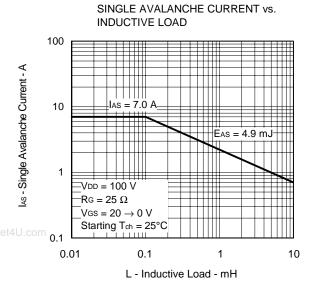


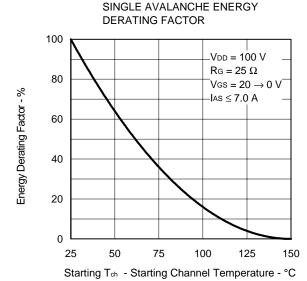












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