

MOS FIELD EFFECT TRANSISTOR μ PA1743TP

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA1743TP is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

FEATURES

- High voltage: VDSS = 250 V
- Gate voltage rating: ±30 V
- Low on-state resistance

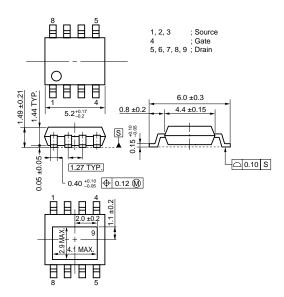
RDS(on) = 0.45Ω MAX. (Vgs = 10 V, ID = 4.0 A)

- Low input capacitance
 - Ciss = 570 pF TYP. (VDS = 10 V, VGS = 0 V)
- · Built-in gate protection diode
- Small and surface mount package (Power HSOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1743TP	Power HSOP8

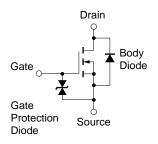
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, unless otherwise noted. All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	250	V	
Gate to Source Voltage (Vps = 0 V)	Vgss	±30	V	
Drain Current (DC) (Tc = 25°C)	$I_{D(DC)}$	±8.0	Α	
Drain Current (pulse) Note1	D(pulse)	±24	Α	
Total Power Dissipation (Tc = 25°C)	P _{T1}	26	W	
Total Power Dissipation (T _A = 25°C) Note2	P _{T2}	1.0	W	
Channel Temperature	Tch	150	°C	
Storage Temperature	Tstg	-55 to +150	°C	
Single Avalanche Current Note3	IAS	8.0	Α	
Single Avalanche Energy Note3	Eas	6.4	mJ	
Repetitive Avalanche Current Note4	Iar	8.0	Α	
Repetitive Pulse Avalanche Energy Note4	Ear	6.4	mJ	

EQUIVALENT CIRCUIT



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on a glass epoxy board of 1 inch x 1 inch x 0.8 mm
 - 3. Starting T_{ch} = 25°C, V_{DD} = 125 V, R_G = 25 Ω , L = 100 μ H, V_{GS} = 20 \rightarrow 0 V
 - **4.** $T_{ch(peak)} \le 150^{\circ}C$, L = 100 μH

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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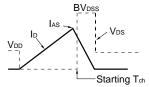
ELECTRICAL CHARACTERISTICS (TA = 25°C, unless otherwise noted. All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	loss	Vps = 250 V, Vgs = 0 V			10	μΑ
Gate Leakage Current	Igss	Vgs = ±30 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5	3.5	4.5	٧
Forward Transfer Admittance Note	yfs	V _{DS} = 10 V, I _D = 4.0 A	3	5		S
Drain to Source On-state Resistance Note	RDS(on)	Vgs = 10 V, ID = 4.0 A		0.34	0.45	Ω
Input Capacitance	Ciss	Vps = 10 V		570		pF
Output Capacitance	Coss	Vgs = 0 V		120		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		50		pF
com Turn-on Delay Time	td(on)	V _{DD} = 125 V, I _D = 4.0 A		12		ns
Rise Time	tr	Vgs = 10 V		9		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		28		ns
Fall Time	t _f			8		ns
Total Gate Charge	QG	V _{DD} = 200 V		17		nC
Gate to Source Charge	Qgs	V _G S = 10 V		3		nC
Gate to Drain Charge	Q _{GD}	ID = 8.0 A		9		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	IF = 8.0 A, VGS = 0 V		0.9	1.5	V
Reverse Recovery Time	trr	IF = 8.0 A, VGS = 0 V		140		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		610		nC

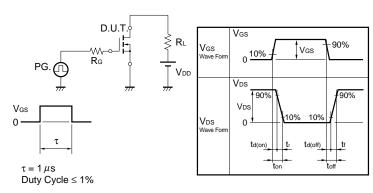
Note Pulsed: PW \leq 800 μ s, Duty Cycle \leq 2%

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = 20 \rightarrow 0 \text{ V}$ $PG. \quad PG. \quad PG. \quad V_{MM} = 25 \Omega \text{ PG}$ $PG. \quad PG. \quad$



TEST CIRCUIT 2 SWITCHING TIME



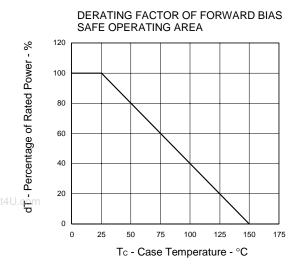
TEST CIRCUIT 3 GATE CHARGE

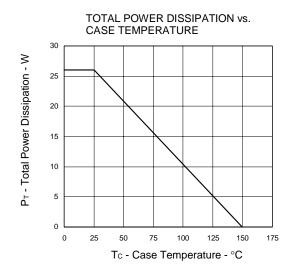
$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline \end{array}$$

$$\begin{array}{c|c} PG. & \\ \hline \end{array} \begin{array}{c} S & \\ \hline \end{array} \begin{array}{c} D.U.T. \\ \hline \end{array}$$

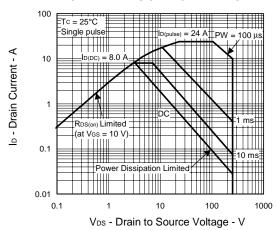
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TYPICAL CHARACTERISTICS (TA = 25°C, unless otherwise noted. All terminals are connected.)

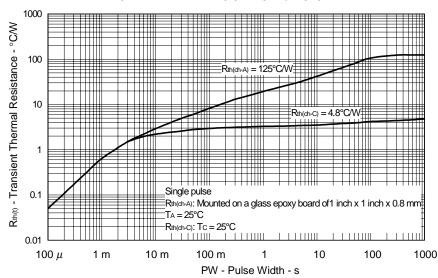




FORWARD BIAS SAFE OPERATING AREA

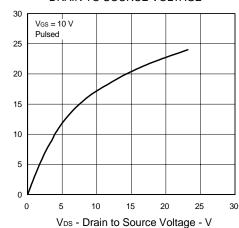


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

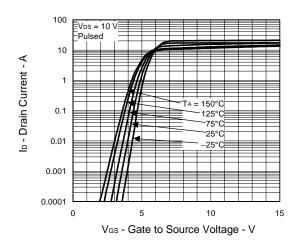


lo - Drain Current - A

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

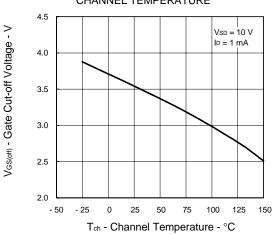


FORWARD TRANSFER CHARACTERISTICS

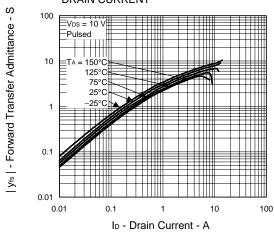


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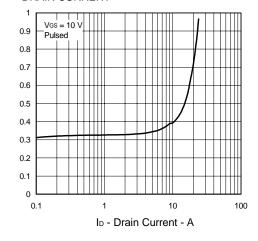
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



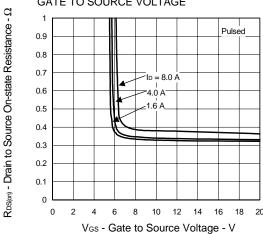
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

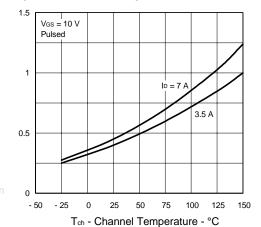


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

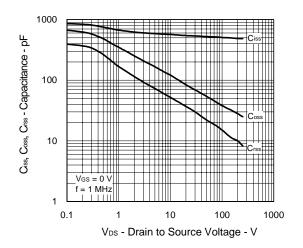


R_{DS(m)} - Drain to Source On-state Resistance - Ω

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

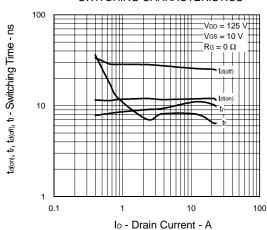


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

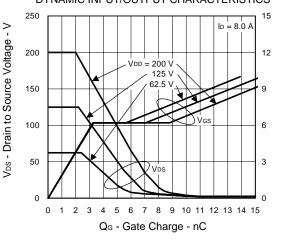


www.Drain to Source On-state Resistance - Ω

SWITCHING CHARACTERISTICS

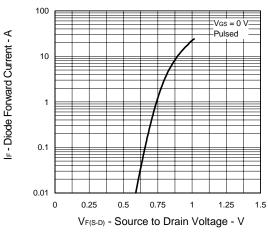


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

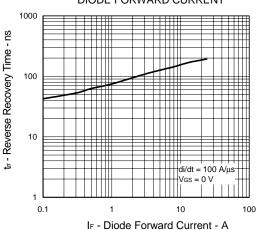


Ves - Gate to Source Voltage - V

SOURCE TO DRAIN DIODE FORWARD VOLTAGE

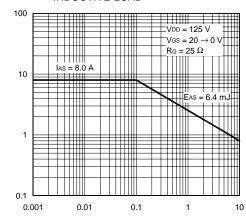


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



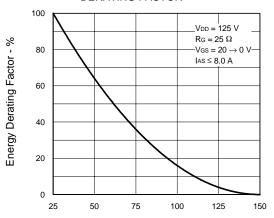
IAS - Single Avalanche Current - A

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



L - Inductive Load - mH

SINGLE AVALANCHE ENERGY DERATING FACTOR



Starting Tch - Starting Channel Temperature - °C

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