

SWITCHING
N-AND P-CHANNEL POWER MOS FET
INDUSTRIAL USE

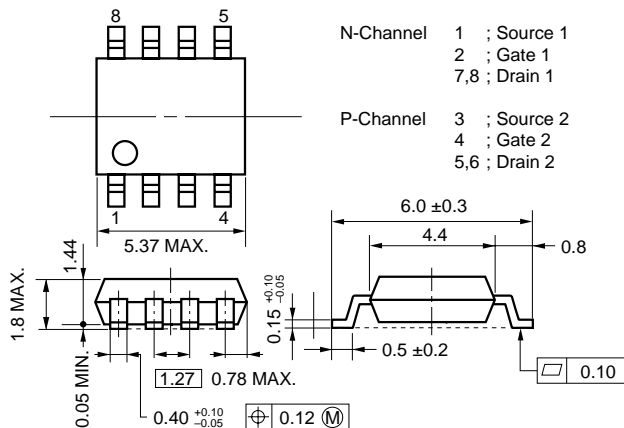
DESCRIPTION

This product is N-and P-Channel MOS Field Effect Transistor designed for motor driver applications.

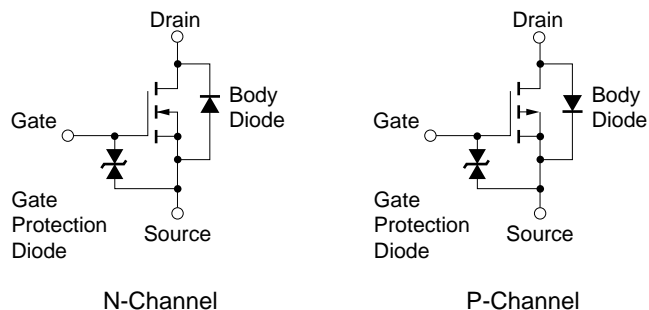
FEATURES

- Dual chip type
- Low on-resistance
N-Channel $R_{DS(on)1} = 0.12 \Omega$ TYP. ($V_{GS} = 10 V, I_D = 0.5 A$)
 $R_{DS(on)2} = 0.19 \Omega$ TYP. ($V_{GS} = 4 V, I_D = 0.5 A$)
P-Channel $R_{DS(on)1} = 0.45 \Omega$ TYP. ($V_{GS} = -10 V, I_D = -0.35 A$)
 $R_{DS(on)2} = 0.74 \Omega$ TYP. ($V_{GS} = -4 V, I_D = -0.35 A$)
- Low input capacitance
N-Channel $C_{iss} = 180 pF$ TYP.
P-Channel $C_{iss} = 230 pF$ TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



EQUIVALENT CIRCUIT



ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1790G	Power SOP8

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	60	-60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	∓ 20	V
Drain Current (DC)	I _{D(DC)}	±1.0	∓ 0.7	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±4.0	∓ 2.8	A
Total Power Dissipation (1 unit) ^{Note2}	P _T	1.7		W
Total Power Dissipation (2 unit) ^{Note2}	P _T	2.0		W
Channel Temperature	T _{ch}	150		°C
Storage Temperature	T _{stg}	-55 to +150		°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

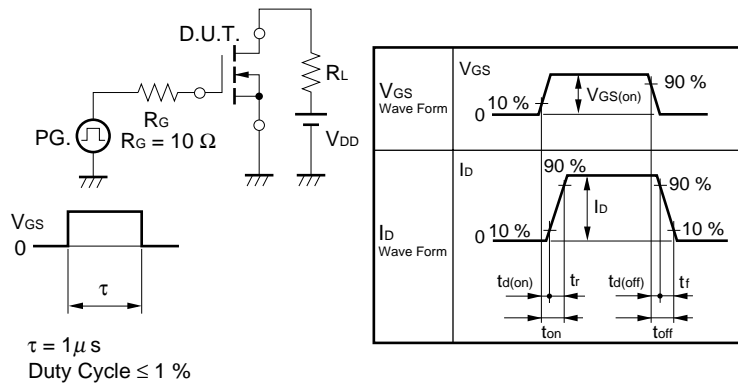
2. Mounted on ceramic substrate of 2000 mm² x 2.25 mm

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

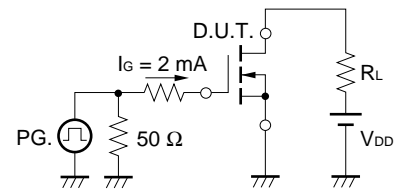
N-CHANNEL

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 0.5 A		0.12	0.26	Ω
	R _{DS(on)2}	V _{GS} = 4 V, I _D = 0.5 A		0.19	0.34	Ω
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.7	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 0.5 A	1.0	1.7		S
Drain Leakage Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		180		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		100		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		35		pF
Turn-on Delay Time	t _{d(on)}	I _D = 0.5 A		1		ns
Rise Time	t _r	V _{GS(on)} = 10 V		1.4		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 30 V		23		ns
Fall Time	t _f	R _G = 10 Ω		17		ns
Total Gate Charge	Q _G	I _D = 1.0 A		8		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 48 V		1		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		3.5		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 1.0 A, V _{GS} = 0 V		0.75		V
Reverse Recovery Time	t _{rr}	I _F = 1.0 A, V _{GS} = 0 V		30		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		33		nC

TEST CIRCUIT 1 SWITCHING TIME



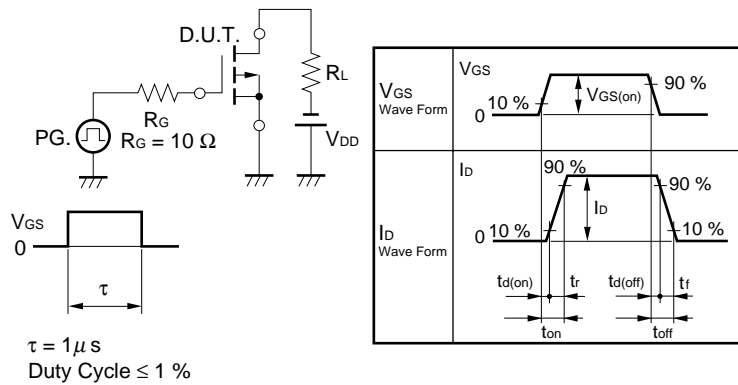
TEST CIRCUIT 2 GATE CHARGE



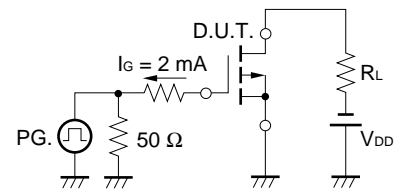
P-CHANNEL

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -0.35\text{ A}$		0.45	0.6	Ω
	$R_{DS(on)2}$	$V_{GS} = -4\text{ V}, I_D = -0.35\text{ A}$		0.74	1.1	Ω
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-1.0	-1.7	-2.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -0.35\text{ A}$	5.0			S
Drain Leakage Current	I_{DSS}	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$			-10	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \mp 16\text{ V}, V_{DS} = 0\text{ V}$			∓ 10	μA
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V}$		230		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		100		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		25		pF
Turn-on Delay Time	$t_{d(on)}$	$I_D = -0.35\text{ A}$		1.9		ns
Rise Time	t_r	$V_{GS(on)} = -10\text{ V}$		1.7		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{DD} = -30\text{ V}$		30		ns
Fall Time	t_f	$R_G = 10\ \Omega$		15		ns
Total Gate Charge	Q_G	$I_D = -0.7\text{ A}$		7.6		nC
Gate to Source Charge	Q_{GS}	$V_{DD} = -48\text{ V}$		1		nC
Gate to Drain Charge	Q_{GD}	$V_{GS} = -10\text{ V}$		2		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 0.7\text{ A}, V_{GS} = 0\text{ V}$		0.85		V
Reverse Recovery Time	t_{rr}	$I_F = 0.7\text{ A}, V_{GS} = 0\text{ V}$		58		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		130		nC

TEST CIRCUIT 1 SWITCHING TIME



TEST CIRCUIT 2 GATE CHARGE



[MEMO]

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