NEC

MOS FIELD EFFECT TRANSISTOR

μPA1793

SWITCHING
N- AND P-CHANNEL POWER MOS FET

DESCRIPTION

The μPA1793 is N- and P-Channel MOS Field Effect Transistors designed for Motor Drive application.

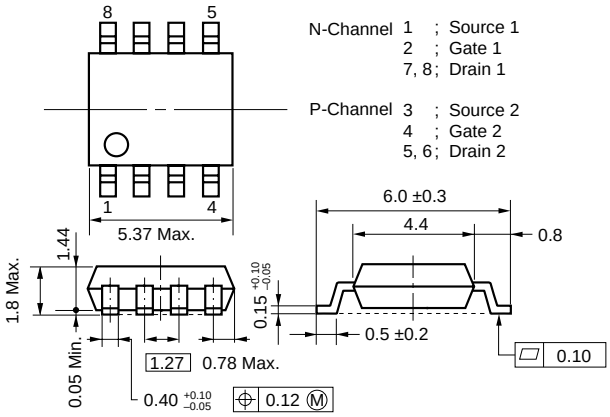
FEATURES

- Low on-state resistance
  - N-Channel $R_{DS(on)1}$ = 69 mΩ MAX. (V_{GS} = 4.5 V, I_D = 1.5 A)
  - $R_{DS(on)2}$ = 72 mΩ MAX. (V_{GS} = 4.0 V, I_D = 1.5 A)
  - $R_{DS(on)3}$ = 107 mΩ MAX. (V_{GS} = 2.5 V, I_D = 1.0 A)
  - P-Channel $R_{DS(on)1}$ = 115 mΩ MAX. (V_{GS} = –4.5 V, I_D = –1.5 A)
  - $R_{DS(on)2}$ = 120 mΩ MAX. (V_{GS} = –4.0 V, I_D = –1.5 A)
  - $R_{DS(on)3}$ = 190 mΩ MAX. (V_{GS} = –2.5 V, I_D = –1.0 A)
- Low input capacitance
  - N-Channel C_{iss} = 160 pF TYP.
  - P-Channel C_{iss} = 370 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

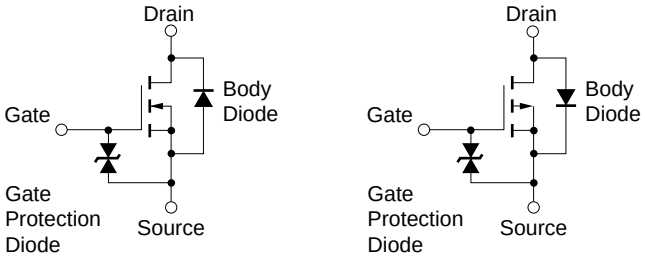
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1793G	Power SOP8

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	20	–20	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	± 12	∓ 12	V
Drain Current (DC)	$I_{D(DC)}$	± 3	∓ 3	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	± 12	∓ 12	A
Total Power Dissipation (1 unit) Note2	P_T	1.7		W
Total Power Dissipation (2 units) Note2	P_T	2.0		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	–55 to +150		°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

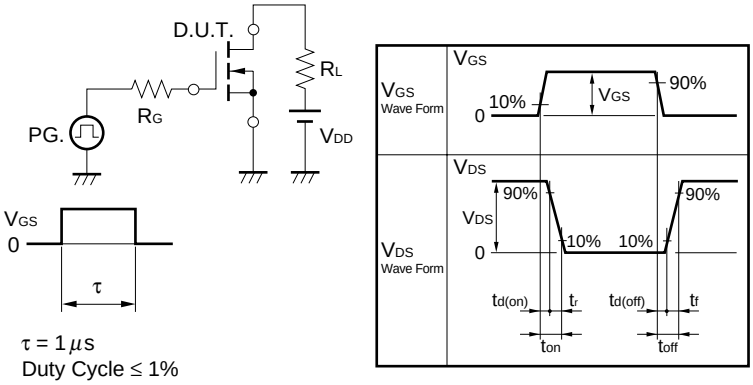
2. Mounted on ceramic substrate of 5500 $mm^2 \times 2.2$ mm, T_A = 25°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

A) N-Channel

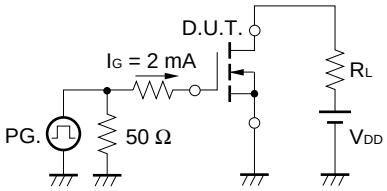
Characteristice	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	0.5	1.0	1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D =1.5 A	1.0			S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 4.5 V, I_D = 1.5 A		55	69	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 1.5 A		57	72	mΩ
	$R_{DS(on)3}$	V_{GS} = 2.5 V, I_D = 1.0 A		78	107	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		160		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		60		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		40		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 10 V, I_D = 1.5 A		17		ns
Rise Time	t_r	V_{GS} = 4.0 V		50		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		86		ns
Fall Time	t_f			80		ns
Total Gate Charge	Q_G	V_{DD} = 16 V		3.1		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 4.0 V		0.7		nC
Gate to Drain Charge	Q_{GD}	I_D = 3.0 A		1.4		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 3.0 A, V_{GS} = 0 V		0.86		V
Reverse Recovery Time	t_{rr}	I_F = 3 A, V_{GS} = 0 V		70		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		12		nC

TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

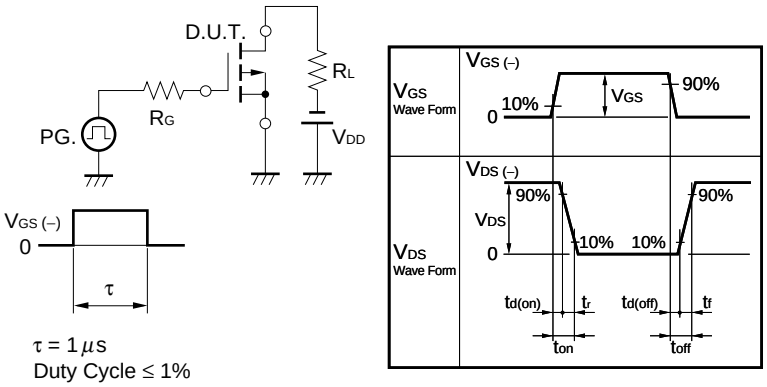
TEST CIRCUIT 2 GATE CHARGE



B) P-Channel

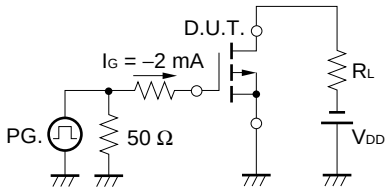
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓ 12 V, V_{DS} = 0 V			∓ 10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–0.5	–1.0	–1.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –1.5 A	1.0			S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –4.5 V, I_D = –1.5 A		75	115	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.0 V, I_D = –1.5 A		80	120	mΩ
	$R_{DS(on)3}$	V_{GS} = –2.5 V, I_D = –1.0 A		116	190	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		370		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		110		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		40		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –10 V, I_D = –1.5 A		120		ns
Rise Time	t_r	V_{GS} = –4.0 V		260		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		410		ns
Fall Time	t_f			360		ns
Total Gate Charge	Q_G	V_{DD} = –10 V		3.4		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –4.0 V		1.3		nC
Gate to Drain Charge	Q_{GD}	I_D = –3.0 A		1.6		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 3.0 A, V_{GS} = 0 V		0.86		V
Reverse Recovery Time	t_{rr}	I_F = 3 A, V_{GS} = 0 V		24		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 10 A/μs		1.5		nC

TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

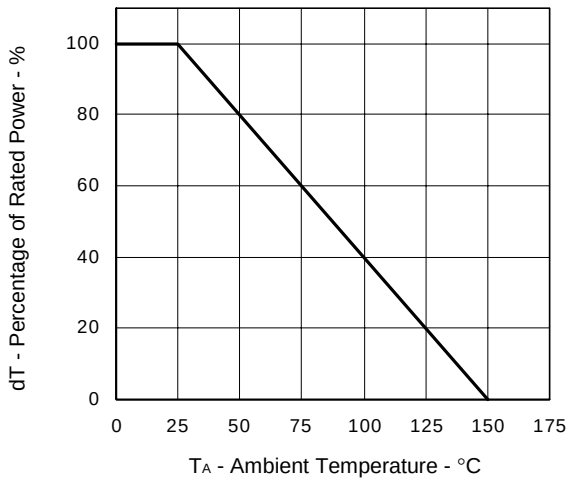
TEST CIRCUIT 2 GATE CHARGE



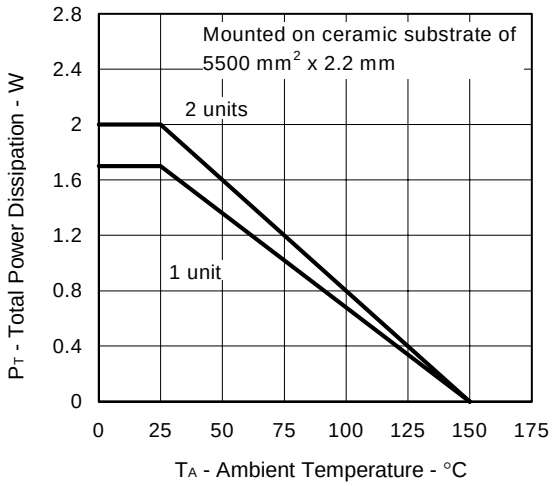
TYPICAL CHARACTERISTICS (T_A = 25°C)

A) N-Channel

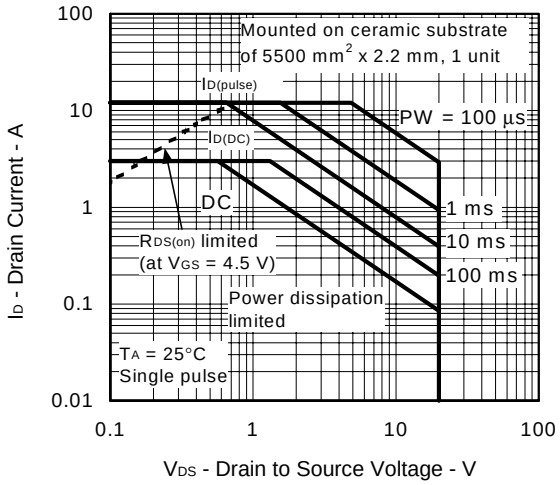
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



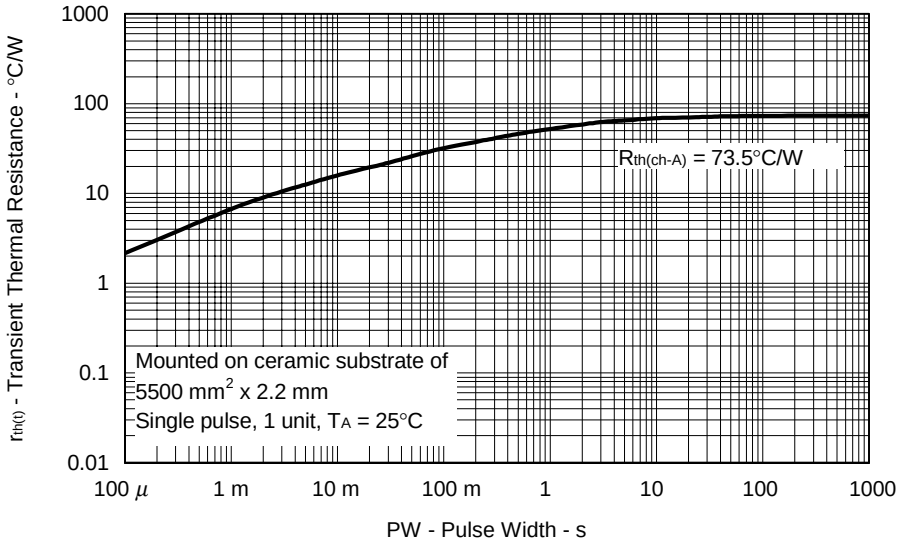
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA

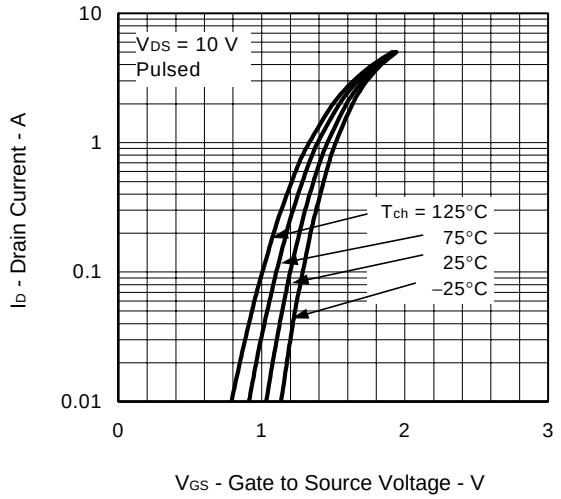


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

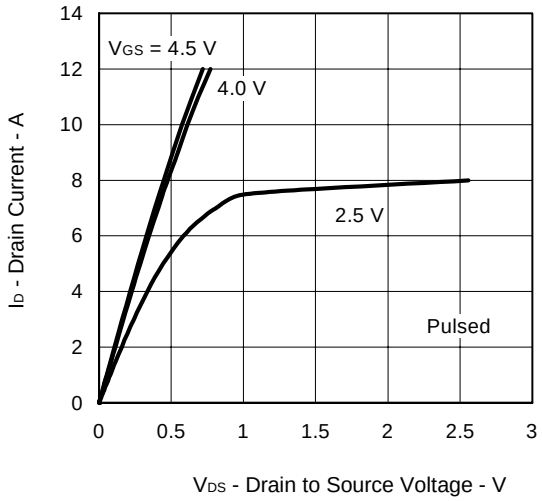


A) N-Channel

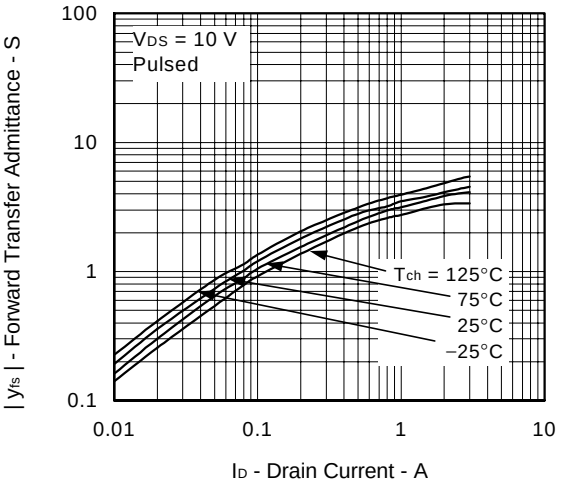
FORWARD TRANSFER CHARACTERISTICS



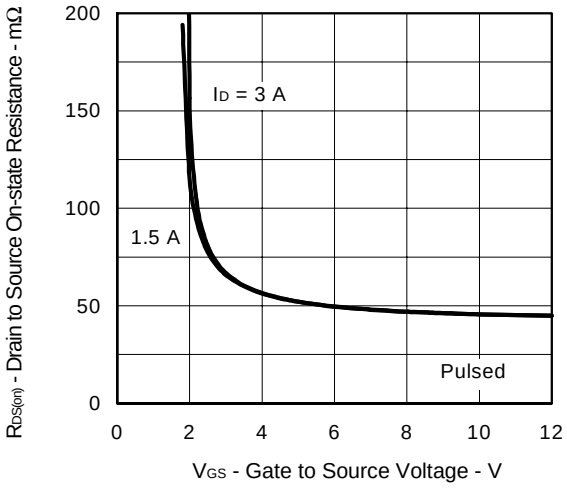
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



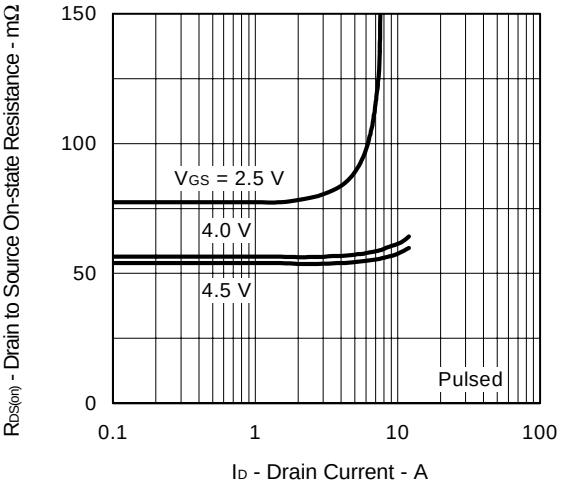
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



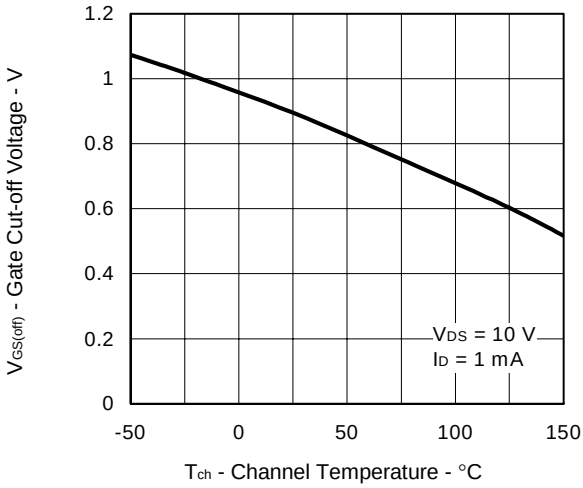
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT

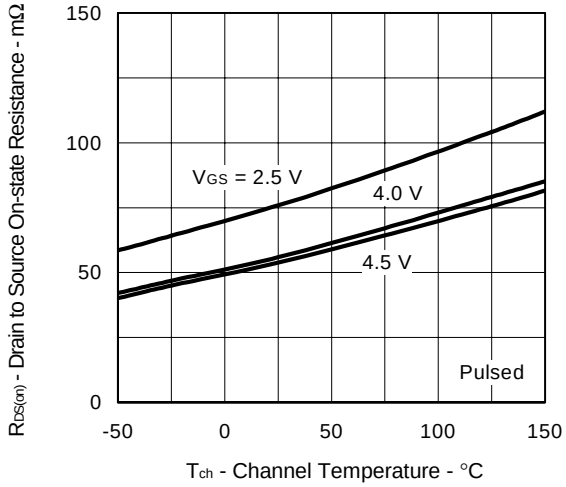


GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE

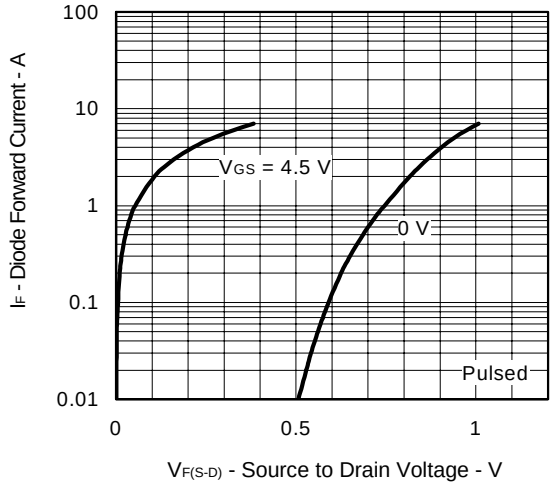


A) N-Channel

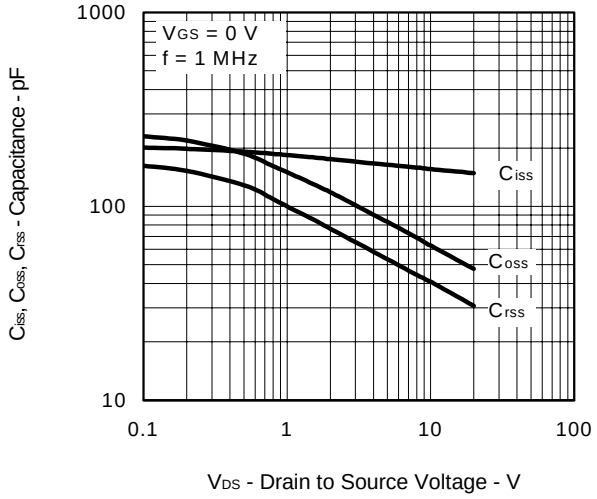
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



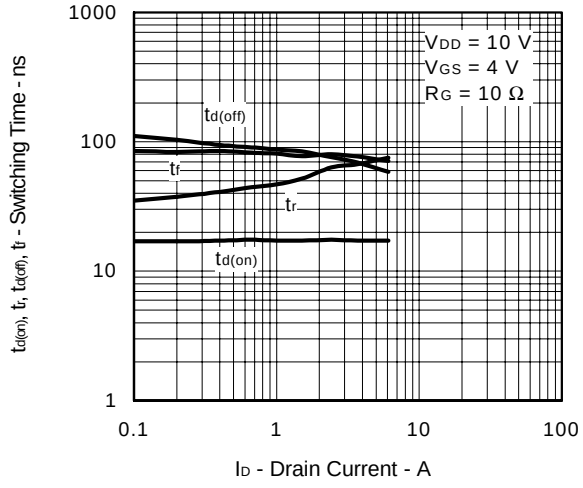
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



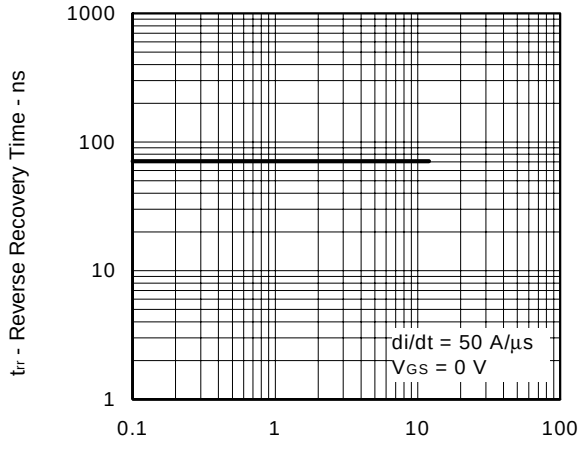
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



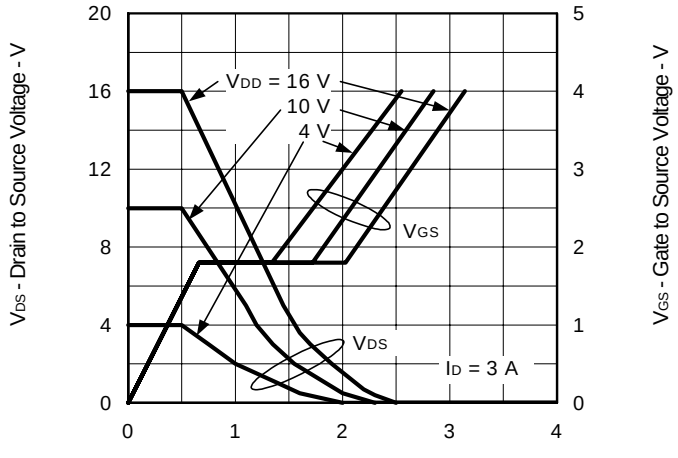
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

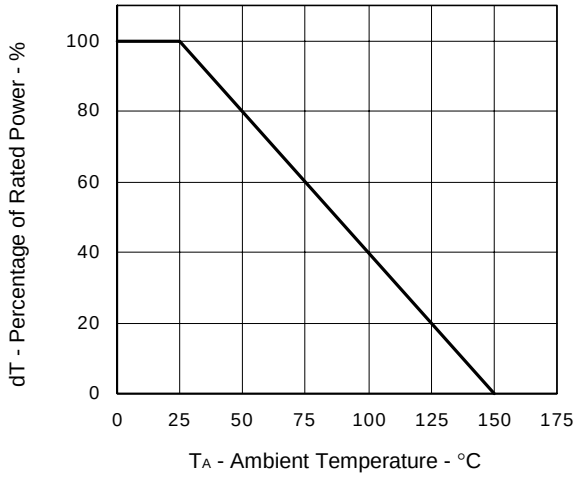


DYNAMIC INPUT/OUTPUT CHARACTERITICS

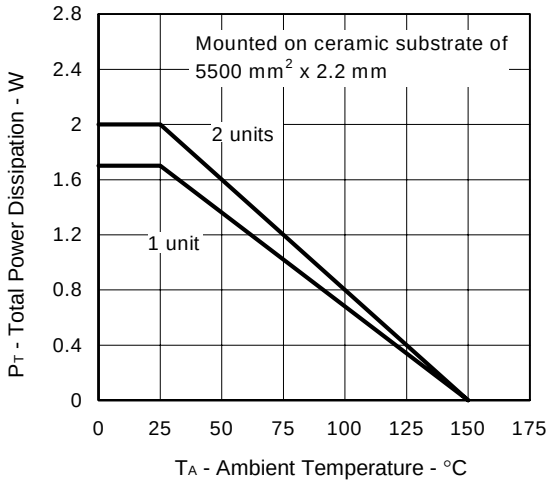


B) P-Channel

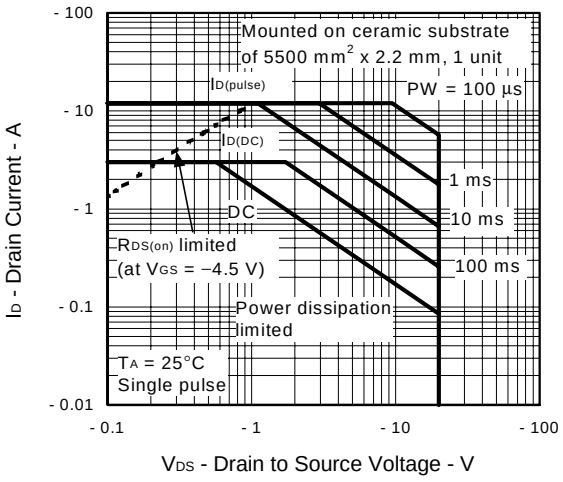
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



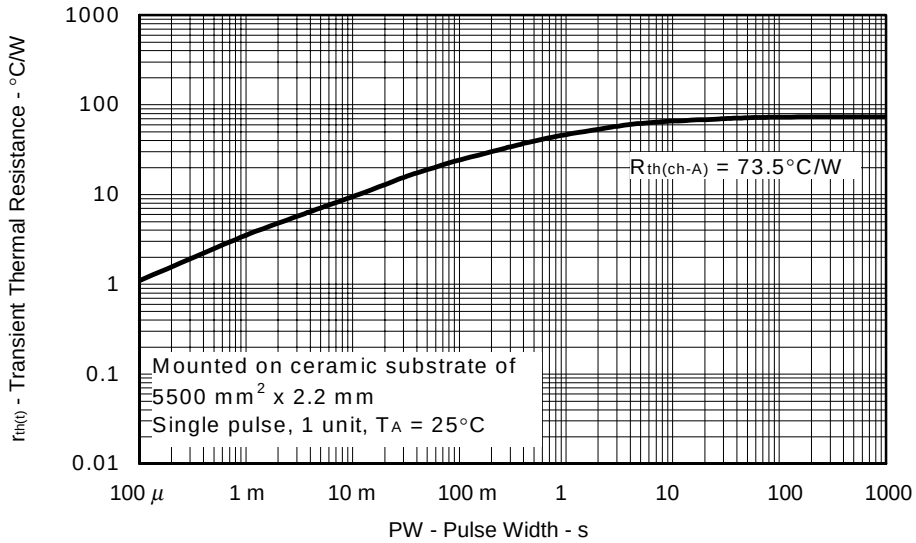
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA

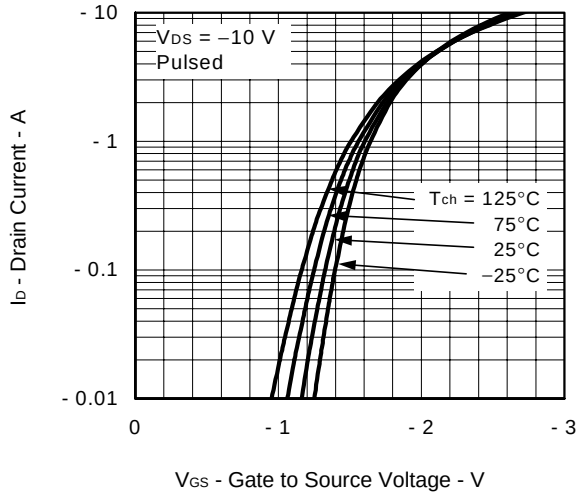


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

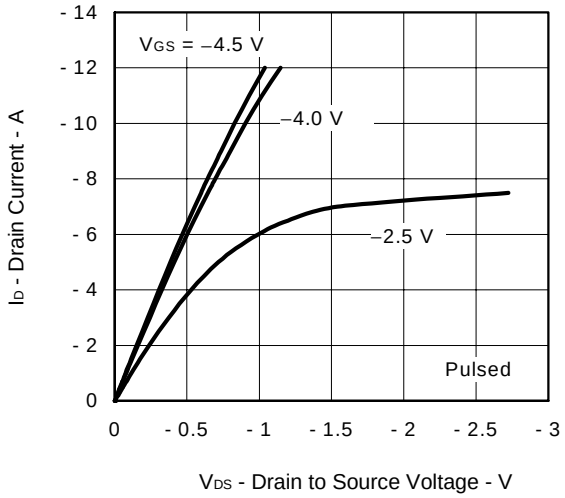


B) P-Channel

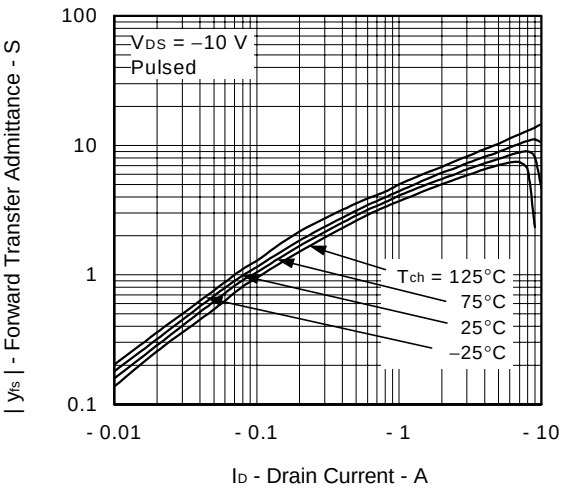
FORWARD TRANSFER CHARACTERISTICS



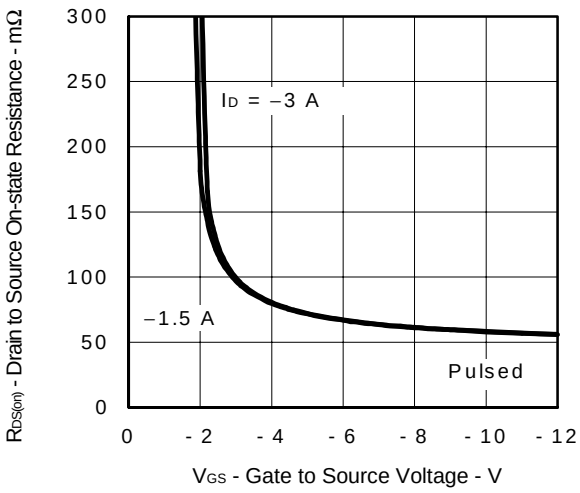
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



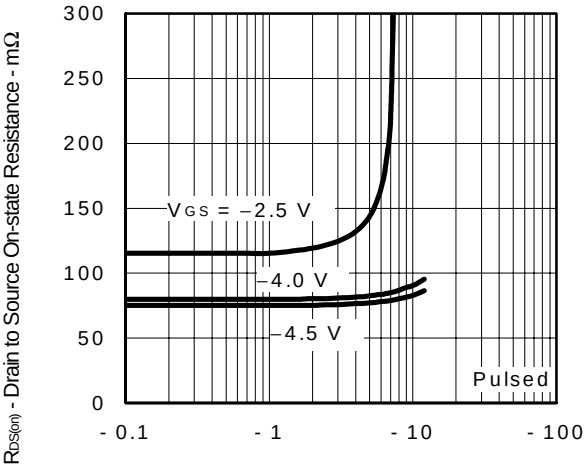
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



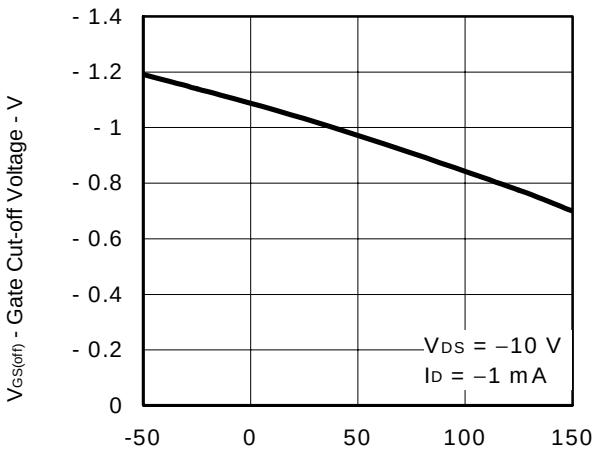
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT

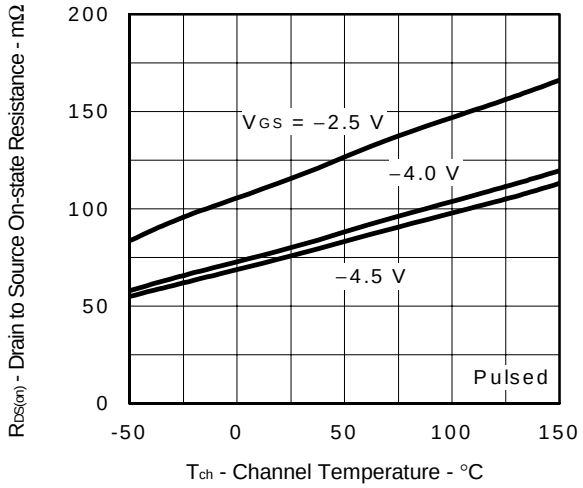


GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE

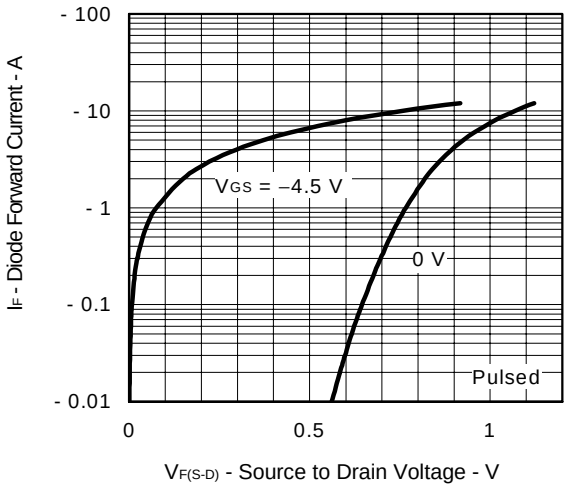


) P-Channel

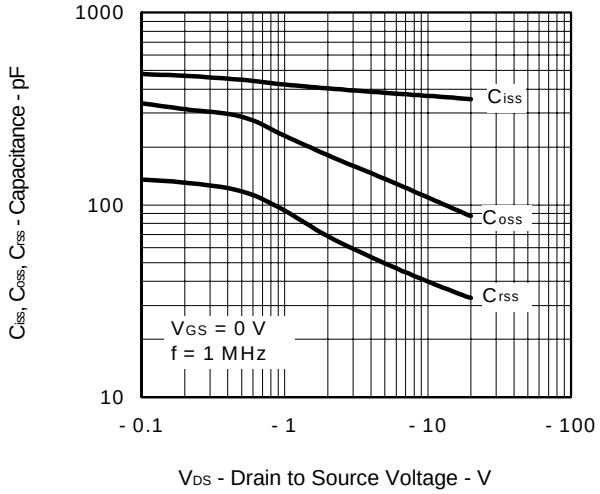
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



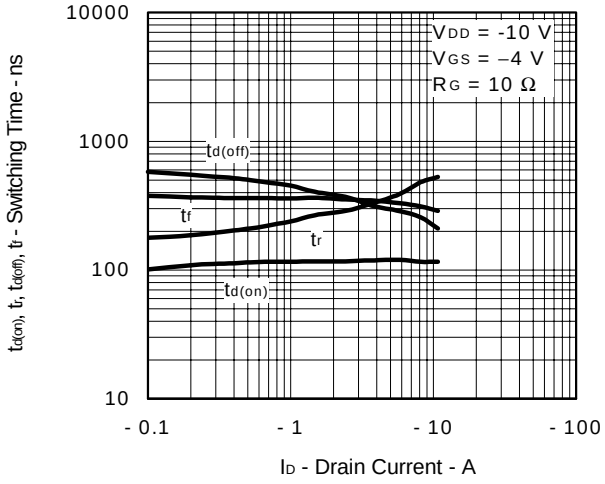
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



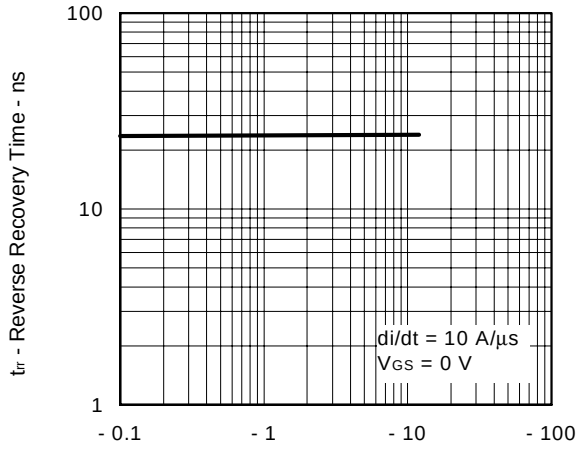
CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



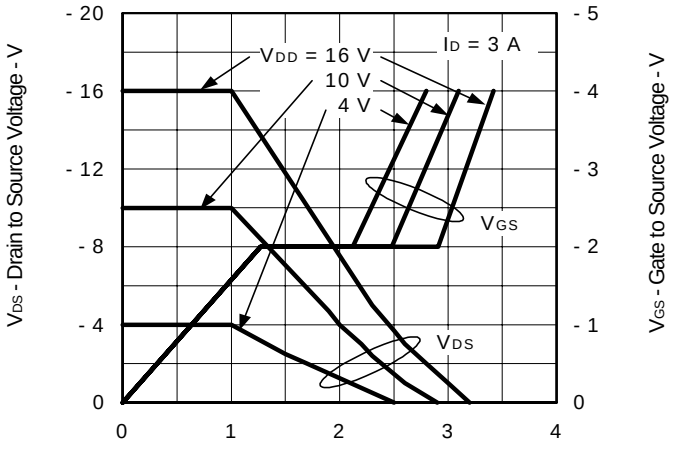
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERITICS



[MEMO]

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