DATA SHEET

MOS FIELD EFFECT TRANSISTOR
μPA2200T1M

N-CHANNEL MOS FET
FOR SWITCHING

DESCRIPTION

The μPA2200T1M is N-channel MOS Field Effect Transistor designed for power management applications of portable equipments, such as load switch.

FEATURES

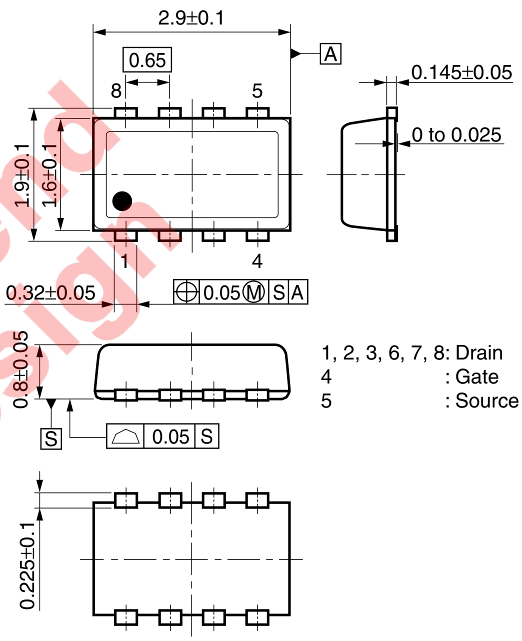
- Low on-state resistance
  $R_{DS(on)1}$ = 23 mΩ MAX. (V_{GS} = 10 V, I_D = 8 A)
  $R_{DS(on)2}$ = 31 mΩ MAX. (V_{GS} = 4.5 V, I_D = 4 A)
- Built-in gate protection diode
- 4.5 V Gate drive available

ORDERING INFORMATION

PART NUMBER	PACKING	PACKAGE
μPA2200T1M-T1-AT Note	8 mm embossed taping	8-pin VSOF (1629)
μPA2200T1M-T2-AT Note	3000 p/reel	0.011 g TYP.

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

PACKAGE DRAWING (Unit: mm)

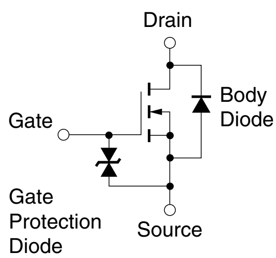


ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±8	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±32	A
Total Power Dissipation Note2	P_{T1}	1.1	W
Total Power Dissipation (PW = 5 sec) Note2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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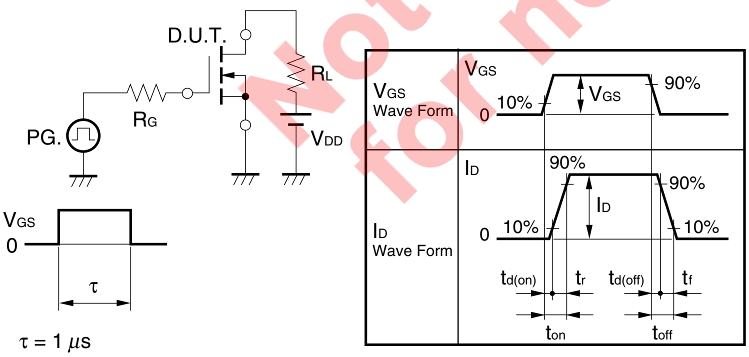
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0		2.5	V
Forward Transfer Admittance Note	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 4 A	3			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 8 A		18	23	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 4 A		23	31	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V,		870		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		160		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		80		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 4 A,		9.2		ns
Rise Time	t_r	V_{GS} = 10 V,		3.4		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		31.7		ns
Fall Time	t_f			5.3		ns
Total Gate Charge	Q_G	V_{DD} = 24 V,		8.7		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5 V,		3.0		nC
Gate to Drain Charge	Q_{GD}	I_D = 8 A		3.2		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 8 A, V_{GS} = 0 V		0.85	1.2	V
Reverse Recovery Time	t_{rr}	I_F = 8 A, V_{GS} = 0 V,		22		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		15		nC

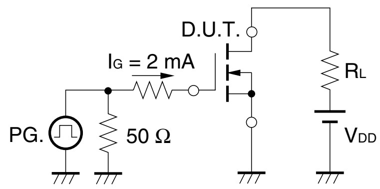
Note Pulsed

TEST CIRCUIT 1 SWITCHING TIME



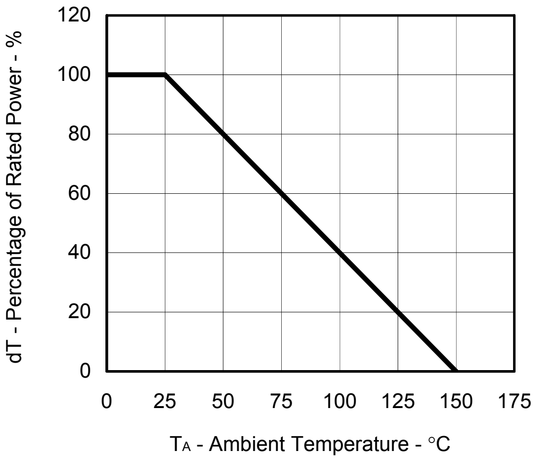
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE

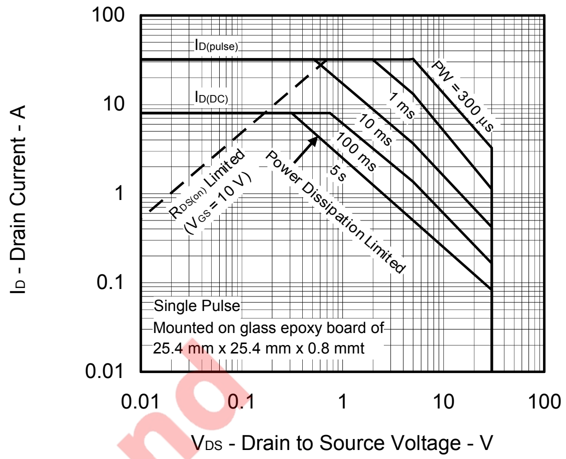


TYPICAL CHARACTERISTICS (T_A = 25°C)

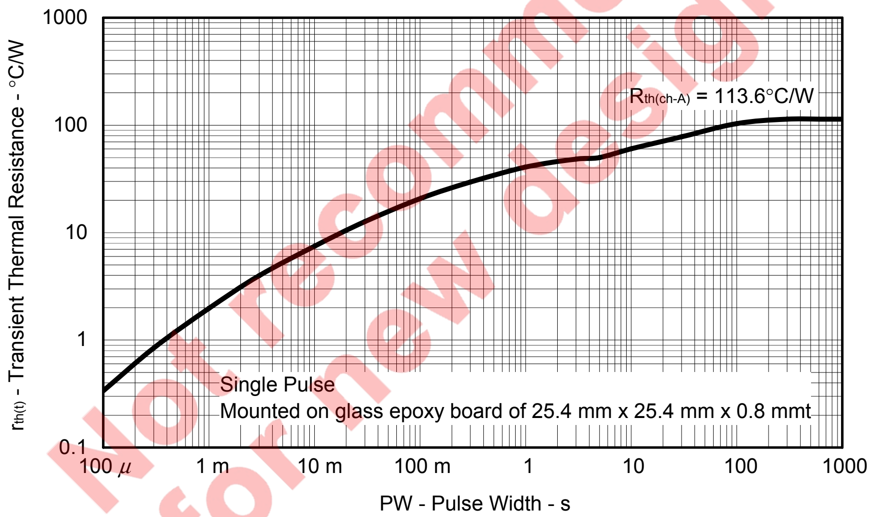
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



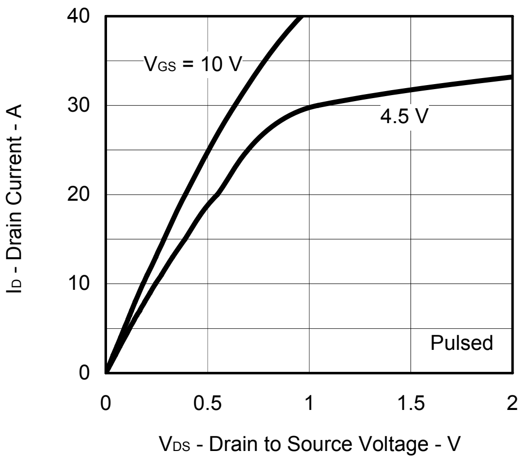
FORWARD BIAS SAFE OPERATING AREA



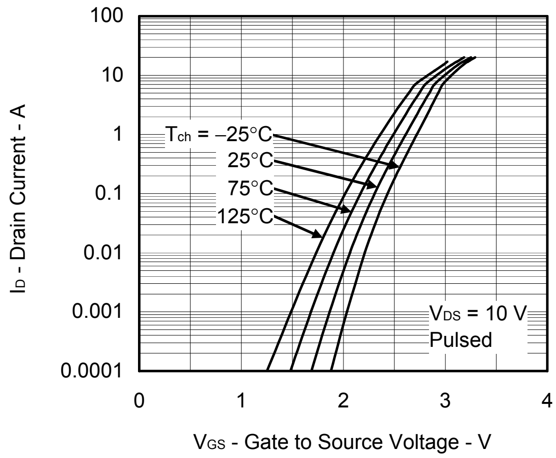
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



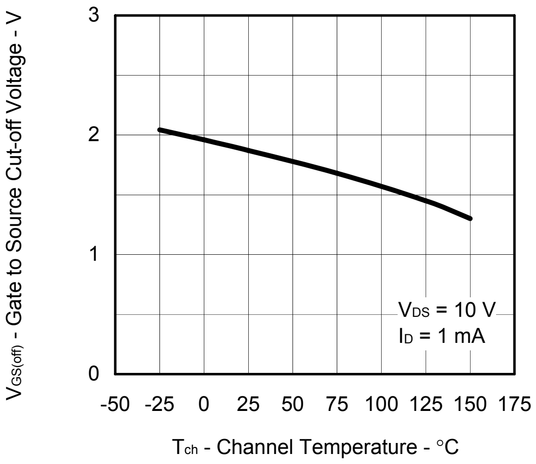
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



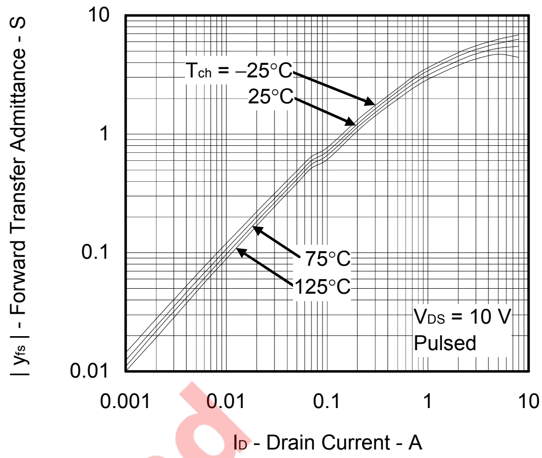
FORWARD TRANSFER CHARACTERISTICS



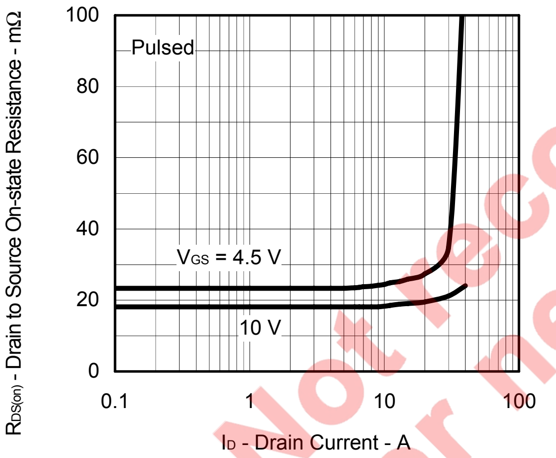
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



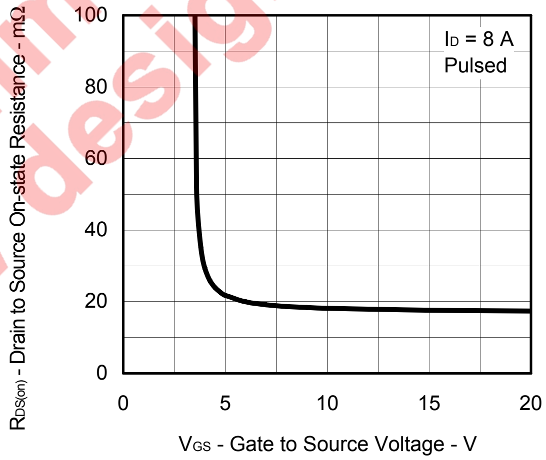
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



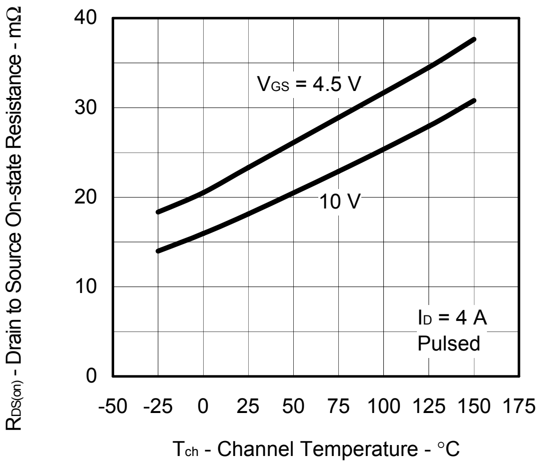
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



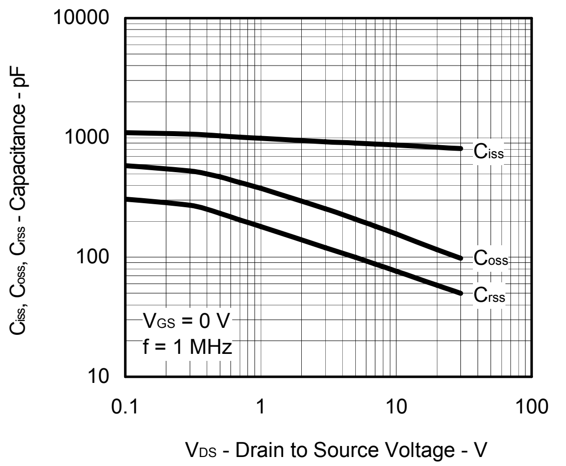
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



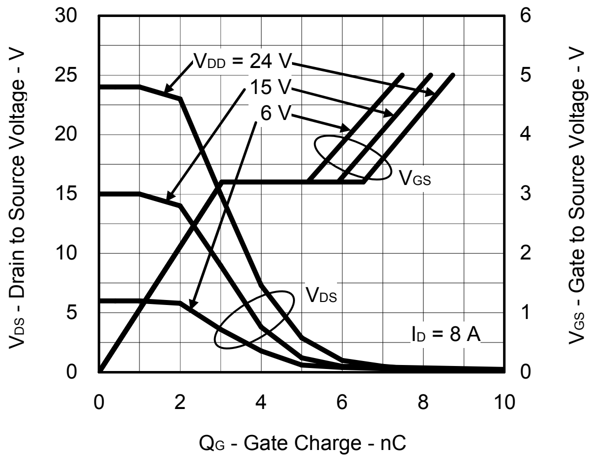
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE