# MOS FIELD EFFECT TRANSISTOR $\mu PA2451B$

# N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

### DESCRIPTION

NEC

The  $\mu$  PA2451B is a switching device, which can be driven directly by a 2.5 V power source.

The  $\mu$  PA2451B features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

# FEATURES

- 2.5 V drive available
- Low on-state resistance  $R_{DS(on)1} = 20.0 \text{ } m\Omega \text{ } MAX. \text{ } (V_{GS} = 4.5 \text{ } \text{V}, \text{ } \text{I}_{D} = 4.0 \text{ } \text{A})$   $R_{DS(on)2} = 21.0 \text{ } m\Omega \text{ } MAX. \text{ } (V_{GS} = 4.0 \text{ } \text{V}, \text{ } \text{I}_{D} = 4.0 \text{ } \text{A})$   $R_{DS(on)3} = 25.0 \text{ } m\Omega \text{ } MAX. \text{ } (V_{GS} = 3.1 \text{ } \text{V}, \text{ } \text{I}_{D} = 4.0 \text{ } \text{A})$  $R_{DS(on)4} = 32.0 \text{ } m\Omega \text{ } MAX. \text{ } (V_{GS} = 2.5 \text{ } \text{V}, \text{ } \text{I}_{D} = 4.0 \text{ } \text{A})$
- Built-in G-S protection diode against ESD

## ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA2451BTL	6PIN HWSON (4521)

### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGS = 0 V)	VDSS	30.0	
Gate to Source Voltage (VDS = 0 V)	Vgss	±12.0	
Drain Current (DC) Note1	D(DC)	±8.2	
Drain Current (pulse) <sup>Note2</sup>	D(pulse)	±65.0	
Total Power Dissipation (2 units) Note1	PT1	2.5	
Total Power Dissipation (2 units) Note3	Pt2	0.7	
Channel Temperature	Tch	150	
Storage Temperature	Tstg	–55 to +150	

Notes 1. Mounted on ceramic board of 50 cm<sup>2</sup> x 1.1 mm

- **2.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%
- 3. Mounted on FR-4 board of 50 cm<sup>2</sup> x 1.1 mm
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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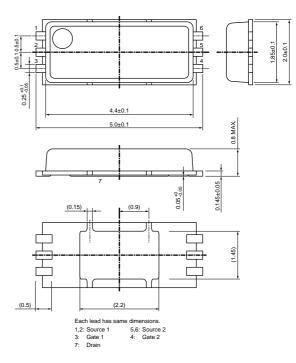
°C

°C

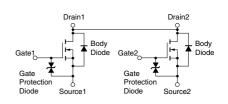
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### PACKAGE DRAWING (Unit: mm)



# EQUIVALENT CIRCUIT

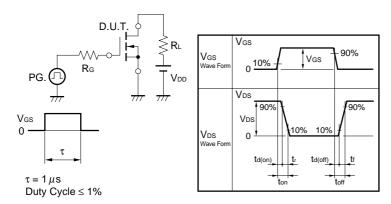


CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 30.0 V, V <sub>GS</sub> = 0 V			1.0	μA
Gate Leakage Current	lgss	V <sub>GS</sub> = ±12.0 V, V <sub>DS</sub> = 0 V			±10.0	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10.0 V, I <sub>D</sub> = 1.0 mA	0.50		1.50	V
Forward Transfer Admittance Note	y <sub>fs</sub>	V <sub>DS</sub> = 10.0 V, I <sub>D</sub> = 4.0 A	3.5			S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.0 A	12.0	15.0	20.0	mΩ
	RDS(on)2	$V_{GS}$ = 4.0 V, I <sub>D</sub> = 4.0 A	12.5	15.5	21.0	mΩ
	RDS(on)3	V <sub>GS</sub> = 3.1 V, I <sub>D</sub> = 4.0 A	14.0	17.5	25.0	mΩ
	RDS(on)4	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 4.0 A	15.5	22.0	32.0	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10.0 V		540		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		100		pF
Reverse Transfer Capacitance	Crss	f = 1.0 MHz		70		pF
Turn-on Delay Time	td(on)	V <sub>DD</sub> = 15.0 V, I <sub>D</sub> = 4.0 A		20		ns
Rise Time	tr	V <sub>GS</sub> = 4.0 V		80		ns
Turn-off Delay Time	td(off)	R <sub>G</sub> = 6 Ω		131		ns
Fall Time	tr			89		ns
Total Gate Charge	QG	V <sub>DD</sub> = 24.0 V		9.2		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 4.0 V		1.7		nC
Gate to Drain Charge	Qgd	I <sub>D</sub> = 8.2 A		4.1		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 8.2 A, VGS = 0 V		0.83		V
Reverse Recovery Time	trr	IF = 8.2 A, VGS = 0 V		64		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		36		nC

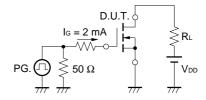
# ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

**Note** Pulsed: PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

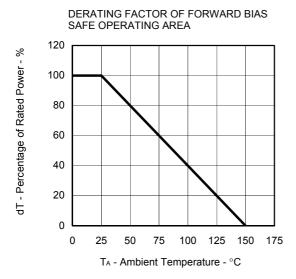
# TEST CIRCUIT 1 SWITCHING TIME



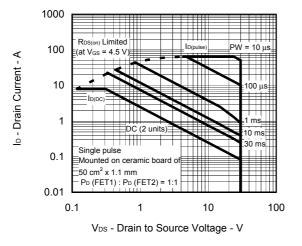
### **TEST CIRCUIT 2 GATE CHARGE**

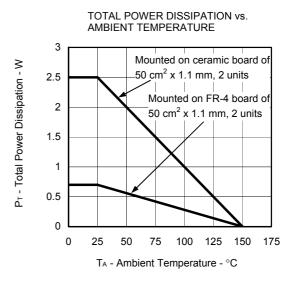


# ELECTRICAL CHARACTERISTICS (TA = 25°C)

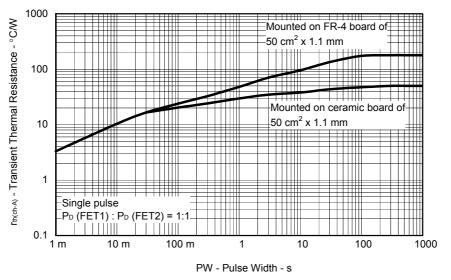








### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



Data Sheet G16636EJ1V0DS

1.4

1.2

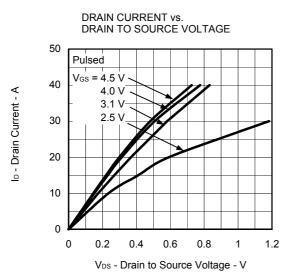
1

0.8

0.6

0.4 -50

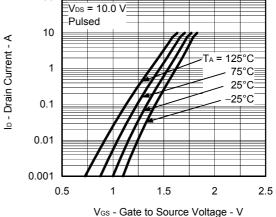
V<sub>GS(off</sub>) - Gate Cut-off Voltage - V



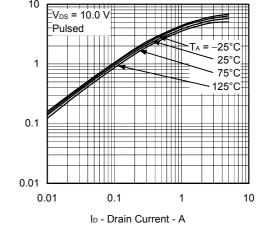
GATE CUT-OFF VOLTAGE vs.

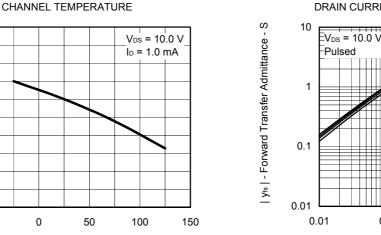
FORWARD TRANSFER CHARACTERISTICS

100



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

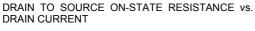


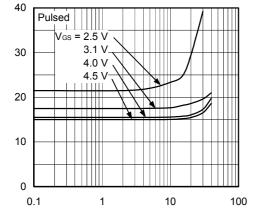


50 Tch - Channel Temperature - °C

0

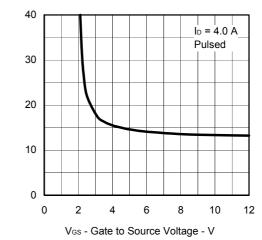




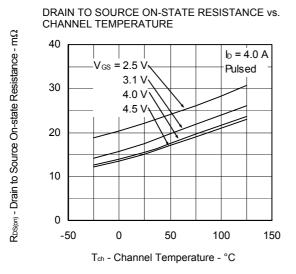


ID - Drain Current - A

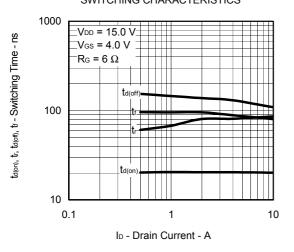
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



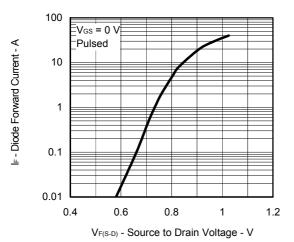
 $R_{DS(on)}$  - Drain to Source On-state Resistance -  $m\Omega$ 



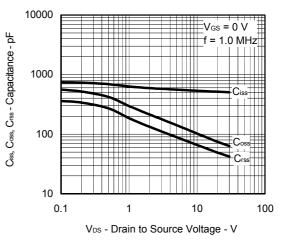
SWITCHING CHARACTERISTICS



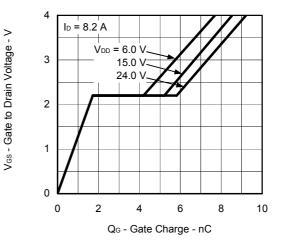
SOURCE TO DRAIN DIODE FORWARD VOLTAGE







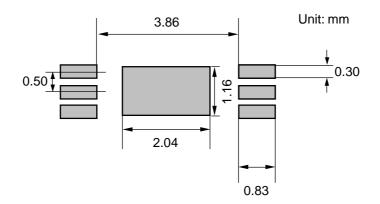
DYNAMIC INPUT CHARACTERISTICS



### <Notes for using this device safely>

When you use this device, in order to prevent a customer's hazard and damage, use it with understanding the following contents. If used exceeding recommended conditions, there is a possibility of causing failure of the device and characteristic degradation.

- 1. When you mount the device on a substrate, carry out within our recommended soldering conditions of infrared reflow. If mounted exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.
- 2. When you wash the device mounted the substrate, carry out within our recommended conditions. If washed exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.
- 3. When you use ultrasonic wave to substrate after the device mounting, prevent from touching a resonance generator directly. If it touches, the characteristic of a device may be degraded and it may result in failure.
- 4. Please refer to **Figure 1** as an example of the land pattern. Optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.



### Figure 1. Example of the land pattern

5. This device is very thin device and should be handled with caution for mechanical stress. The rate of distortion applied to the device should become below 2000  $\mu\epsilon$ .<sup>Note1</sup> If the rate of distortion exceeds 2000  $\mu\epsilon$ , the characteristic of a device may be degraded and it may result in failure.

### Figure 2. Direction of substrate and stress

The substrate that mounted the device is on a stand with a support width of 24 mm. The device is turned downward. The stress is applied from a top.

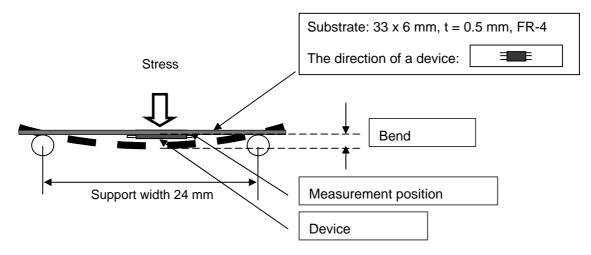
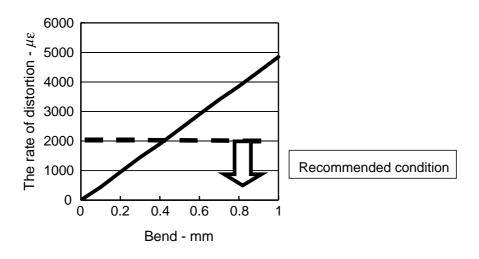


Figure 3. Example of the bend and the rate of distortion Note2



- Note 1. Definition of rate of distortion (written as  $\boldsymbol{\epsilon}$  in this document)
  - $\epsilon = (I I_0)/I_0$
  - lo: Distance for two arbitrary points before receiving stress.
  - I: Distance above-mentioned when receiving stress.
  - 2. The relation of the distortion and the bend changes with several conditions, such as a size of substrate and so on.

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