

DATA SHEET

NEC**MOS FIELD EFFECT TRANSISTOR**
 μ PA2451C**N-CHANNEL MOS FIELD EFFECT TRANSISTOR**
FOR SWITCHING**DESCRIPTION**

The μ PA2451C is a switching device, which can be driven directly by a 2.5 V power source.

The μ PA2451C features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

- 2.5 V drive available
- Low on-state resistance
 - $R_{DS(on)1} = 20.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 4.5 \text{ V}$, $I_D = 4.0 \text{ A}$)
 - $R_{DS(on)2} = 21.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 4.0 \text{ V}$, $I_D = 4.0 \text{ A}$)
 - $R_{DS(on)3} = 25.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 3.1 \text{ V}$, $I_D = 4.0 \text{ A}$)
 - $R_{DS(on)4} = 32.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 2.5 \text{ V}$, $I_D = 4.0 \text{ A}$)
- Built-in G-S protection diode against ESD

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30.0	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 12.0	V
Drain Current (DC) ^{Note1}	$I_{D(DC)}$	± 8.2	A
Drain Current (pulse) ^{Note2}	$I_{D(pulse)}$	± 60.0	A
Total Power Dissipation (2 units) ^{Note1}	P_{T1}	2.5	W
Total Power Dissipation (2 units) ^{Note3}	P_{T2}	0.7	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes**
1. Mounted on ceramic board of $50 \text{ cm}^2 \times 1.1 \text{ mm}$
 2. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$
 3. Mounted on FR-4 board of $50 \text{ cm}^2 \times 1.1 \text{ mm}$

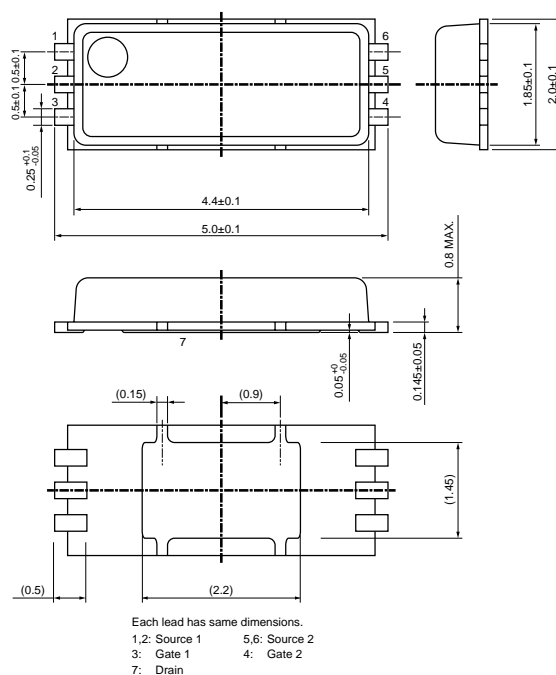
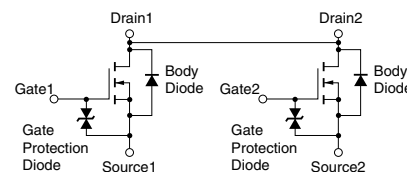
ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2451CTL-E1-A ^{Note}	Sn-Bi	Reel	6PIN HWSON (4521)
μ PA2451CTL-E2-A ^{Note}		3000 p/reel	

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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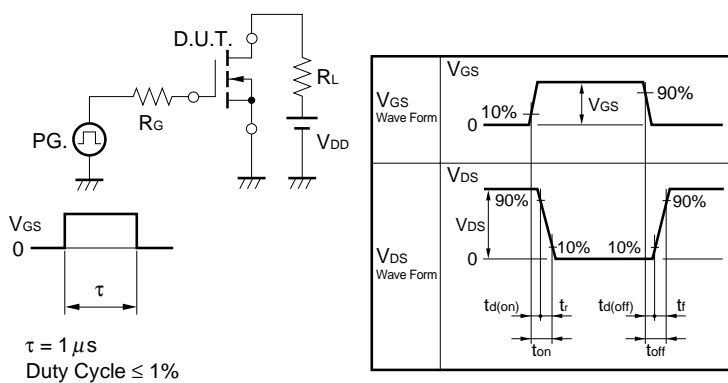
PACKAGE DRAWING (Unit: mm)**EQUIVALENT CIRCUIT**

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

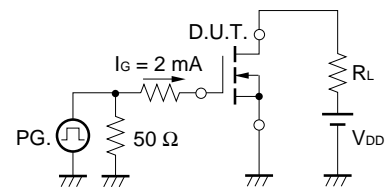
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30.0 V, V _{GS} = 0 V			1.0	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±12.0 V, V _{DS} = 0 V			±10.0	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10.0 V, I _D = 1.0 mA	0.50		1.50	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10.0 V, I _D = 4.0 A	6.0			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 4.5 V, I _D = 4.0 A	12.0	17.5	20.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.0 V, I _D = 4.0 A	12.5	18.0	21.0	mΩ
	R _{DS(on)3}	V _{GS} = 3.1 V, I _D = 4.0 A	14.0	21.0	25.0	mΩ
	R _{DS(on)4}	V _{GS} = 2.5 V, I _D = 4.0 A	15.5	25.5	32.0	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10.0 V,		605		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		87		pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz		40		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15.0 V,		40		ns
Rise Time	t _r	I _D = 4.0 A,		75		ns
Turn-off Delay Time	t _{d(off)}	V _{GS} = 4.0 V,		140		ns
Fall Time	t _f	R _G = 6 Ω		85		ns
Total Gate Charge	Q _G	V _{DD} = 24.0 V,		6.3		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 4.0 V,		1.5		nC
Gate to Drain Charge	Q _{GD}	I _D = 8.2 A		2.3		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 8.2 A, V _{GS} = 0 V		0.86		V

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

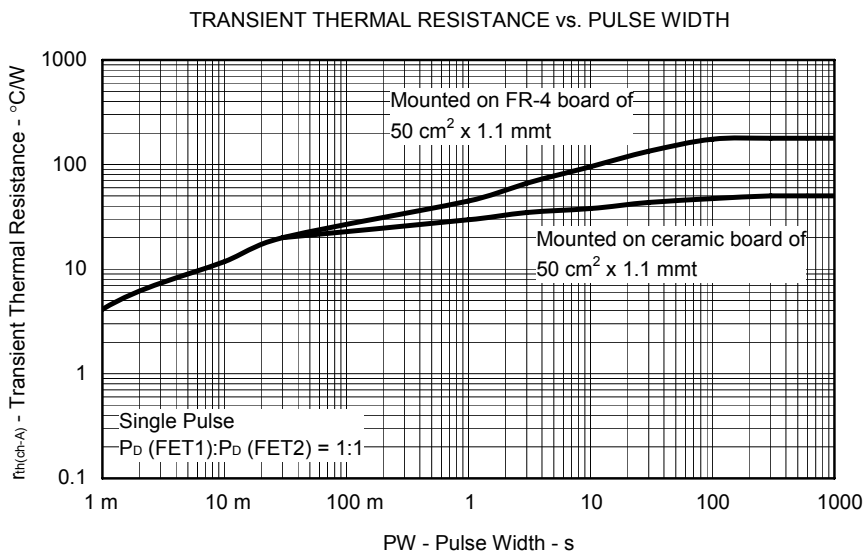
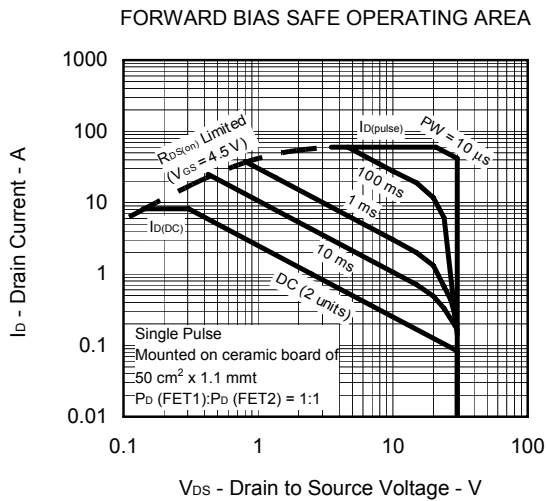
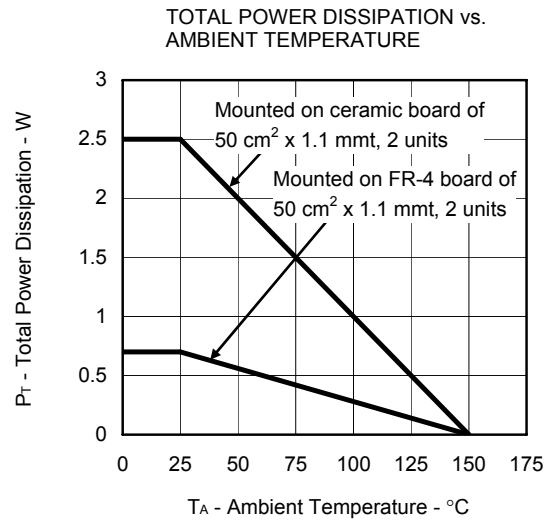
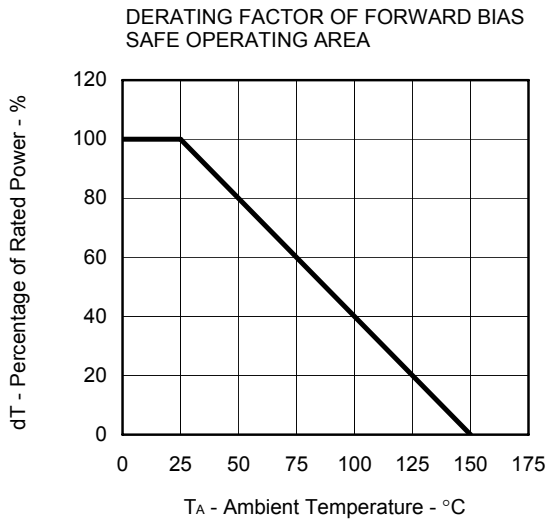
TEST CIRCUIT 1 SWITCHING TIME



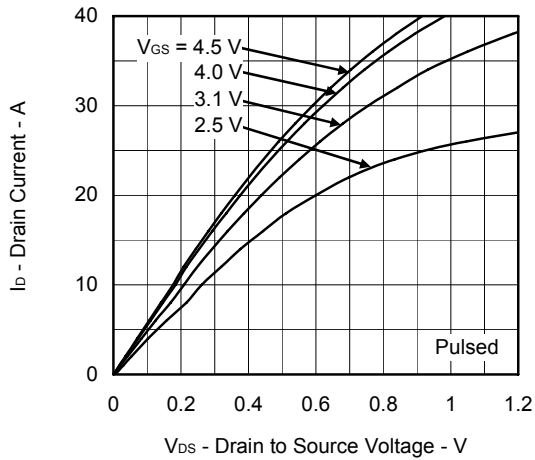
TEST CIRCUIT 2 GATE CHARGE



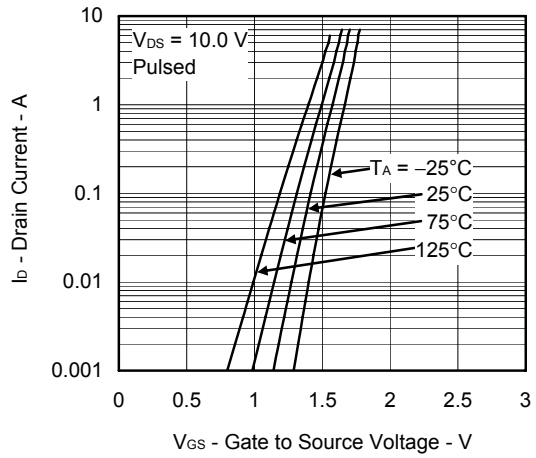
ELECTRICAL CHARACTERISTICS (T_A = 25°C)



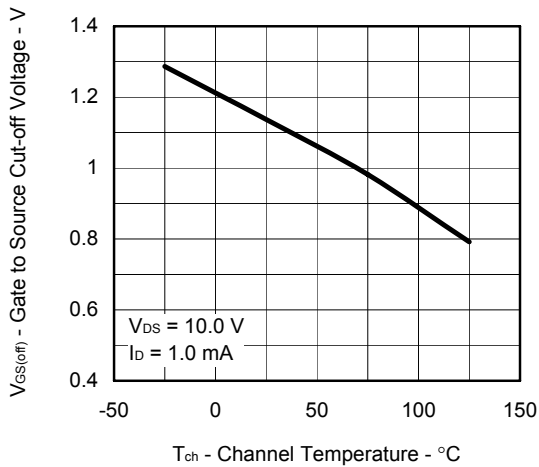
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



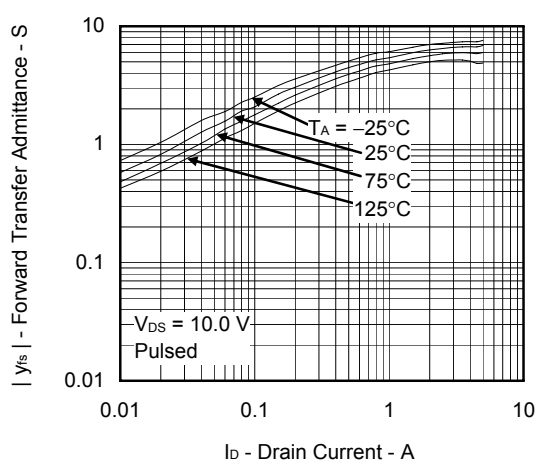
FORWARD TRANSFER CHARACTERISTICS



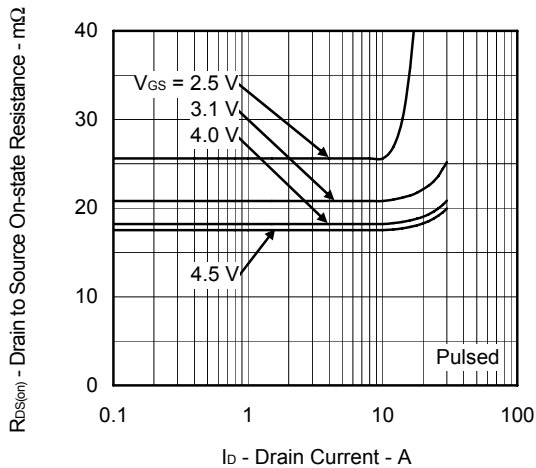
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



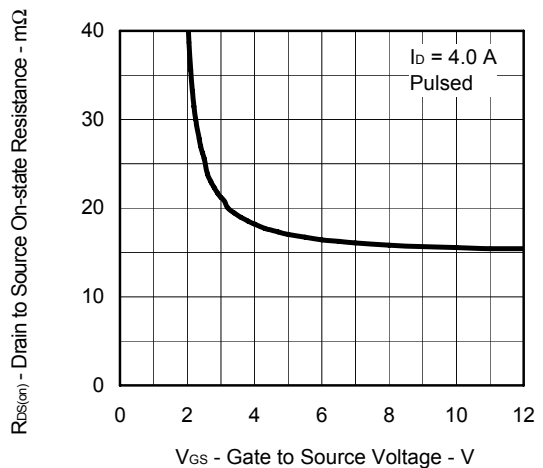
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



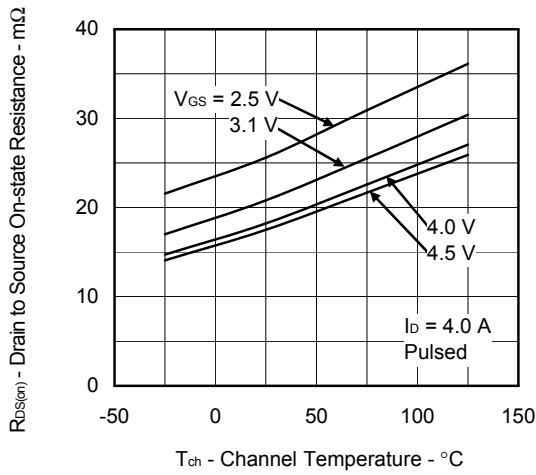
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



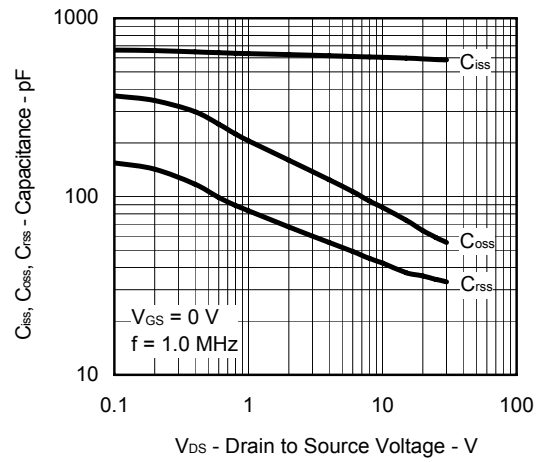
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



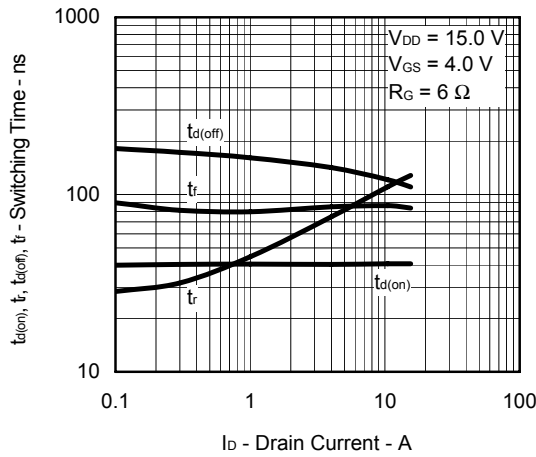
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



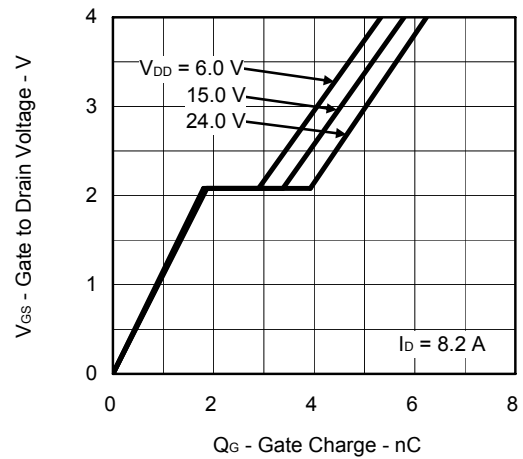
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



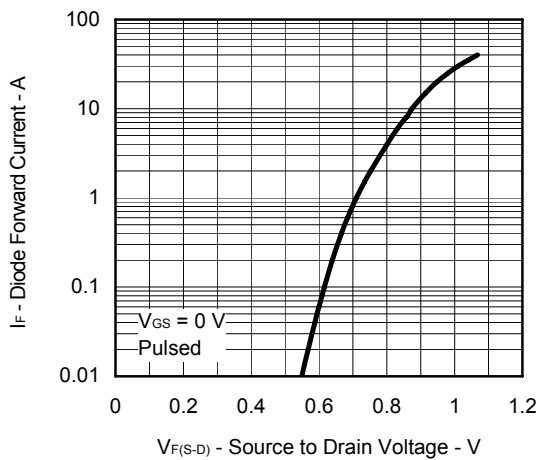
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

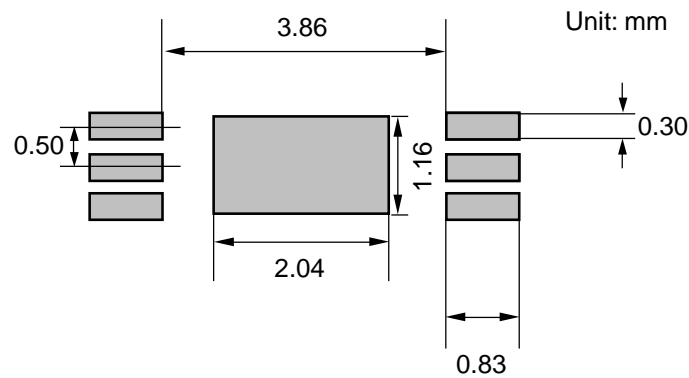


<Notes for using this device safely>

When you use this device, in order to prevent a customer’s hazard and damage, use it with understanding the following contents. If used exceeding recommended conditions, there is a possibility of causing failure of the device and characteristic degradation.

1. When you mount the device on a substrate, carry out within our recommended soldering conditions of infrared reflow. If mounted exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.
2. When you wash the device mounted the substrate, carry out within our recommended conditions. If washed exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.
3. When you use ultrasonic wave to substrate after the device mounting, prevent from touching a resonance generator directly. If it touches, the characteristic of a device may be degraded and it may result in failure.
4. Please refer to **Figure 1** as an example of the land pattern. Optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.

Figure 1. Example of the land pattern



5. This device is very thin device and should be handled with caution for mechanical stress. The rate of distortion applied to the device should become below 2000 με. ^{Note1} If the rate of distortion exceeds 2000 με, the characteristic of a device may be degraded and it may result in failure.

Figure 2. Direction of substrate and stress

The substrate that mounted the device is on a stand with a support width of 24 mm.
The device is turned downward. The stress is applied from a top.

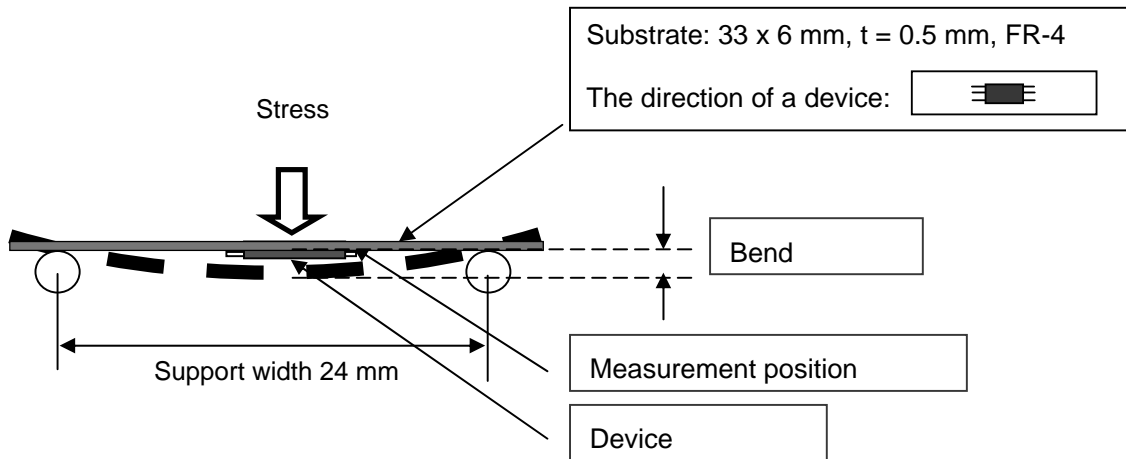
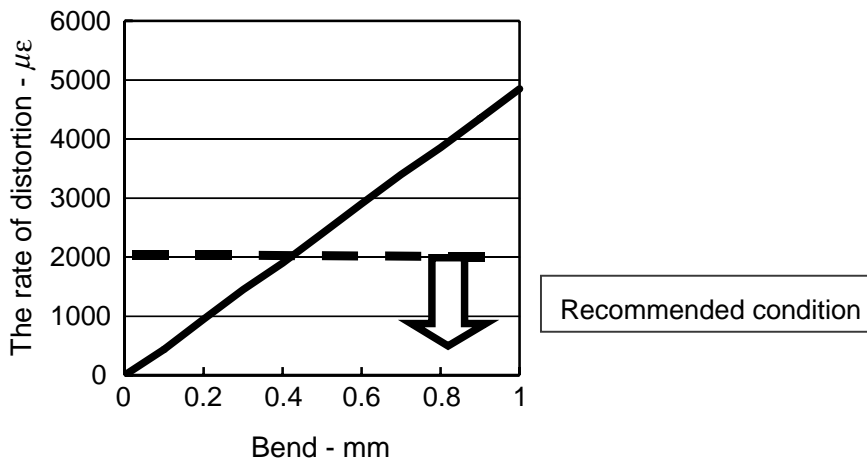


Figure 3. Example of the bend and the rate of distortion ^{Note2}



Note 1. Definition of rate of distortion(written as ε in this document)

$$\epsilon = (l - l_0) / l_0$$

l₀: Distance for two arbitrary points before receiving stress.

l: Distance above-mentioned when receiving stress.

2. The relation of the distortion and the bend changes with several conditions, such as a size of substrate and so on.

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