RENESAS

MOS FIELD EFFECT TRANSISTOR

μPA2731UT1A

SWITCHING
P-CHANNEL POWER MOSFET

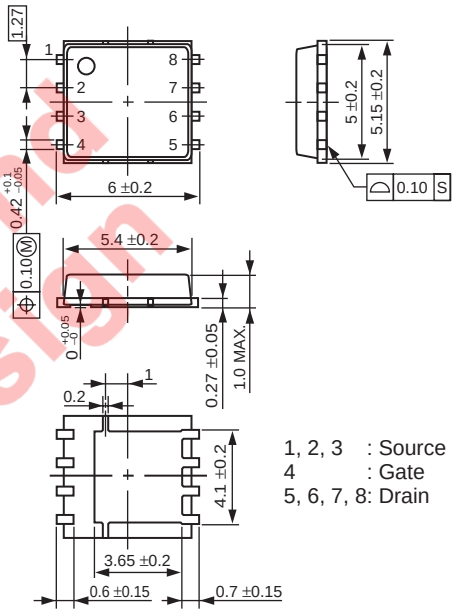
DESCRIPTION

The μPA2731UT1A is P-channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 3.3 mΩ MAX. (V_{GS} = –10 V, I_D = –22 A)
  $R_{DS(on)2}$ = 6.4 mΩ MAX. (V_{GS} = –4.5 V, I_D = –22 A)
- Low C_{iss}: C_{iss} = 3620 pF TYP.
- Small and surface mount package (8pin HVSON)

PACKAGE DRAWING (Unit: mm)



ORDERING INFORMATION

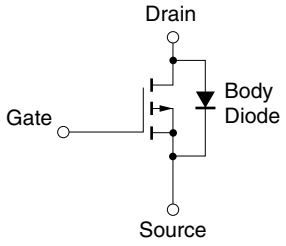
PART NUMBER	PACKAGE
μPA2731UT1A-E1-AZ Note	8pin HVSON
μPA2731UT1A-E2-AZ Note	8pin HVSON

Note Pb-free (This product does not contain Pb in external electrode.)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)}$	∓44	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓180	A
Total Power Dissipation Note2	P_{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) Note2	P_{T2}	4.6	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note3	I_{AS}	–22	A
Single Avalanche Energy Note3	E_{AS}	48	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on a glass epoxy board (25.4 mm x 25.4 mm x 0.8 mm)

3. Starting T_{ch} = 25°C, V_{DD} = –15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = –20 → 0 V

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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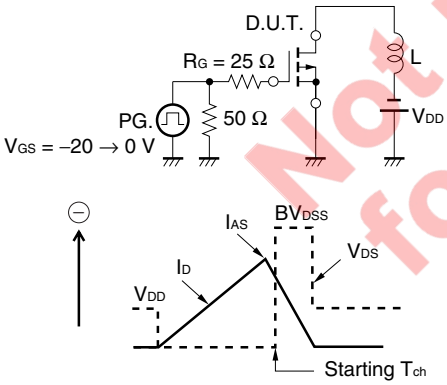
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

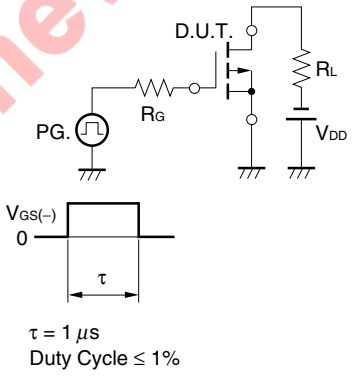
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0		–2.5	V
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –22 A		2.6	3.3	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –22 A		4.2	6.4	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		3620		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		1540		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		630		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –22 A		15		ns
Rise Time	t_r	V_{GS} = –10 V		16		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		760		ns
Fall Time	t_f			510		ns
Total Gate Charge	Q_G	V_{DD} = –24 V		149		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		17		nC
Gate to Drain Charge	Q_{GD}	I_D = –44 A		48		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 44 A, V_{GS} = 0 V		0.85		V
Reverse Recovery Time	t_{rr}	I_F = 44 A, V_{GS} = 0 V		87		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		60		nC

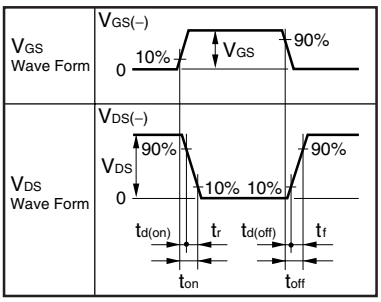
Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

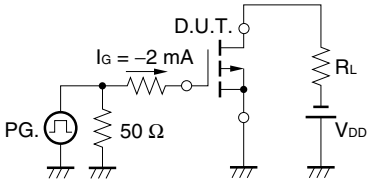


TEST CIRCUIT 2 SWITCHING TIME



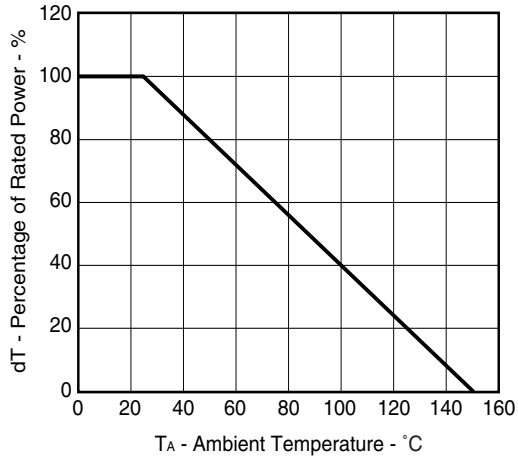


TEST CIRCUIT 3 GATE CHARGE

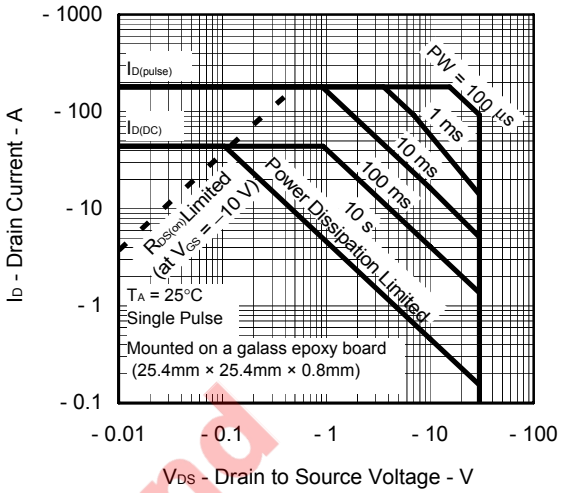


TYPICAL CHARACTERISTICS (T_A = 25°C)

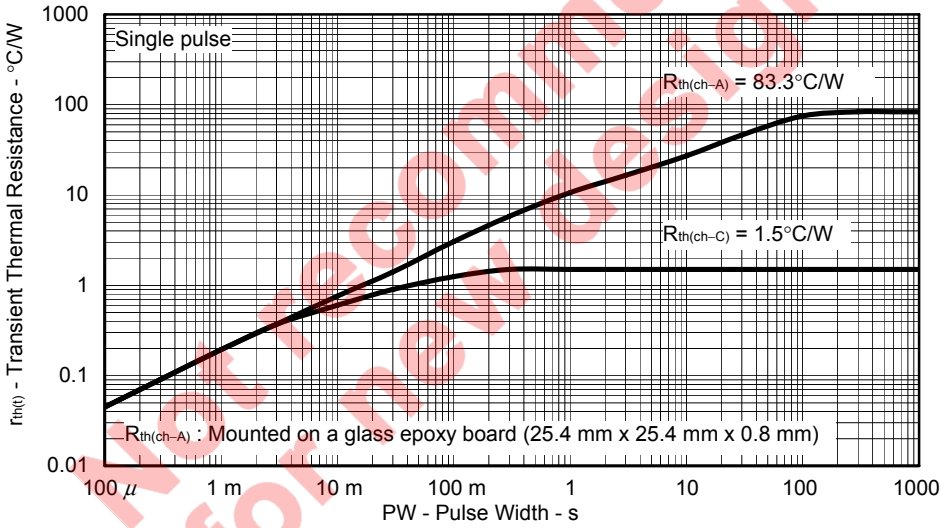
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



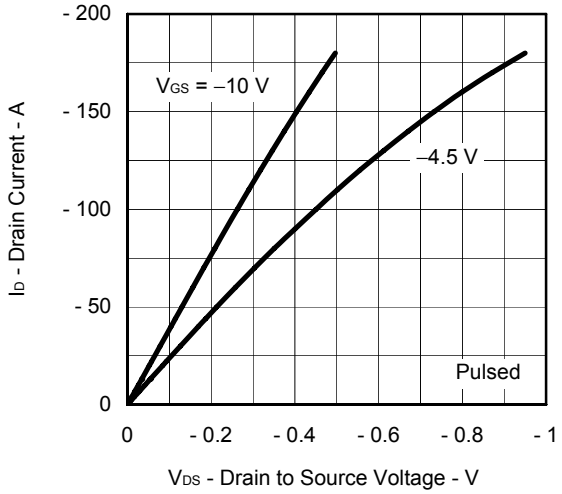
FORWARD BIAS SAFE OPERATING AREA



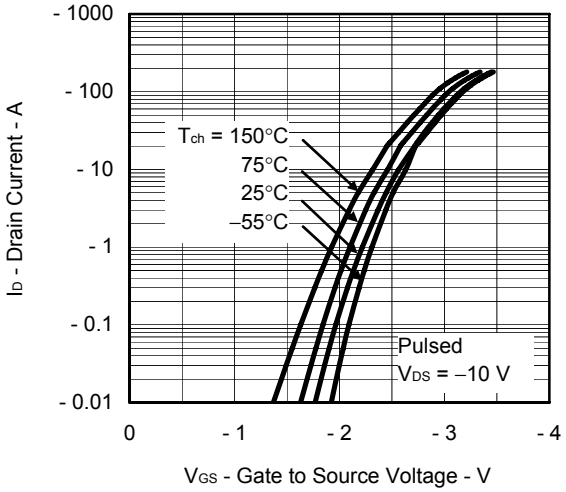
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



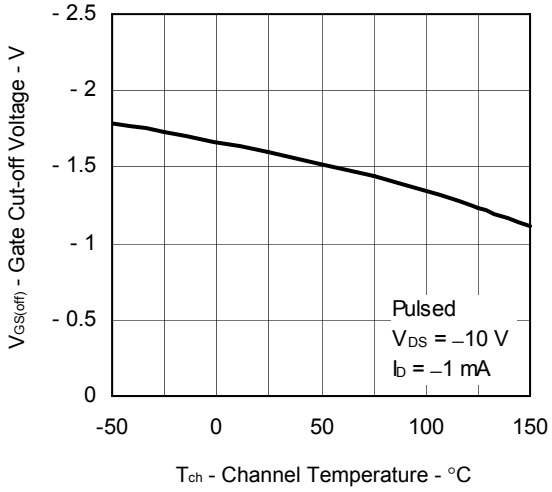
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



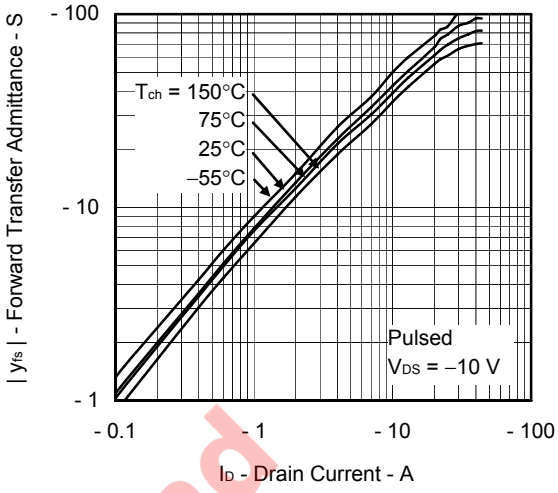
FORWARD TRANSFER CHARACTERISTICS



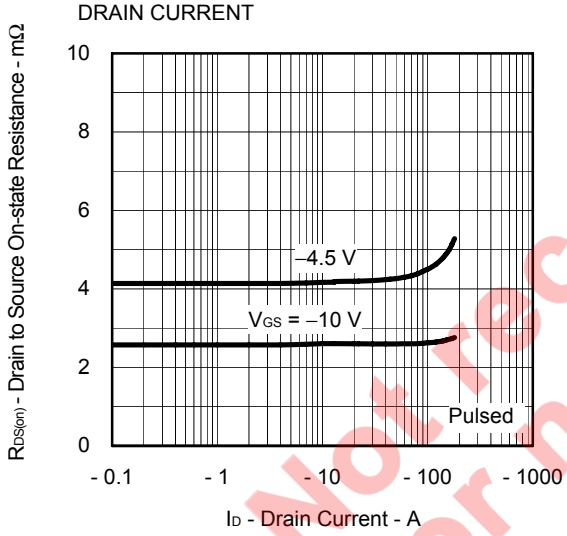
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



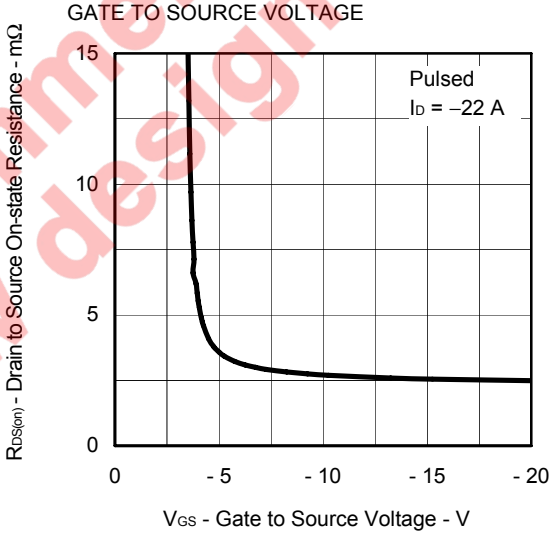
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



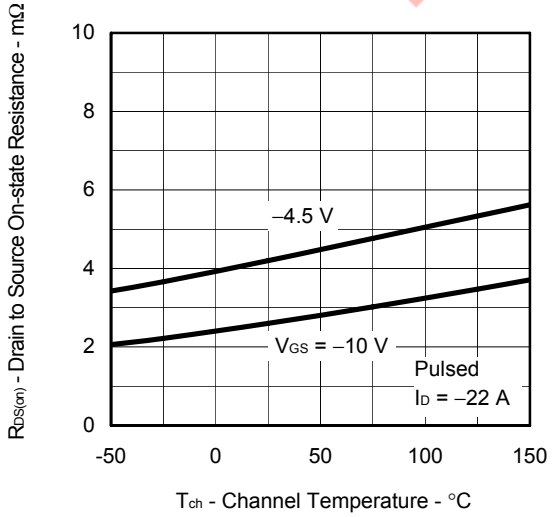
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



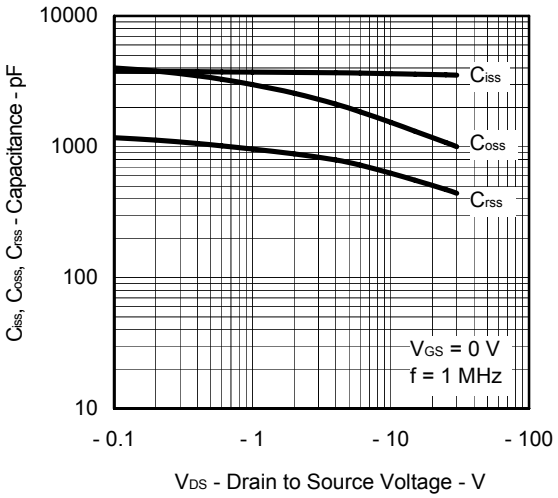
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



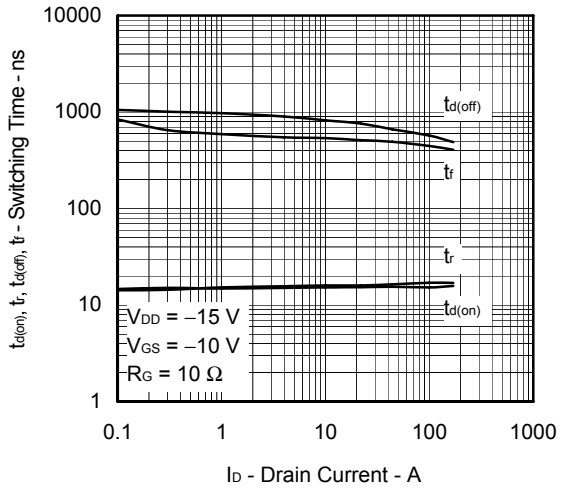
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



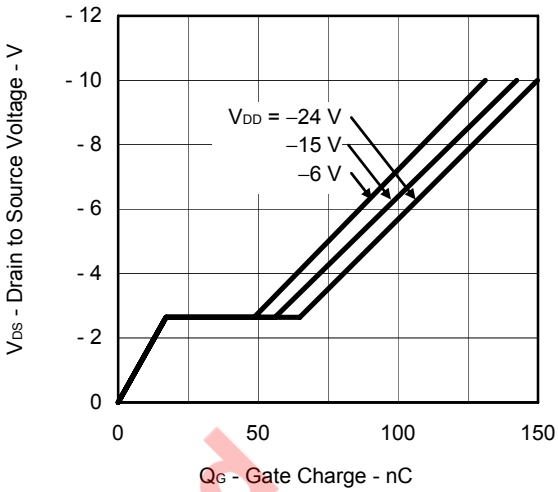
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



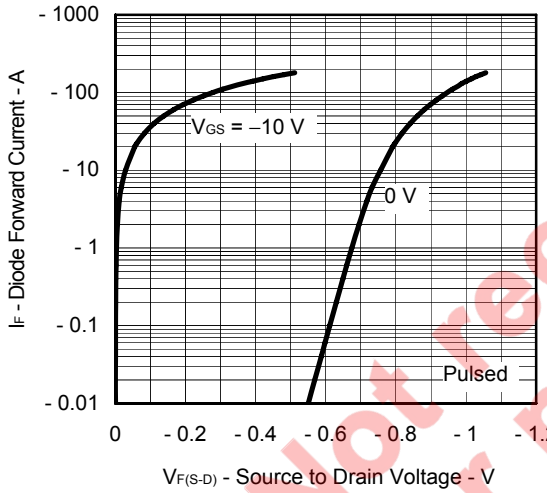
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT