DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

μPA2733GR

SWITCHING
P-CHANNEL POWER MOSFET

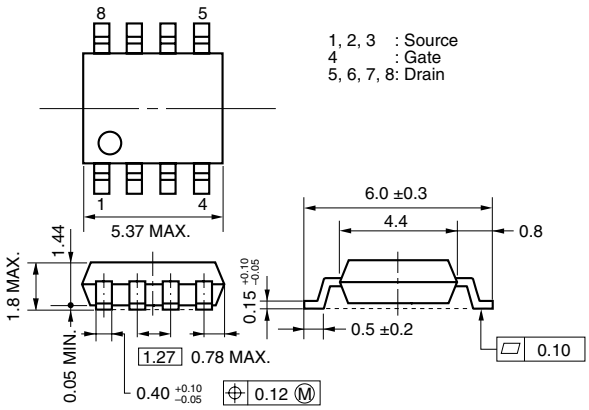
DESCRIPTION

The μPA2733GR is P-channel MOS Field Effect Transistor designed for power management applications of notebook computers and so on.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 38 mΩ MAX. (V_{GS} = –10 V, I_D = –2.5 A)
  $R_{DS(on)2}$ = 53 mΩ MAX. (V_{GS} = –4.5 V, I_D = –2.5 A)
- Low C_{iss}: C_{iss} = 870 pF TYP.
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)

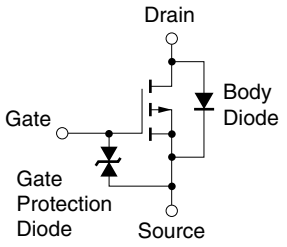


ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2733GR-E1	Power SOP8
μPA2733GR-E1-A Note	Power SOP8
μPA2733GR-E2	Power SOP8
μPA2733GR-E2-A Note	Power SOP8

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)}$	∓5	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓20	A
Total Power Dissipation Note2	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) Note2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Printed in Japan

The mark <R> shows major revised points.

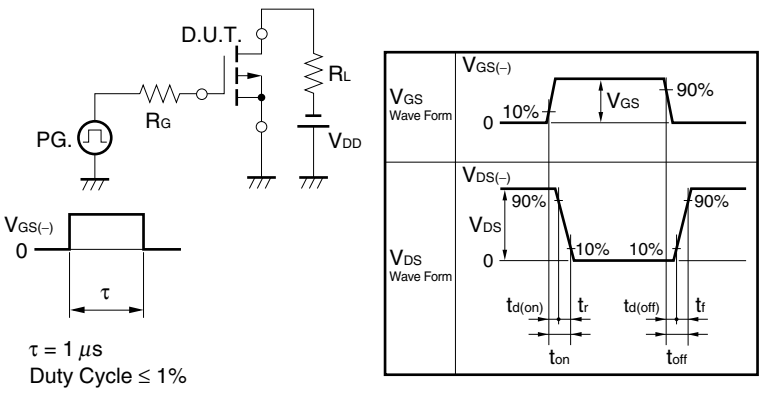
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0		–2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –2.5 A	2.5			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –2.5 A		30	38	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –2.5 A		39	53	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		870		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		200		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		150		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –2.5 A		7.7		ns
Rise Time	t_r	V_{GS} = –10 V		9.5		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		108		ns
Fall Time	t_f			64		ns
Total Gate Charge	Q_G	V_{DD} = –24 V		18		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		2.6		nC
Gate to Drain Charge	Q_{GD}	I_D = –5 A		5.8		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 5 A, V_{GS} = 0 V		0.8		V
Reverse Recovery Time	t_{rr}	I_F = 5 A, V_{GS} = 0 V		98		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		93		nC

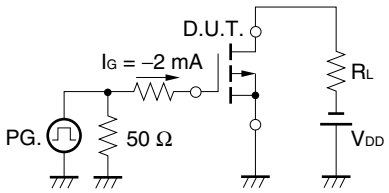
Note Pulsed

TEST CIRCUIT 1 SWITCHING TIME



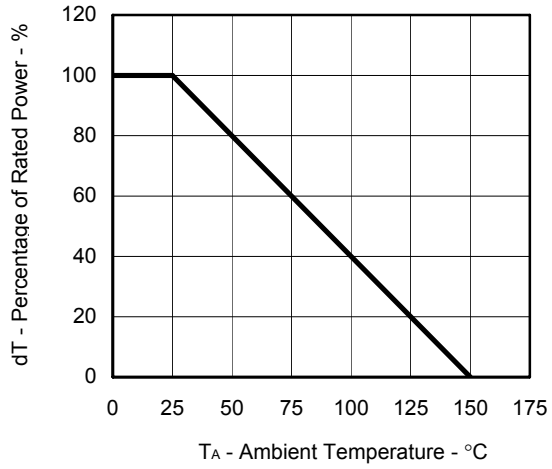
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE

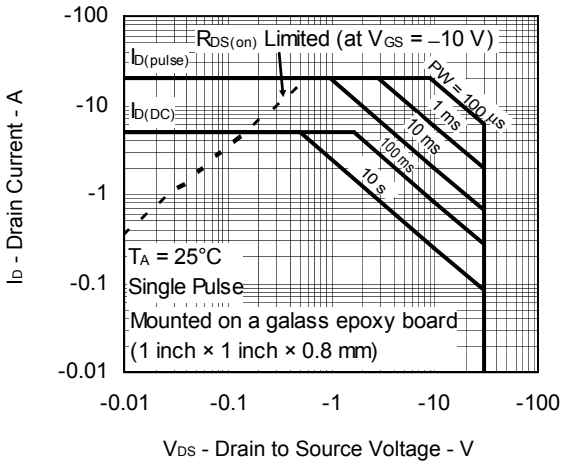


<R> TYPICAL CHARACTERISTICS (T_A = 25°C)

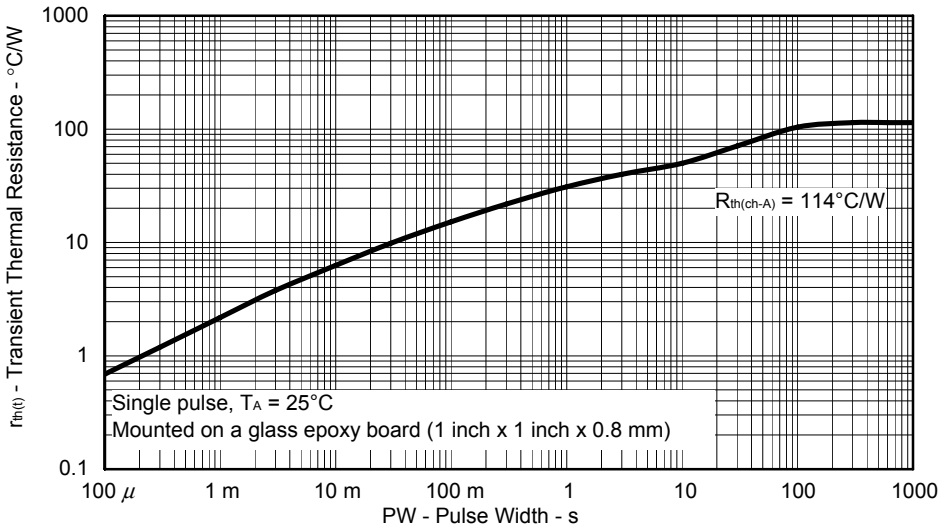
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



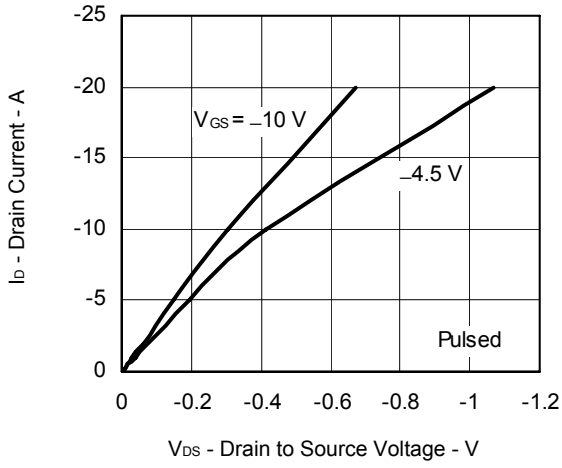
FORWARD BIAS SAFE OPERATING AREA



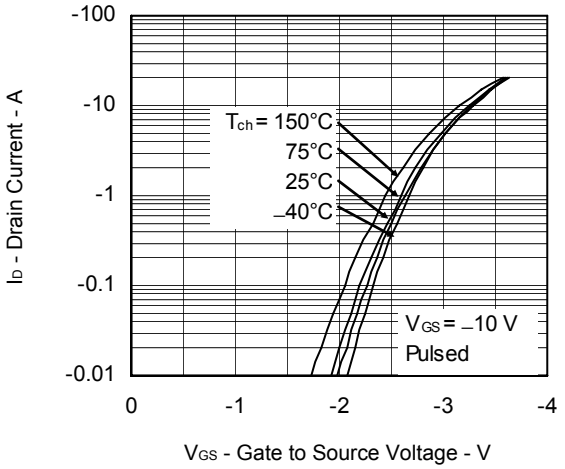
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



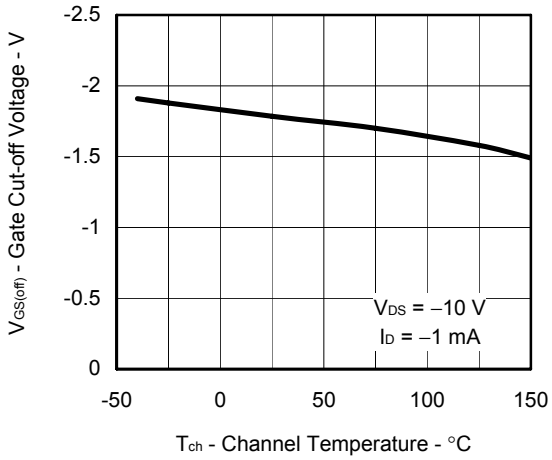
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



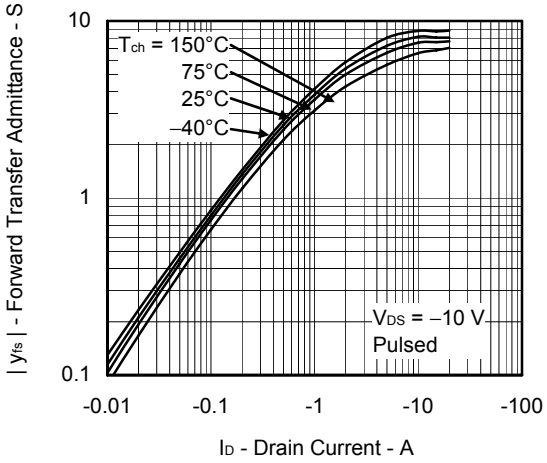
FORWARD TRANSFER CHARACTERISTICS



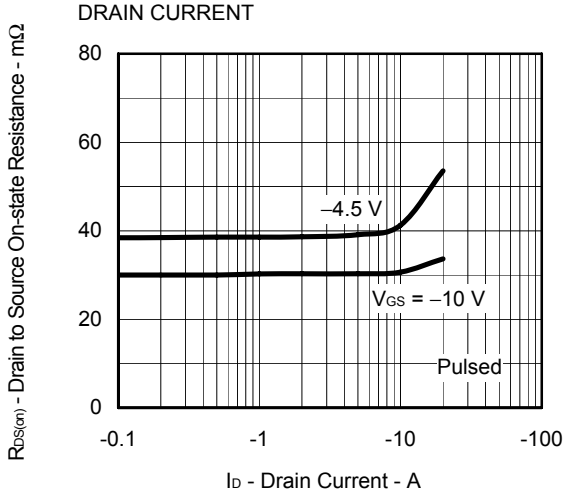
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



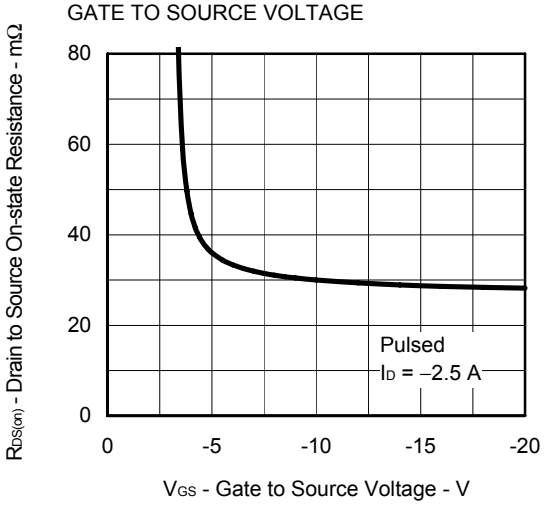
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



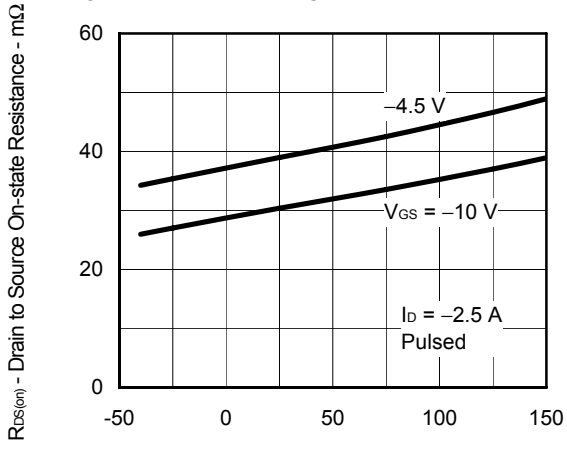
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



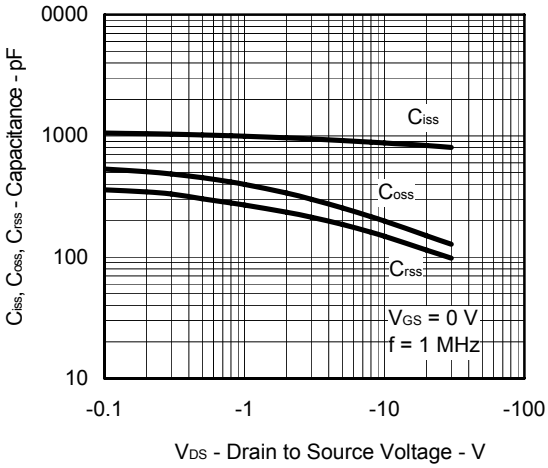
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



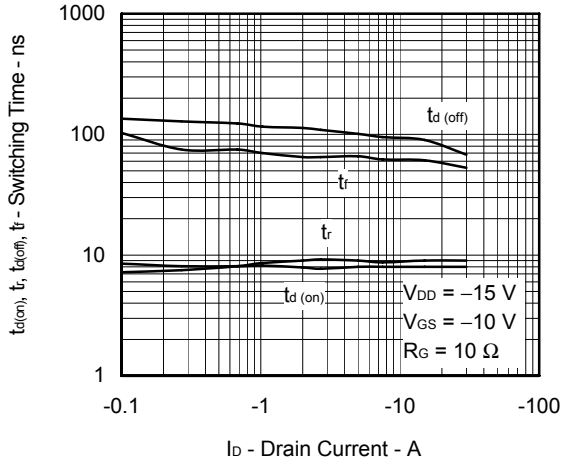
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



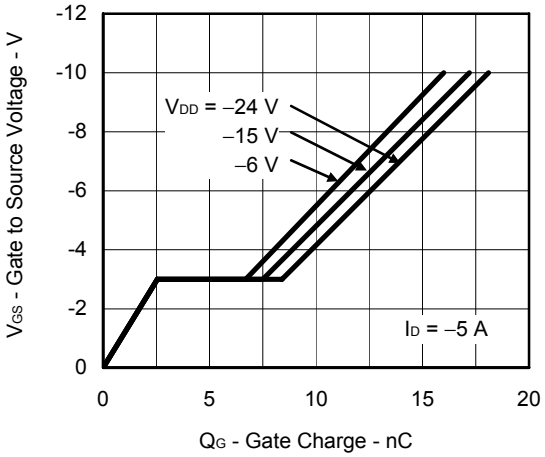
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



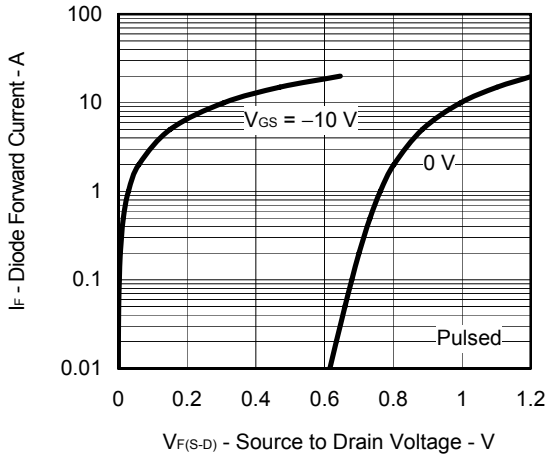
SWITCHING CHARACTERISTICS



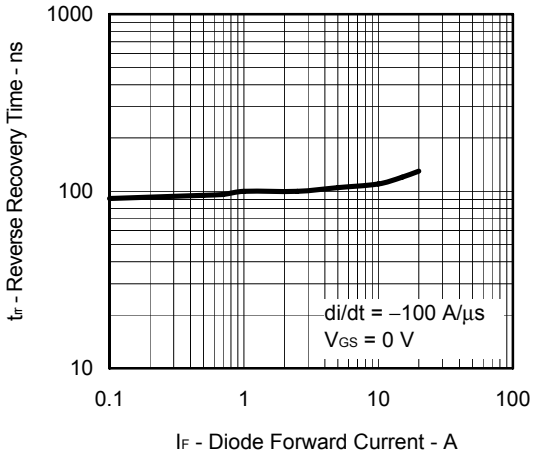
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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