

**SWITCHING  
N-CHANNEL POWER MOSFET**

**DESCRIPTION**

The μPA2743T1A is N-channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

**FEATURES**

- Low on-state resistance  
 $R_{DS(on)1} = 3.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 15 \text{ A)}$   
 $R_{DS(on)2} = 4.6 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 15 \text{ A)}$
- Built-in gate protection diode
- Thin type surface mount package with heat spreader (8-pin HVSON (6051))
- RoHS Compliant

**ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)**

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	±20	V
Drain Current (DC)	$I_{D(DC)}$	±29	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	±170	A
Total Power Dissipation <sup>Note2</sup>	$P_{T1}$	1.5	W
Total Power Dissipation (PW = 10 sec) <sup>Note2</sup>	$P_{T2}$	4.6	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	29	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	84.1	mJ

**THERMAL RESISTANCE**

Channel to Ambient Thermal Resistance <sup>Note2</sup>	$R_{th(ch-A)}$	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	1.5	°C/W

**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

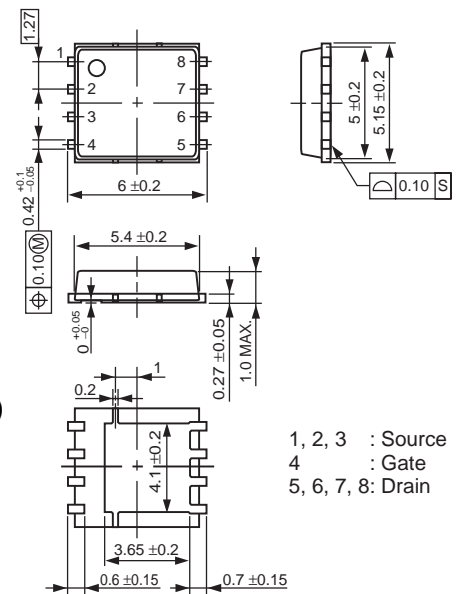
**2.** Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

**3.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$ ,  $L = 100 \mu\text{H}$

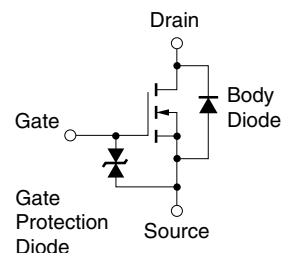
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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**PACKAGE DRAWING (Unit: mm)**



**EQUIVALENT CIRCUIT**

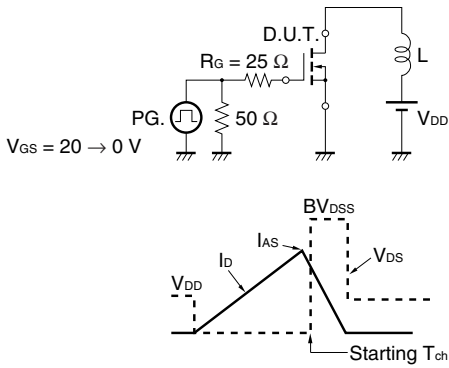


**ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)**

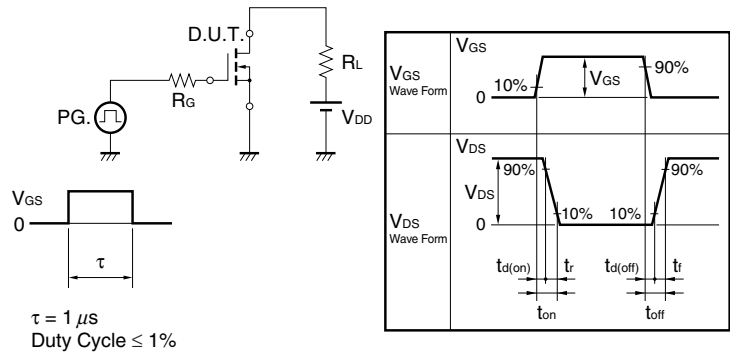
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0		2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A	13			S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		2.1	3.3	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		3.7	4.6	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V,		5080		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V,		650		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		380		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 15 A,		28		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V,		29		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		109		ns
Fall Time	t <sub>f</sub>			32		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V,		39		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5 V,		16		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 29 A		17		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 29 A, V <sub>GS</sub> = 0 V		0.79	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 29 A, V <sub>GS</sub> = 0 V,		38		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		39		nC

**Note** Pulsed

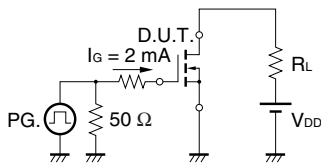
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

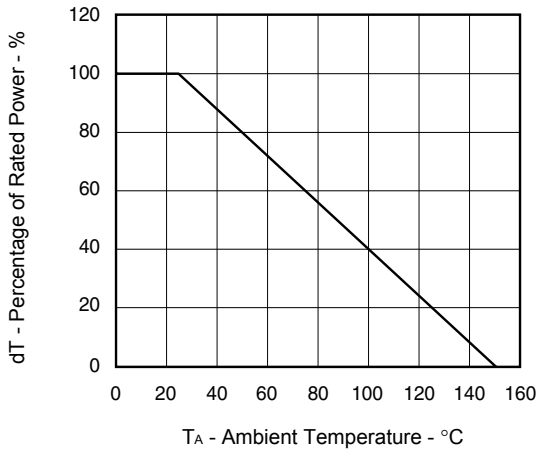


**TEST CIRCUIT 3 GATE CHARGE**

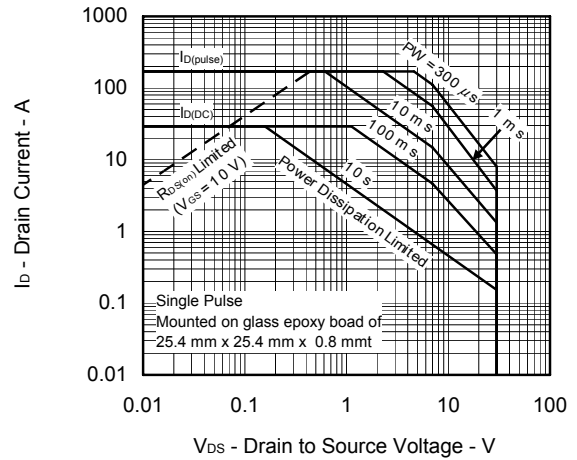


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

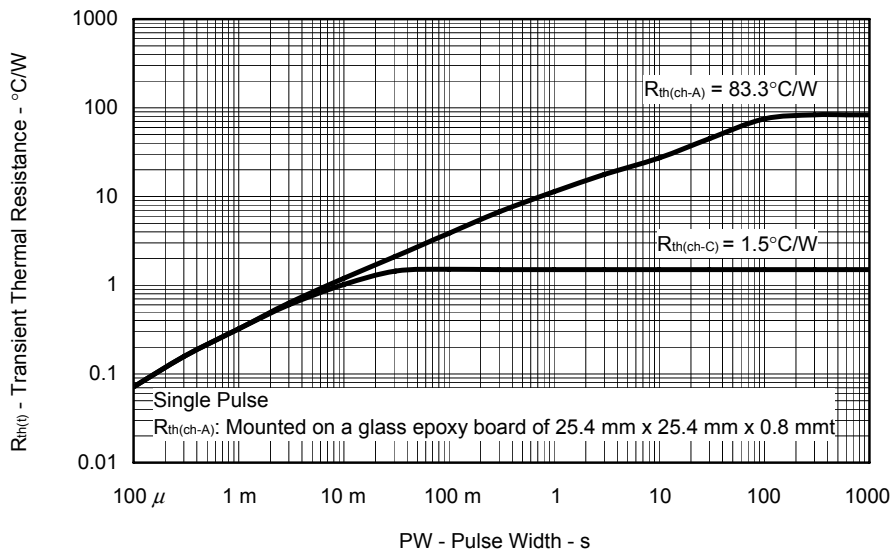
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



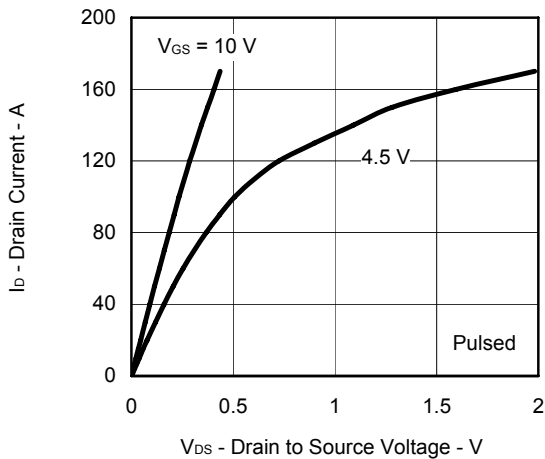
FORWARD BIAS SAFE OPERATING AREA



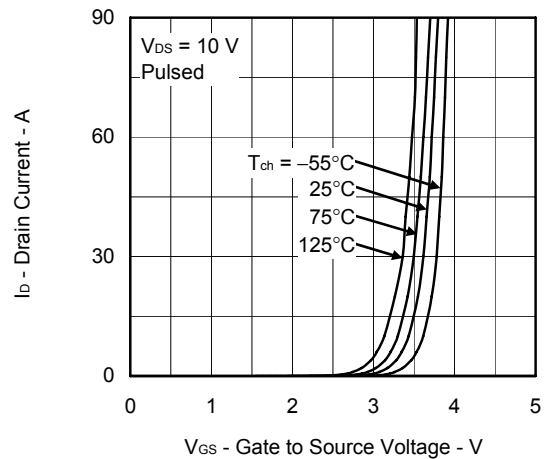
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



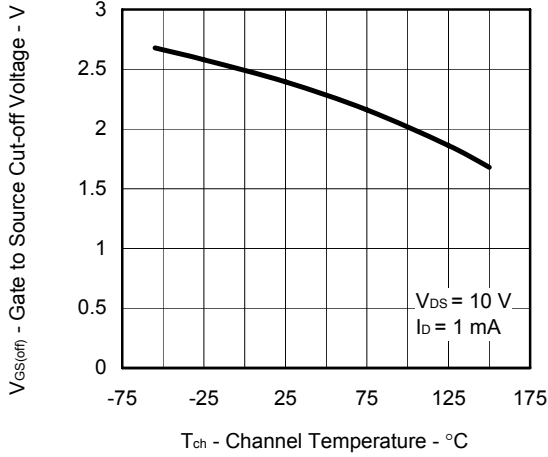
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



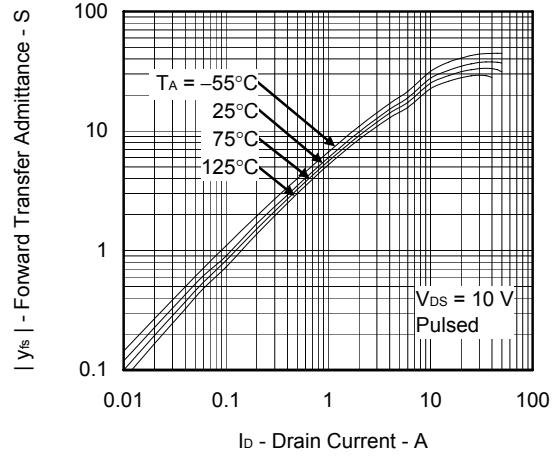
FORWARD TRANSFER CHARACTERISTICS



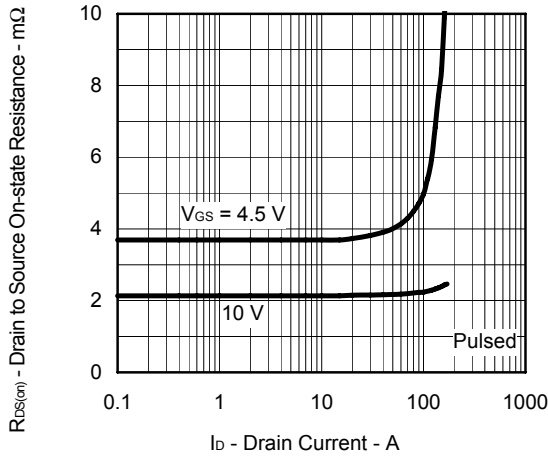
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



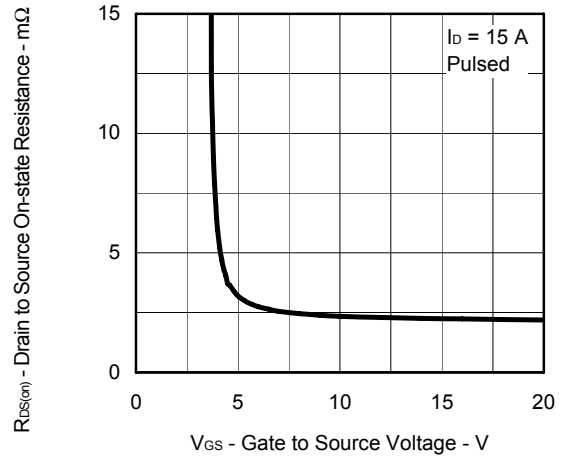
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



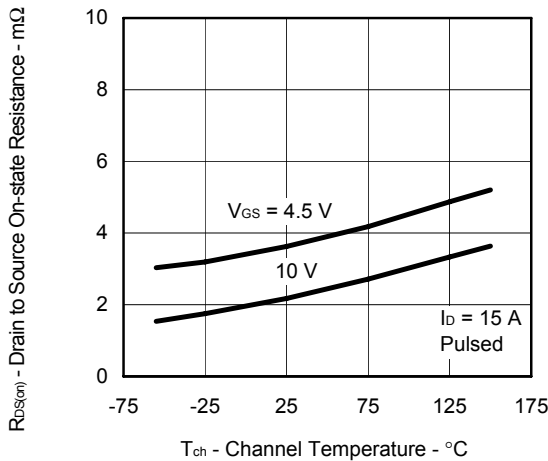
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



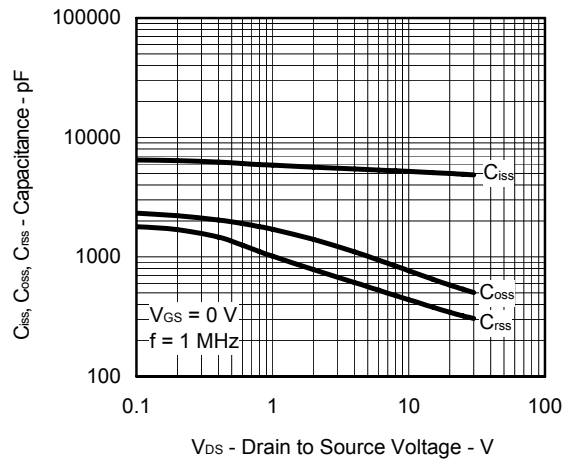
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



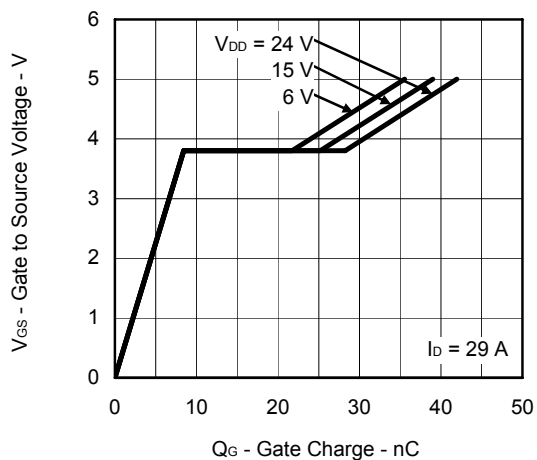
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



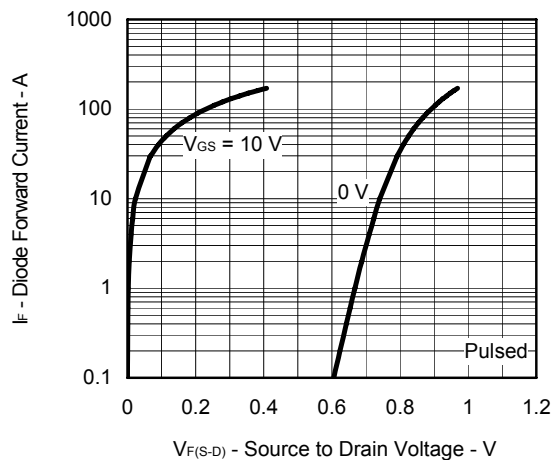
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



**ORDERING INFORMATION**

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
$\mu$ PA2743T1A-E1-AY <sup>Note</sup>	Pure Sn	Tape 3000 p/reel	8-pin HVSON (6051) 0.10 g TYP.
$\mu$ PA2743T1A-E2-AY <sup>Note</sup>			

**Note** Pb-free (This product does not contain Pb in the external electrode.)

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