

μ PA2761UGR

MOS FIELD EFFECT TRANSISTOR

R07DS0010EJ0100

Rev.1.00

Jun 01, 2010

Description

The μ PA2761UGR is N-Channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

Features

- Low on-state resistance
 - $R_{DS(on)1} = 18.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 9 \text{ A)}$
 - $R_{DS(on)2} = 30 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 7 \text{ A)}$
- Low Ciss: $C_{iss} = 550 \text{ pF TYP. (} V_{DS} = 15 \text{ V, } V_{GS} = 0 \text{ V)}$
- Small and surface mount package (Power SOP8)
- RoHS Compliant

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μ PA2761UGR-E1-AT *1	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8 0.08 g TYP.
μ PA2761UGR-E2-AT *1			

Note: *1. Pb-free (This product does not contain Pb in external electrode and other parts.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, All terminals are connected)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	±25	V
Drain Current (DC)	$I_{D(DC)}$	±9	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±40	A
Total Power Dissipation *2	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current *3	I_{AS}	9	A
Single Avalanche Energy *3	E_{AS}	8.1	mJ

Notes: *1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

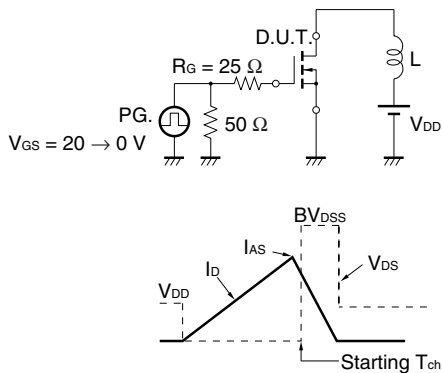
*3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, $L = 100 \mu\text{H}$

Electrical Characteristics (T_A = 25°C, All terminals are connected)

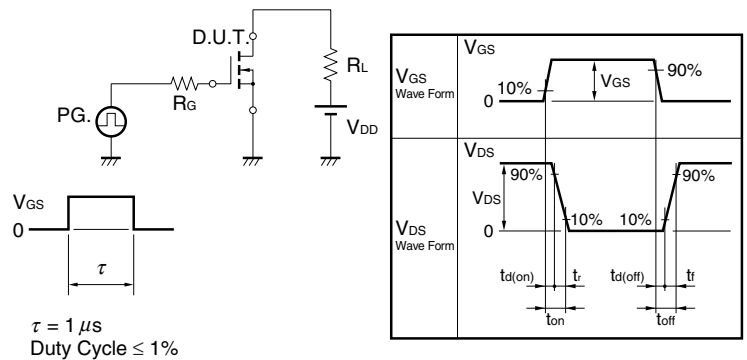
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			10	μA	V _{DS} = 30 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±100	μA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate Cut-off Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance *1	y _{fs}	2.5			S	V _{DS} = 10 V, I _D = 4.5 A
Drain to Source On-state Resistance *1	R _{DS(on)1}		14.3	18.5	mΩ	V _{GS} = 10 V, I _D = 9 A
	R _{DS(on)2}		20.1	30	mΩ	V _{GS} = 4.5 V, I _D = 7 A
Input Capacitance	C _{iSS}		550		pF	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz
Output Capacitance	C _{oSS}		93		pF	
Reverse Transfer Capacitance	C _{rSS}		56		pF	
Turn-on Delay Time	t _{d(on)}		8		ns	V _{DD} = 15 V, I _D = 4.5 A, V _{GS} = 10 V, R _G = 10 Ω
Rise Time	t _r		3.3		ns	
Turn-off Delay Time	t _{d(off)}		24.5		ns	
Fall Time	t _f		4		ns	
Total Gate Charge	Q _G		5.5		nC	V _{DD} = 15 V, V _{GS} = 5 V, I _D = 9 A
Gate to Source Charge	Q _{GS}		2.1		nC	
Gate to Drain Charge	Q _{GD}		2.7		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}			1.2	V	I _F = 9 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		21		ns	I _F = 9 A, V _{GS} = 0 V, di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		13.5		nC	

Note: *1. Pulsed

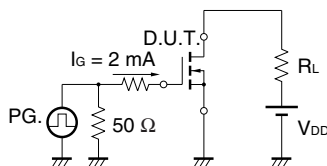
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

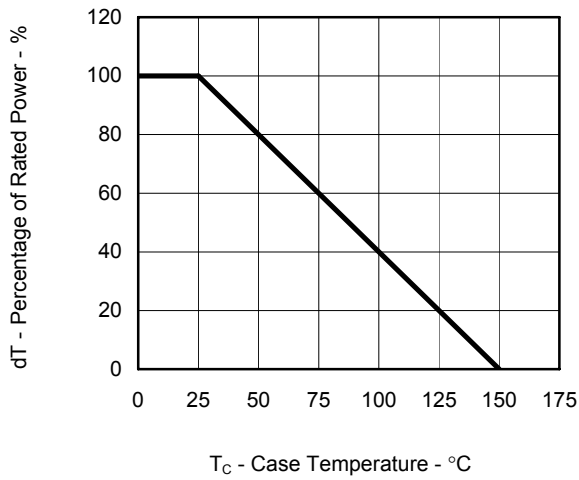


TEST CIRCUIT 3 GATE CHARGE

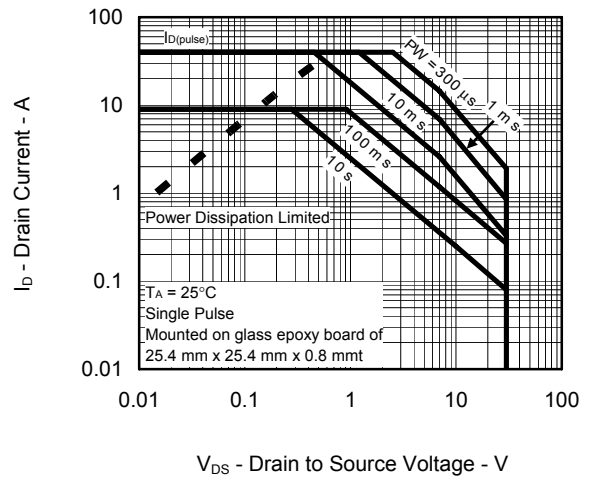


Typical Characteristics (T_A = 25°C)

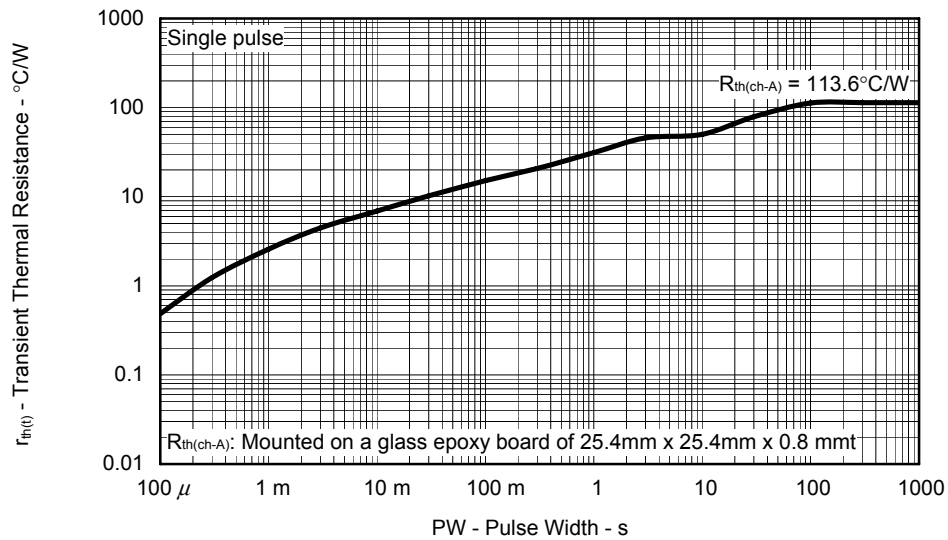
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



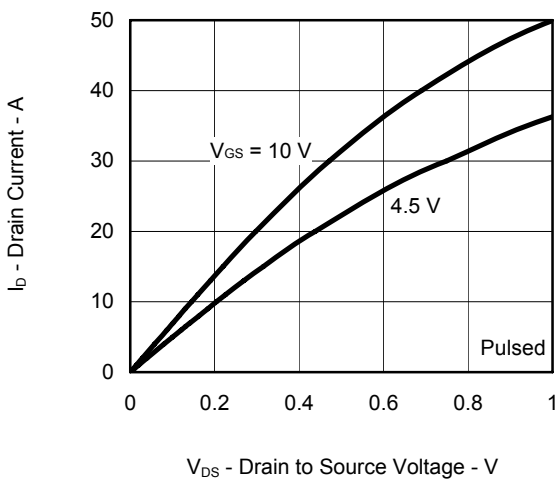
FORWARD BIAS SAFE OPERATING AREA



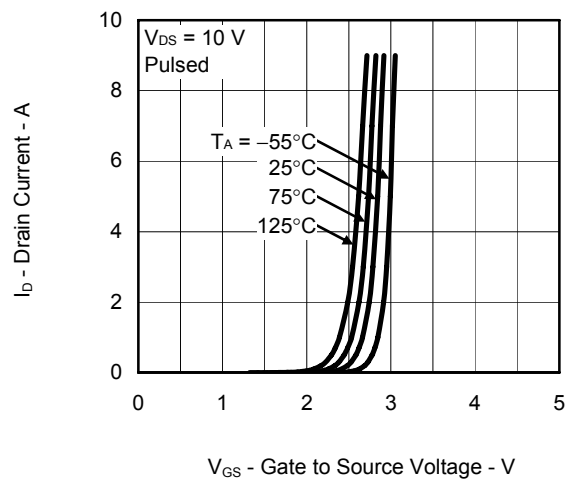
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



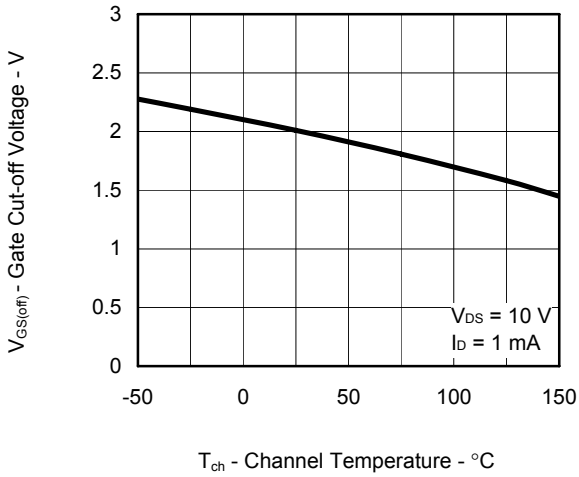
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



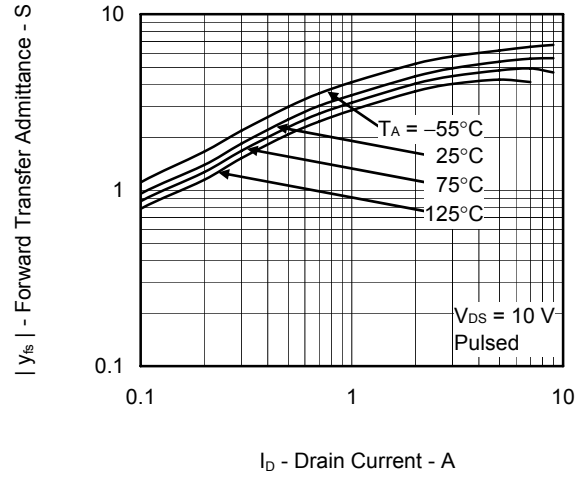
FORWARD TRANSFER CHARACTERISTICS



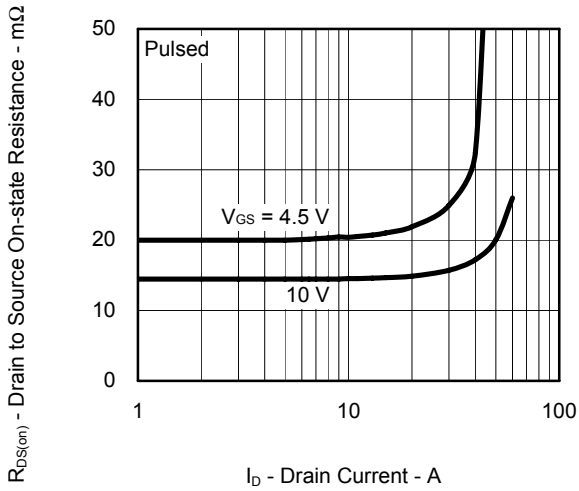
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



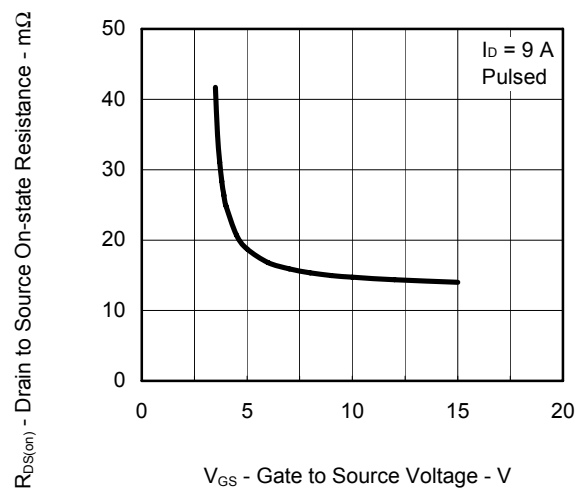
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



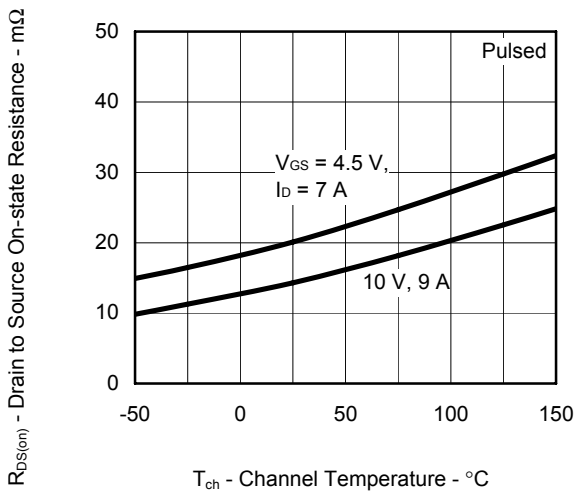
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



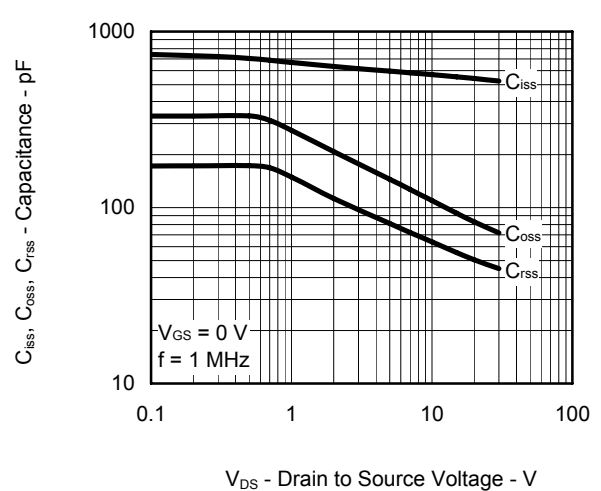
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



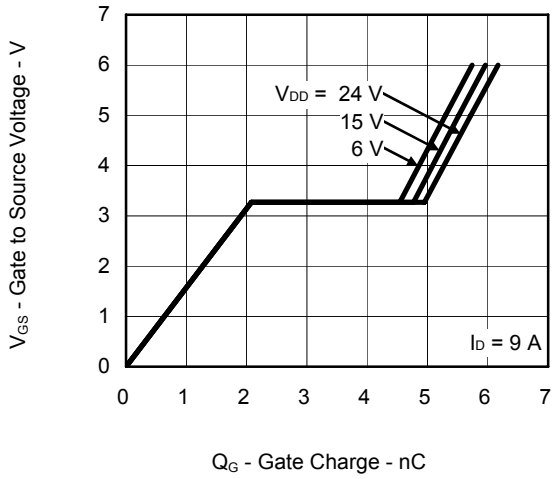
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



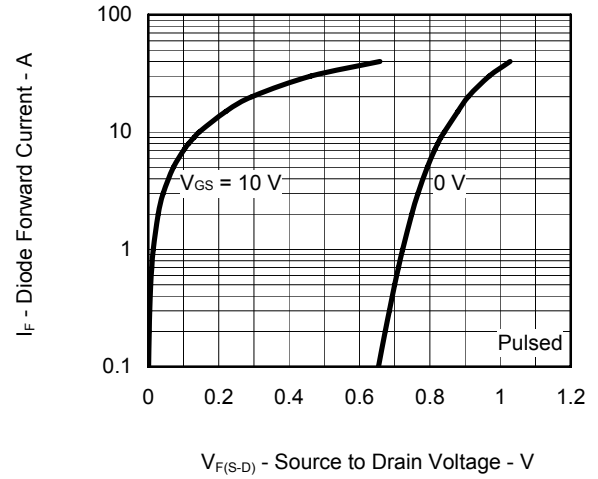
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS

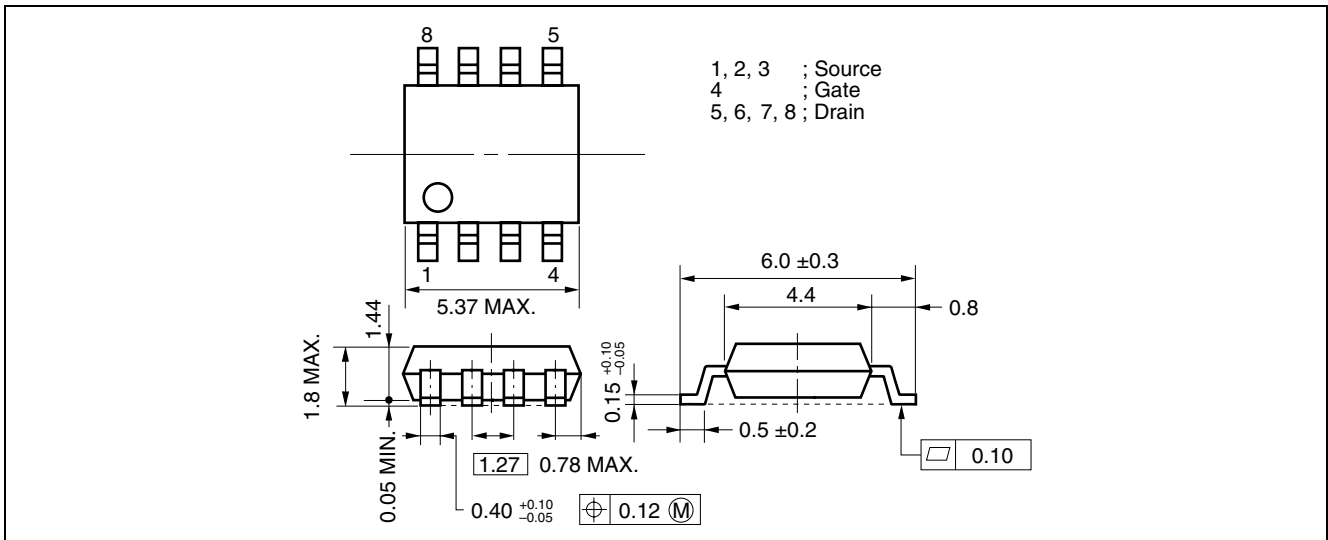


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

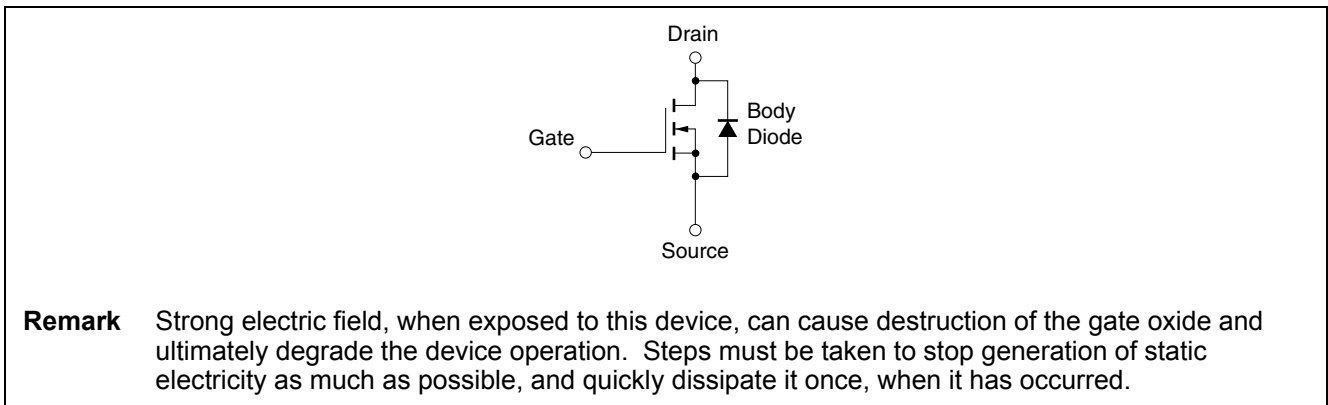


Package Drawings (Unit: mm)

Power SOP8



Equivalent Circuit



Revision History	μPA2761UGR
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Rev.	Date	Description	
		Page	Summary
1.00	June 01, 2010	-	First Eddition Issued

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Renesas Electronics America Inc.

2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141