

μ PA2762UGR

MOS FIELD EFFECT TRANSISTOR

R07DS0011EJ0100 Rev.1.00 Jun 01, 2010

Description

The μ PA2762UGR is N-Channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

Features

- Low on-state resistance
 - $R_{DS(on)1} = 13.5 \text{ m}\Omega \text{ MAX}.$ ($V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$)
 - --- $R_{DS(on)2}$ = 22 mΩ MAX. (V_{GS} = 4.5 V, I_D = 10 A)
- Low Ciss: Ciss = 710 pF TYP. $(V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V})$
- Small and surface mount package (Power SOP8)
- RoHS Compliant

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μ PA2762UGR-E1-AT *1	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8
μ PA2762UGR-E2-AT *1			0.08 g TYP.

Note: *1. Pb-free (This product does not contain Pb in external electrode and other parts.)

Absolute Maximum Ratings ($T_A = 25$ °C, All terminals are connected)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)}	±12	Α
Drain Current (pulse) *1	I _{D(pulse)}	±50	Α
Total Power Dissipation *2	P _{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) *2	P _{T2}	2.5	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	−55 to +150	°C
Single Avalanche Current *3	I _{AS}	12	Α
Single Avalanche Energy *3	E _{AS}	14.4	mJ

Notes: *1. PW \leq 10 μ s, Duty Cycle \leq 1%

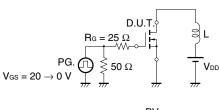
- *2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt
- *3. Starting T_{ch} = 25°C, V_{DD} = 17.5 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

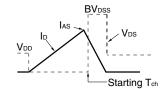
Electrical Characteristics (T_A = 25°C, All terminals are connected)

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	μΑ	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate Cut-off Voltage	$V_{GS(off)}$	1.0		2.5	V	$V_{DS} = 10 \text{ V}, I_{D} = 1 \text{ mA}$
Forward Transfer Admittance *1	y _{fs}	3.5			S	$V_{DS} = 10 \text{ V}, I_{D} = 6 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		11.0	13.5	mΩ	V _{GS} = 10 V, I _D = 12 A
Resistance *1	R _{DS(on)2}		15.8	22	mΩ	$V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$
Input Capacitance	C _{iss}		710		pF	V _{DS} = 15 V,
Output Capacitance	Coss		120		pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		71		pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		8.3		ns	$V_{DD} = 15 \text{ V}, I_D = 6 \text{ A},$
Rise Time	t _r		3.9		ns	$V_{GS} = 10 V,$
Turn-off Delay Time	$t_{d(off)}$		28		ns	$R_G = 10 \Omega$
Fall Time	t _f		5.5		ns	
Total Gate Charge	Q_G		6.2		nC	V _{DD} = 15 V,
Gate to Source Charge	Q_{GS}		2.5		nC	$V_{GS} = 5 V$,
Gate to Drain Charge	Q_{GD}		3.0		nC	I _D = 12 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$			1.2	V	I _F = 12 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		22		ns	I _F = 12 A, V _{GS} = 0 V,
Reverse Recovery Charge	Q _{rr}		15		nC	di/dt = 100 A/μs

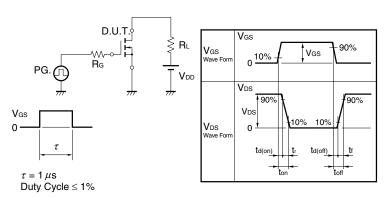
Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY





TEST CIRCUIT 2 SWITCHING TIME

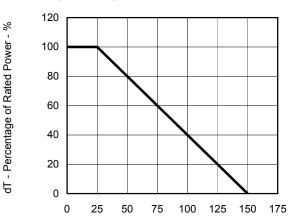


TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline V_{DE} \\ \hline \end{array}$$

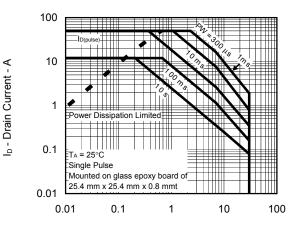
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



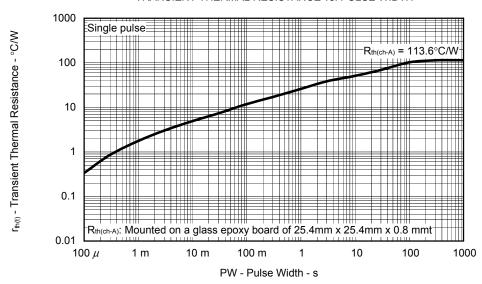
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA

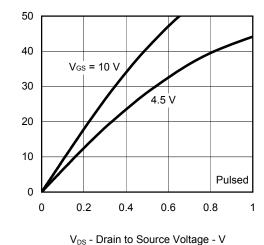


 V_{DS} - Drain to Source Voltage - V

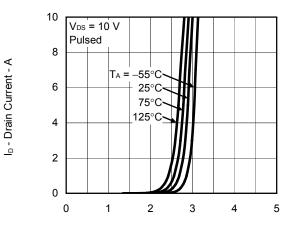
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH







FORWARD TRANSFER CHARACTERISTICS



V_{GS} - Gate to Source Voltage - V

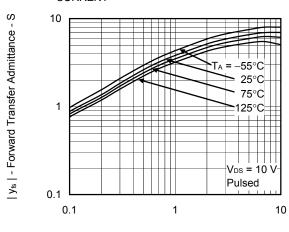
I_D - Drain Current - A

TEMPERATURE 3 V_{GS(off)} - Gate Cut-off Voltage - V 2.5 2 1.5 1 0.5 V_{DS} = 10 V $I_D = 1 \text{ mA}$ 0 0 -50 50 100 150

GATE CUT-OFF VOLTAGE vs. CHANNEL

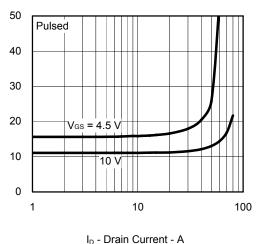
 T_{ch} - Channel Temperature - $^{\circ}C$

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I_D - Drain Current - A

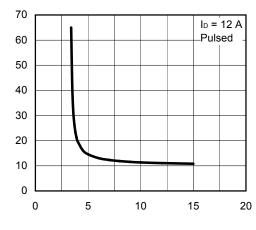
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - m Ω

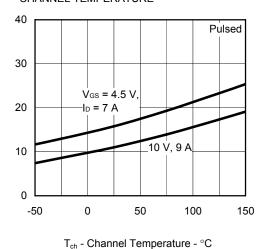
Ciss, Coss, Crss - Capacitance - pF

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

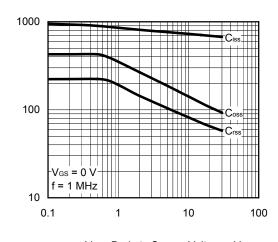


V_{GS} - Gate to Source Voltage - V

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



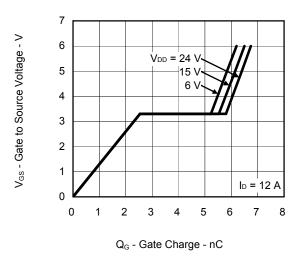
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



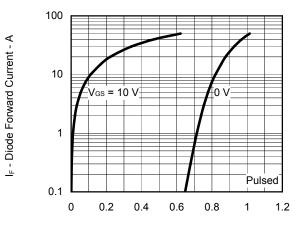
 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

 $R_{DS(on)}$ - Drain to Source On-state Resistance - $m\Omega$

DYNAMIC INPUT CHARACTERISTICS



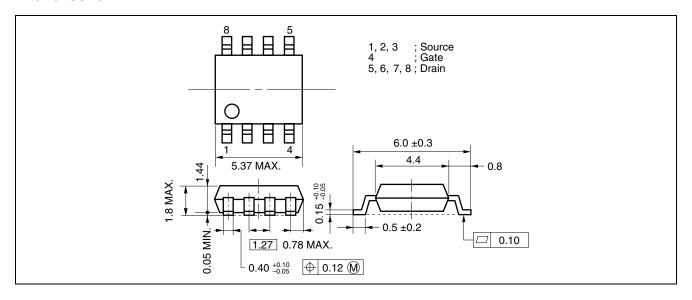
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



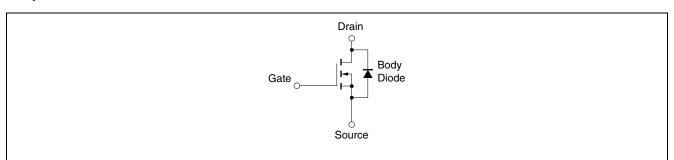
 $V_{F(S\text{-}D)}$ - Source to Drain Voltage - V

Package Drawings (Unit: mm)

Power SOP8



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	μ PA2762UGR
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		Description		
Rev.	Date	Page	Summary	
1.00	June 01, 2010	-	First Eddition Issued	

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