

FEATURES

- **SMALL PACKAGE STYLE:**
SOT-363 package measures just 2.0 mm x 1.25 mm
- **LOW HEIGHT PROFILE:**
Just 0.60 mm high
- **EXCELLENT LOW VOLTAGE, LOW CURRENT PERFORMANCE**

DESCRIPTION

The UPA800TF contains two NE680 NPN high frequency silicon bipolar chips. NEC's new low profile TF package is ideal for all portable wireless applications where reducing component height is a prime consideration. Each transistor chip is independently mounted and easily configured for two stage cascade LNAs and other similar applications.

ABSOLUTE MAXIMUM RATINGS¹ (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V _{CB0}	Collector to Base Voltage	V	20
V _{CEO}	Collector to Emitter Voltage	V	10
V _{EB0}	Emitter to Base Voltage	V	1.5
I _C	Collector Current	mA	35
P _T	Total Power Dissipation		
	1 Die	mW	110
	2 Die	mW	200
T _J	Junction Temperature	°C	150
T _{STG}	Storage Temperature	°C	-65 to +150

Note:

1. Operation in excess of any one of these parameters may result in permanent damage.

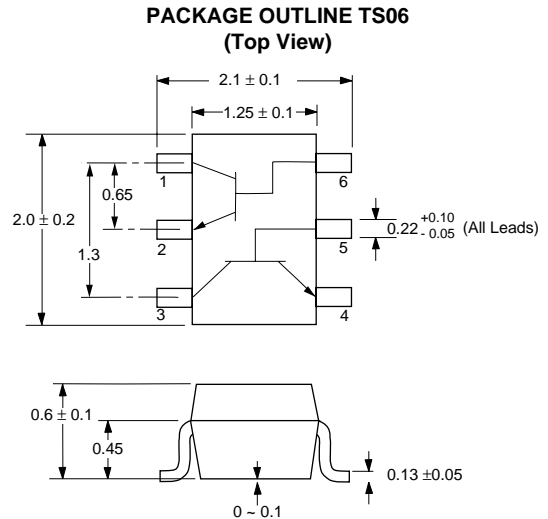
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE			UPA800TF TS06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I _{CBO}	Collector Cutoff Current at V _{CB} = 10 V, I _E = 0	μA			1.0
I _{EBO}	Emitter Cutoff Current at V _{EB} = 1 V, I _C = 0	μA			1.0
h _{FE}	Forward Current Gain ¹ at V _{CE} = 3 V, I _C = 5 mA		80	120	200
f _T	Gain Bandwidth at V _{CE} = 3 V, I _C = 5 mA	GHz	5.5	8.0	
C _{re}	Feedback Capacitance ² at V _{CB} = 3 V, I _E = 0, f = 1 MHz	pF		0.3	0.7
S _{21E} ²	Insertion Power Gain at V _{CE} = 3 V, I _C = 5 mA, f = 2 GHz	dB	5.5	7.5	
NF	Noise Figure at V _{CE} = 3 V, I _C = 5 mA, f = 2 GHz	dB		1.9	3.2

Notes: 1. Pulsed measurement, pulse width ≤ 350 μs, duty cycle ≤ 2 %.

2. The emitter terminal should be connected to the ground terminal of the 3 terminal capacitance bridge. For Tape and Reel version use part number UPA800TF-T1, 3K per reel.

OUTLINE DIMENSIONS (Units in mm)



PIN OUT

1. Collector Transistor 1
2. Emitter Transistor 1
3. Collector Transistor 2
4. Emitter Transistor 2
5. Base Transistor 2
6. Base Transistor 1

Note:

Pin 1 is the lower left most pin as the package lettering is oriented and read left to right.