NEC

3V DUAL DOWNCONVERTER AND PLL FREQUENCY SYNTHESIZER

UPB1004GS

FEATURES

- **INTEGRATED RF BLOCK:** RF & IF Downconverter + PLL frequency synthesizer
- **DOUBLE-CONVERSION:** f_{1stIF} = 61.380 MHz, f_{2ndIF} = 4.092 MHz
- **ADJUSTABLE GAIN:** 20 dB range MIN
- **FIXED DIVISION PRESCALER**
- **LOW POWER CONSUMPTION:** 37.5 mA @ 3 V
- **SMALL 30 PIN SSOP PACKAGE**
- **TAPE AND REEL PACKAGING AVAILABLE**

DESCRIPTION

The UPB1004GS is a Silicon Monolithic Integrated Circuit designed for low cost GPS receivers. The IC combines a double-conversion RF/IF downconverter block and a PLL frequency synthesizer on one chip. The device operates on a 3 V supply voltage and is housed in a small 30 pin SSOP package, resulting in low power consumption and reduced board space. The device is manufactured using the NESAT™ III 20 GHz f_T silicon bipolar process.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3 V, unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPB1004GS S30		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{CC}	Total Circuit Current, No Signals	mA	31.1	37.5	50.7
RF Downconverter Block (f_{RFin} = 1575.42 MHz, $f_{1stLOin}$ = 1636.80 MHz, P_{LOin} = -10 dBm, Z_L = Z_S = 50 Ω)					
I_{CC1}	Circuit Current 1, No Signals	mA	7.2	10	12.1
CG_{RF}	RF Conversion Gain, P_{RFin} = -40 dBm	dB	9.5	12.5	15.5
NF_{RF}	RF SSB Noise Figure, P_{RFin} = -40 dBm	dB		12.5	15.5
$P_{O(sat)RF}$	Maximum IF Output, P_{RFin} = -10 dBm	dBm	-8	-5	-2
LO_{IF}	LO Leakage to IF Pin, f_{LOin} = 1636.80 MHz	dBm		-30	
LO_{RF}	LO Leakage to RF Pin, f_{LOin} = 1636.80 MHz	dBm		-30	
IIP_{3RF}	Input 3rd Order Intercept Point, f_{RFin1} = 1600 MHz, f_{RFin2} = 1605 MHz, f_{LOin} = 1570 MHz	dBm		-6	
IF Downconverter Block ($f_{1stIFin}$ = 61.38 MHz, $f_{2ndLOin}$ = 65.472 MHz, Z_S = 50 Ω, Z_O = 2 kΩ)					
I_{CC2}	Circuit Current 2, No Signals	mA	2.7	3.8	4.7
CG_{IF}	IF Conversion Gain at Max. Gain, $P_{1stIFin}$ = -50 dBm	dB	37	40	43
NF_{IF}	IF SSB Noise Figure at Max. Gain, $P_{1stIFin}$ = -50 dBm	dB	12	15	18
$P_{O(sat)IF}$	Maximum 2nd IF Output Level at Max. Gain, $P_{1stIFin}$ = -20 dBm	dBm	-3	0	+3
V_{GC}	Gain Control Voltage, Voltage at Max. Gain of CG_{IF}	V			1.0
D_{GC}	Gain Control Range	dB	20		
LO_{2ndIF}	LO Leakage to 2nd IF, $f_{2ndLOin}$ = 65.472 MHz	dBm		-20	
LO_{1stIF}	LO Leakage to 1st IF, $f_{2ndLOin}$ = 65.472 MHz	dBm		-40	
2nd IF Amplifier (f_{2ndIF}= 4.092 MHz, Z_S = 50 Ω, Z_O = 2 kΩ)					
I_{CC3}	Circuit Current 3, No Signals	mA	1.2	1.7	2.3
$\|S_{21}\|$	Gain $\|S_{21}\|$, Z_O = 1 MΩ // 27 pF	dB	37	40	43
$V_{2ndIFout}$	Output Voltage, Z_O = 1MΩ // 27 pF	mV_{P-P}	600		
PLL Synthesizer Block					
I_{CC4}	Circuit Current 4, PLL, All Blocks Operating	mA	20	22	31.6
f_{PD}	Phase Comparison Frequency, PLL Loop	MHz	8.0	8.184	8.4
V_{REFin}	Reference Input Level, Z_O = 10 kΩ // 20pF	mV_{P-P}	200		
$V_{LP(H)}$	Loop Filter Output Level (H)	V	2.8		
$V_{LP(L)}$	Loop Filter Output Level (L)	V			0.4
V_{REFout}	Reference Output Voltage, Z_O = 1 MΩ // 27 pF	V_{P-P}	1.0		

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	3.6
I_{CC}	Circuit Current	mA	62
P_D	Power Dissipation[2]	mW	433
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150

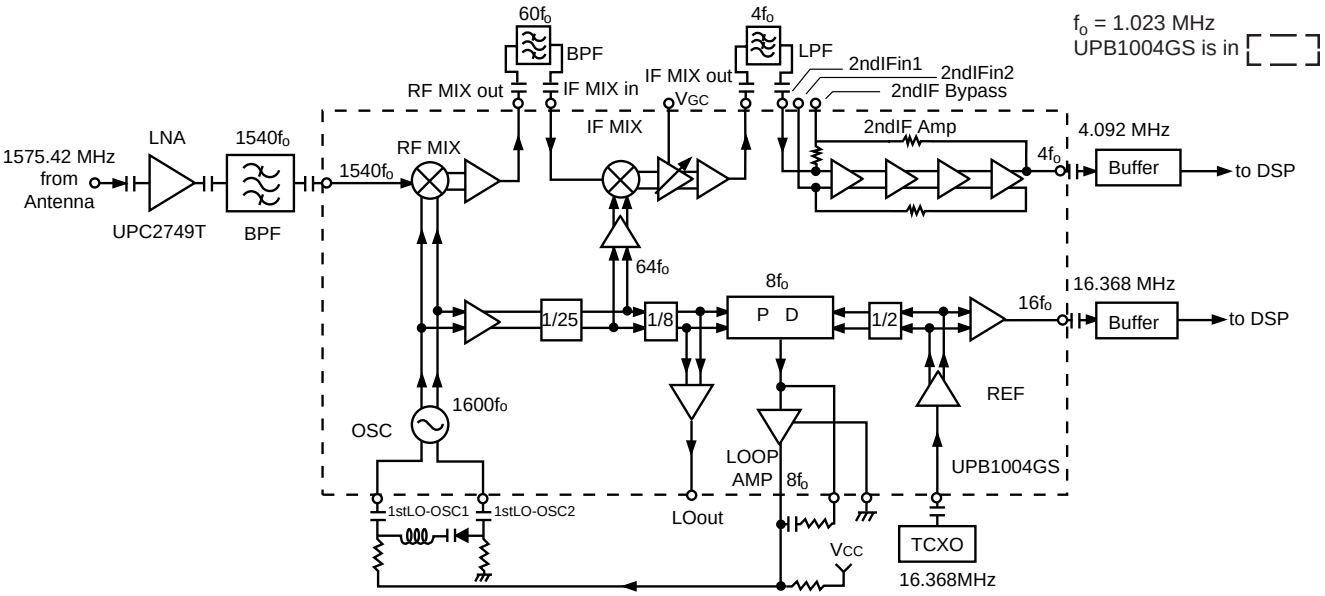
Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50 x 50 x 1.6 mm double-sided copper clad epoxy glass PWB (T_A = +85°C).

RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	3.3
T_{OP}	Operating Temperature	°C	-40	+25	+85
f_{RFin}	RF Input Frequency	MHz		1575.42	
$f_{1stLOin}$	1st LO Oscillating Frequency	MHz	1616.8	1636.8	1656.8
$f_{1stIFIN}$	1st IF Input Frequency	MHz		61.38	
$f_{2ndLOin}$	2nd LO Input Frequency	MHz		65.472	
$f_{2ndIFin}$ $f_{2ndIFout}$	2nd IF Input/Output Frequency	MHz		4.092	
f_{TCXOin} $f_{TCXOout}$	Reference Input/Output Frequency	MHz		16.368	

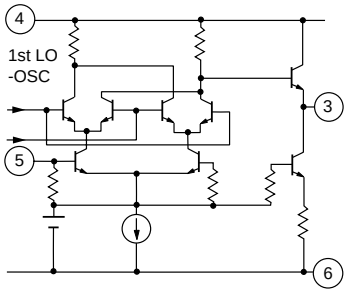
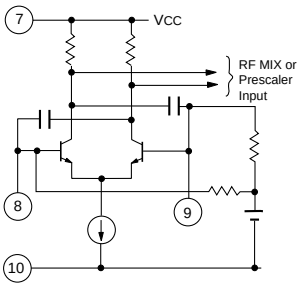
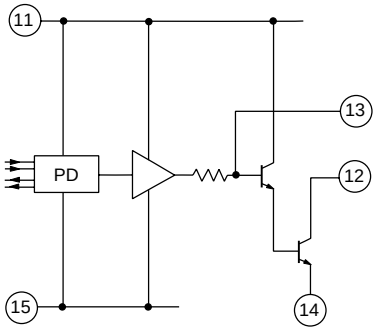
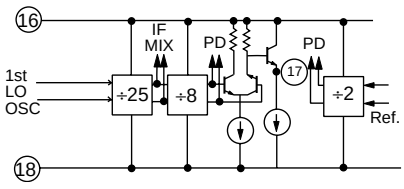
APPLICATION EXAMPLE

GPS Receiver RF Block

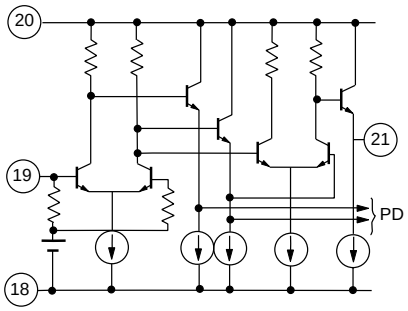
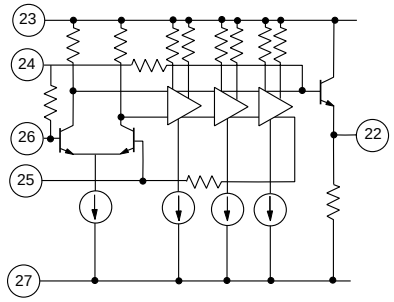
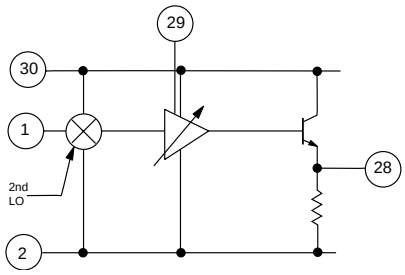


Note: This diagram schematically shows only the UPB1004's internal functions on the system. This diagram does not represent the actual application circuit.

PIN FUNCTIONS

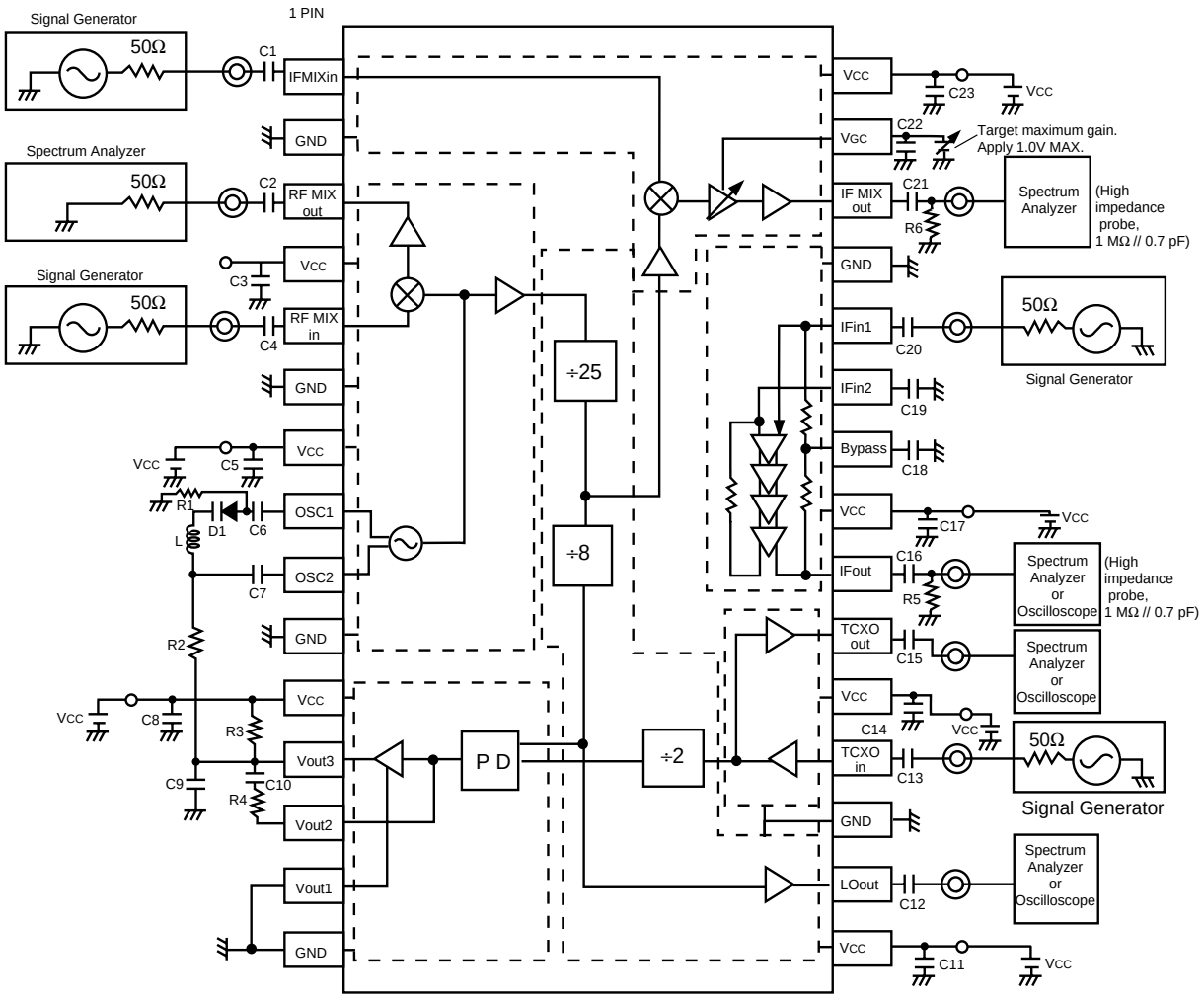
Pin No.	Symbol	Applied Voltage (V)	Pin Voltage (V)	Function and Application	Internal Equivalent Circuit
3	RF MIXout	—	1.68	Output pin of RF mixer. 1st IF filter must be inserted between pin 1 & 3.	
4	VCC (RF MIX)	2.7 to 3.3	—	Supply voltage pin of RF mixer block. This pin must be decoupled with a capacitor (~1000 pF).	
5	RF MIXin	—	1.20	Input pin of RF mixer. 1 575.42 MHz band pass filter must be inserted between pin 5 and external LNA.	
6	GND (RF MIX)	GND	—	Ground pin of RF mixer.	
7	VCC (1stLO-OSC)	2.7 to 3.3	—	Supply voltage pin of differential amplifier for 1st LO oscillator circuit.	
8	1stLO-OSC1	—	1.75	Pins 8 & 9 are each base pins of the differential amplifier for 1st LO oscillator. These pins should be equipped with LC and varactor circuit to oscillate at 1636.8 MHz as VCO.	
9	1stLO-OSC2	—	1.75		
10	GND (1stLO-OSC)	GND	—	Ground pin of differential amplifier for 1st LO oscillator circuit.	
11	VCC (phase detector)	2.7 to 3.3	—	Supply voltage pin of phase detector and active loop filter.	
12	PD-VOUT3	Pull-up with resistor		Pins of active loop filter for tuning VCO. The active transistors configured with darlington pair are built on-chip. Pin 14 should be pulled down with external resistor. Pin 12 to 13 should be equipped with external RC in order to adjust damping factor and cutoff frequency. This tuning voltage output must be connected to varactor diode of 1st LO-OSC.	
13	PD-VOUT2	—	Output in accordance with phase difference		
14	PD-Vout1	GND			
15	GND (phase detector)	GND	—	Ground pin of phase detector and active loop filter.	
16	VCC (divider block)	2.7 to 3.3	—	Supply voltage pin of prescalers.	
17	LOout	—	1.98	Monitor pin of comparison frequency at phase detector.	
18	GND (divider block)	GND	—	Ground pin of prescalers and LOout amplifier.	

PIN FUNCTIONS

Pin No.	Symbol	Applied Voltage (V)	Pin Voltage (V)	Function and Application	Internal Equivalent Circuit
19	TCXOin	—	1.97	Input pin of reference frequency. This pin should be equipped with external TCXO of 16.368 MHz.	
20	V_{CC} (reference block)	2.7 to 3.3	—	Supply voltage pin of input/output amplifiers in reference block.	
21	TCXOout	—	1.75	Output pin of reference frequency. The frequency from pin 19 can be measured at 1 V_{p-p} swing.	
22	2ndIFout	—	1.65	Output pin of 2nd IF amplifier. This output is a 4.092 MHz clipped sinewave.	
23	V_{CC} (2ndIF AMP)	2.7 to 3.3	—	Supply voltage pin of 2nd IF amplifier.	
24	2ndIF bypass	—	2.25	Bypass pin of 2nd IF amplifier input 1. This pin should be grounded through a capacitor.	
25	2ndIFin2	—	2.25	Pin of 2nd IF amplifier input 2. This pin should be grounded through capacitor.	
26	2ndIFin1	—	2.25	Pin of 2nd IF amplifier input 1. 2nd IF filter must be inserted between pins 26 & 28.	
27	GND (2ndIF AMP)	GND	—	Ground pin of 2nd IF amplifier.	
28	IF MIXout	—	1.80	Output pin from IF mixer. IF mixer output signal goes through gain control amplifier before this emitter follower output port.	
29	V_{GC} (IF MIX)	0 to 3.3		Gain control voltage pin of IF mixer output amplifier. This voltage performs forward control (V_{GC} up→Gain down).	
30	V_{CC} (IF MIX)	2.7 to 3.3	—	Supply voltage pin of IF mixer, gain control amplifier and emitter follower transistor.	
1	IF MIXin	—	1.18	Input pin of IF mixer.	
2	GND (IF MIX)	GND	—	Ground pin of IF mixer.	

Note: Ground pattern on the board must be formed as wide as possible to minimize ground impedance.

TEST CIRCUIT



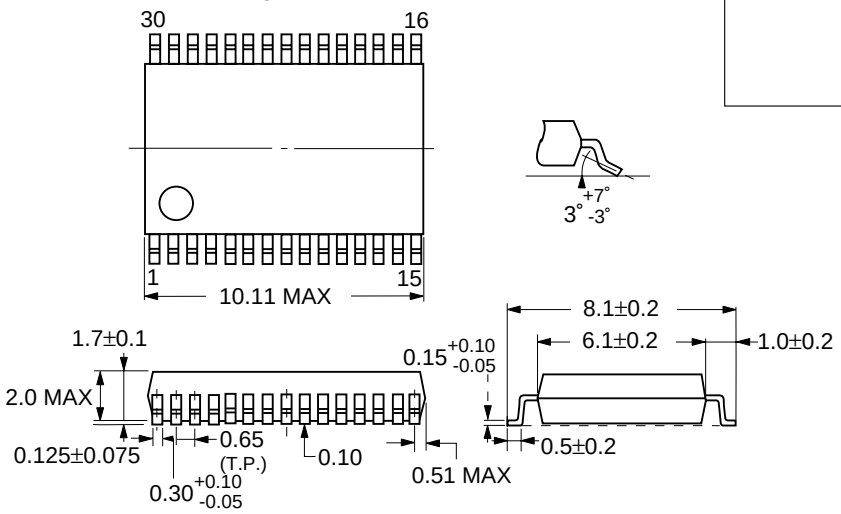
NOTE: Spectrum Analyzer to measure frequency.
Oscilloscope to measure voltage swing.

COMPONENTS LIST

FORM	SYMBOL	VALUE
Chip Capacitor	C1 to C5, C8, C11 to C15,C17, C18, C22, C23	1000 pF
	C6, C7	820 pF
	C9	6600 pF
	C19	9900 pF
	C10	0.2 μF
Ceramic capacitor	C16, C20	0.1 μF
	C21	0.01 μF
Chip Resistor	R1, R2	15 kΩ
	R3	1.5 kΩ
	R4	3 kΩ
	R5, R6	2 kΩ
Varactor Diode	D1	—
Chip Inductor	L	1.57 nH

OUTLINE DIMENSIONS (Units in mm)

Package Outline S30



Note:
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ORDERING INFORMATION

Part Number	Package	Quantity and Form
UPB1004GS-E1	30 Pin plastic SSOP	Embossed tape 16 mm wide. Qty 2.5 kp/reel. Pin 1 is in tape pull-out direction.

INTERNAL BLOCK DIAGRAM