

# NEC's 3 V DUAL DOWNCONVERTER AND PLL FREQUENCY SYNTHESIZER

## UPB1007K

### FEATURES

- **INTEGRATED RF BLOCK:**  
LNA, RF & IF Downconverter + PLL frequency synthesizer
- **STATE OF THE ART 25 GHz ft UHS0 BIPOLAR PROCESS**
- **DOUBLE-CONVERSION:**  $f_{1stIF} = 61.380$  MHz  
 $f_{2ndIF} = 4.092$  MHz
- **ADJUSTABLE GAIN:** 20 dB range MIN
- **FIXED DIVISION PRESCALER**
- **LOW POWER CONSUMPTION:** 25 mA @ 3 V
- **SMALL 36 PIN QFN PACKAGE**  
Flat lead style for better performance
- **TAPE AND REEL PACKAGING AVAILABLE**

### DESCRIPTION

NEC's UPB1007K is a Silicon RFIC designed for low cost GPS receivers. The IC combines an LNA, followed by a double-conversion RF/IF downconverter block and a PLL frequency synthesizer on one chip. The device operates on a 3V supply voltage and is housed in a small 36 pin QFN (Quad Flat No-lead) package, resulting in low power consumption and reduced board space. The device is manufactured using the state of the art UHS0 25 GHz ft silicon bipolar process. NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

### APPLICATIONS

- **LOW POWER HANDHELD GPS RECEIVER**
- **IN-VEHICLE NAVIGATION SYSTEMS**
- **PC/PDA+GPS INTEGRATION**

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.0$ V, unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPB1007K QFN-36		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
I <sub>CC</sub>	Total Circuit Current, No Signals	mA		25	31
V <sub>CC</sub>	Supply Voltage	V	2.7	3.0	3.3

#### LNA ( $f_{RFIN} = 1575.42$ MHz, $Z_L = Z_s = 50 \Omega$ )

Z <sub>LNAin</sub>	RF Input Impedance of LNA	$\Omega$		28 - j38	
Z <sub>LNAop</sub>	RF Output Impedance of LNA	$\Omega$		85 - jx6	
P <sub>1dB</sub> LNA	1 dB Compression, Input matched	dBm		-22	
P <sub>G</sub> LNA	Power Gain LNA, Input matched, P <sub>RFIN</sub> = -60 dBm	dB	14	15	
N <sub>F</sub> LNA	Noise Figure of LNA, Input matched	dB		2.8	3.2

#### Mixer ( $f_{RFIN} = 1575.42$ MHz, $f_{1stLOin} = 1636.80$ MHz, P<sub>LO</sub> = -10 dBm, $f_{1stIF} = 61.38$ MHz, $Z_L = Z_s = 50 \Omega$ )

Z <sub>MIXin</sub>	RF Input Impedance of Mixer	$\Omega$		31 - j103	
P <sub>1dB</sub> MIX	1 dB Compression (refer to input), Input matched	dBm		-25	
P <sub>C</sub> G <sub>MIX</sub>	Power Conversion Gain	dB		21	
N <sub>F</sub> MIX	Noise Figure of Mixer (SSB), Input matched	dB		9.5	10
A <sub>LO-IF</sub>	LO Leakage to IF Pins, P <sub>LO</sub> = -10 dBm	dBm		-40	
A <sub>LO-RF</sub>	LO Leakage to RF Input Pins, P <sub>LO</sub> = -10 dBm	dBm		-48	
Z <sub>MIXout</sub>	RF Output Impedance of Mixer			+152 - j9	

#### PLL

I <sub>CP</sub> OH	PLL Charge Pump High Side Current @ V <sub>CPout</sub> = V <sub>CC</sub> /2	mA		1	
I <sub>CP</sub> OL	PLL Charge Pump Low Side Current @ V <sub>CPout</sub> = V <sub>CC</sub> /2	mA		-1	
f <sub>PD</sub>	Phase Comparison Frequency	MHz		8.184	

#### IF Downconverter Block ( $f_{1stIFin} = 61.38$ MHz, $f_{2ndLOin} = 65.472$ MHz, $f_{2ndIF}$ output = 4.092 MHz, $Z_s = 2k\Omega$ , $Z_L = 2k\Omega$ )

N <sub>F</sub> 2ndMIX	Noise Figure of 2nd IF Mixer (SSB), ( $Z_s = 50\Omega$ )	dB		12	
G <sub>V</sub> 2ndMIX	Voltage Gain of 2nd Mixer/Amplifier, P <sub>1stIF</sub> = -50 dBm	dB		47	
V <sub>GC</sub>	Gain Control Voltage (Voltage at maximum gain)	V		0.5	
D <sub>GC</sub>	Gain Control Range, P <sub>1stIF</sub> = -50 dBm (Voltage at maximum gain)	dB	20		
A <sub>2ndLO1stIF</sub>	2nd LO Isolation to 1st IF Input Pins, V <sub>AGC</sub> = 0 V	dB		-70	
A <sub>2ndLO2ndIF</sub>	2nd LO Isolation to 2nd IF Output Pins, V <sub>AGC</sub> = 0 V	dB		-70	

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$ , unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPB1007K QFN-36		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
<b>2nd IF Amplifier Block</b> ( $f_{2ndIF} = 4.096\text{ MHz}$ , $Z_s = 2\text{ k}\Omega$ , $Z_L = 2\text{ k}\Omega$ )					
GV <sub>LIM</sub>	Voltage Gain of Limiter Amplifier, $P_{IN} = -60\text{ dBm}$	dB		48	
f <sub>BB</sub>	Roll-off Frequency	MHz		110	
<b>Reference Amplifier Block</b>					
V <sub>REFin</sub>	Reference Input Minimum Level	mV <sub>pp</sub>	400	400	
V <sub>REFout</sub>	Reference Output Swing (open collector output), $C_L = 2\text{ pF}/R_L = 10\text{ k}\Omega$	V <sub>pp</sub>	1.1	1.2	1.3
<b>Power Down Control Pins</b>					
V <sub>IH</sub>	Digital Control Input High	V	1.83	1.86	2.15
V <sub>LIL</sub>	Digital Control Input Low	V		0.5	0.6

**ABSOLUTE MAXIMUM RATINGS**<sup>1,2</sup> ( $T_A = 25^\circ\text{C}$ )

SYMBOLS	PARAMETERS	UNITS	RATINGS
V <sub>CC</sub>	Supply Voltage	V	3.6
P <sub>T</sub>	Total Power Dissipation <sup>3</sup>	mW	433
T <sub>OP</sub>	Operating Temperature	°C	-40 to +85
T <sub>STG</sub>	Storage Temperature	°C	-55 to +150

Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. More than two items must not be reached simultaneously.
3.  $T_A = +85^\circ\text{C}$ , mounted on a 50 x 50 x 1.6 mm double-sided copper clad epoxy glass PWB.

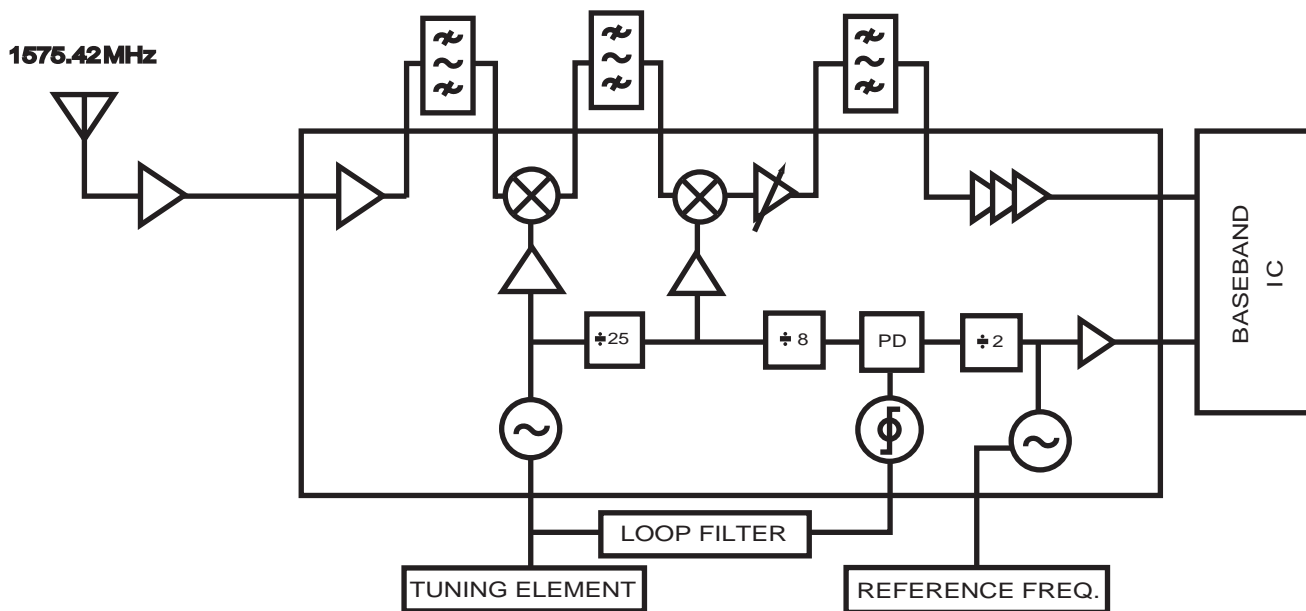
**RECOMMENDED  
OPERATING CONDITIONS**

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V <sub>CC</sub>	Supply Voltage	V	2.7	3.0	3.3
T <sub>OP</sub>	Operating Temperature	°C	-40	+25	+85
f <sub>RFin</sub>	RF Input Frequency	MHz		1575.42	
f <sub>REFin</sub> f <sub>REFout</sub>	Reference Frequency	MHz		16.368	
f <sub>1stLo</sub>	1st LO Oscillating Frequency	MHz		1636.8	
f <sub>1stIFin</sub>	1st IF Input Frequency	MHz		61.38	
f <sub>2ndLOin</sub>	2nd LO Input Frequency	MHz		65.472	
f <sub>2ndIFin</sub> f <sub>2ndIFout</sub>	2nd IF Input/Output Frequency	MHz		4.092	
V <sub>IH</sub>	Power Down Control Voltage "High"	V	1.8		3
V <sub>LIL</sub>	Power Down Control Voltage "Low"	V			0.6

### CURRENT BUDGET

SYMBOL	PARAMETER AND CONDITIONS	UNITS	MIN	TYP	MAX
<b>IC Performance Parameters</b>					
Vcc	Supply Voltage	V	2.7	3.0	3.3
Icc	Total Circuit Current, Vcc = 3.0 V, no signal	mA		25	31
Icc_PL	Power Down Node Current	mA		0.15	
Icc_XO	Oscillator Supply Current, (Pin 15 = 0 V, Pin 16 = 3 V)	mA		2.7	
Icc_RX	Receiver Supply Current, (Pin 15 = 0 V, Pin 16 = 3 V)	mA		22.3	
<b>Functional Blocks Current Details</b>					
Icc_LNA	Supply Current of LNA, RF off	mA		2.6	
Icc_MIX1	Supply Current of RF Mixer, RF off	mA		6.7	
Icc_MIX2	Supply Current of IF Mixer, RF off	mA		3.5	
Icc_IFAMP	Supply Current of IF Amplifier, RF off	mA		1.1	
Icc_XO	Crystal Oscillator Supply Current	mA		2.7	
Icc9	PLL Supply Current	mA		6.3	
Icc_CF	Control Functions Supply Current	μA		2.1	
VIL	Power Down Pin Logic LOW Level	V			0.6
VIH	Power Down Pin Logic HIGH Level	V	1.8		
τd_PON	Power-on Response Time	ms		3	

### APPLICATION EXAMPLE



**PIN FUNCTIONS**

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
1	LNAout	Output pin of LNA. Output biasing and matching required as it is an open collector output.	
2	Vcc (Vreg)	Supply voltage pin of regulator mixer block.	
3	GND (Vreg)	Ground pin of regulator reference cell.	
4	RF MIXin	Input pin of RF mixer. 1575.42 MHz band pass filter can be inserted between pin 1 and mixer input.	
5	GND (MIX)	Ground pin of RF mixer cell.	
6	1stLO-OSC1	Pins 6 & 7 are base pins of the differential amplifier for 1st LO oscillator. These pins should be equipped with LC and varactor circuits to oscillate at 1636.8 MHz.	
7	1stLO-OSC2		
8	Vcc (1stLO-OSC)	Supply voltage pin of differential amplifier for 1st LO oscillator circuit (VCO).	
9	Vcc (Charge Pump)	Supply voltage pin of the phase detector charge pump.	
10	PD-out	This is a current mode charge pump output for connection to a passive RC loop filter for driving the external varactor diode of 1stLO-OSC.	
11	GND (Charge Pump)	Ground pin of phase detector charge pump.	

**PIN FUNCTIONS**

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
12	Vcc (Divider Block)	Supply voltage pin of prescaler, phase detector, crystal oscillator, VCO buffer.	
13	LO_out	Monitor pin of frequency at phase detector.	
14	XO_out	Monitor pin of oscillator $\pm 2$ output at phase detector.	
15	PD1	Power down control pin Low = Whole chip off except XTAL osc. High = Whole chip on except XTAL osc.	
16	PD2	Reference block standby mode. Low = Reference block disabled. High = Reference block enabled.	
17	REFout	Output pin of reference frequency. The frequency from pin 17 can be taken out as 1Vp-p swing.	

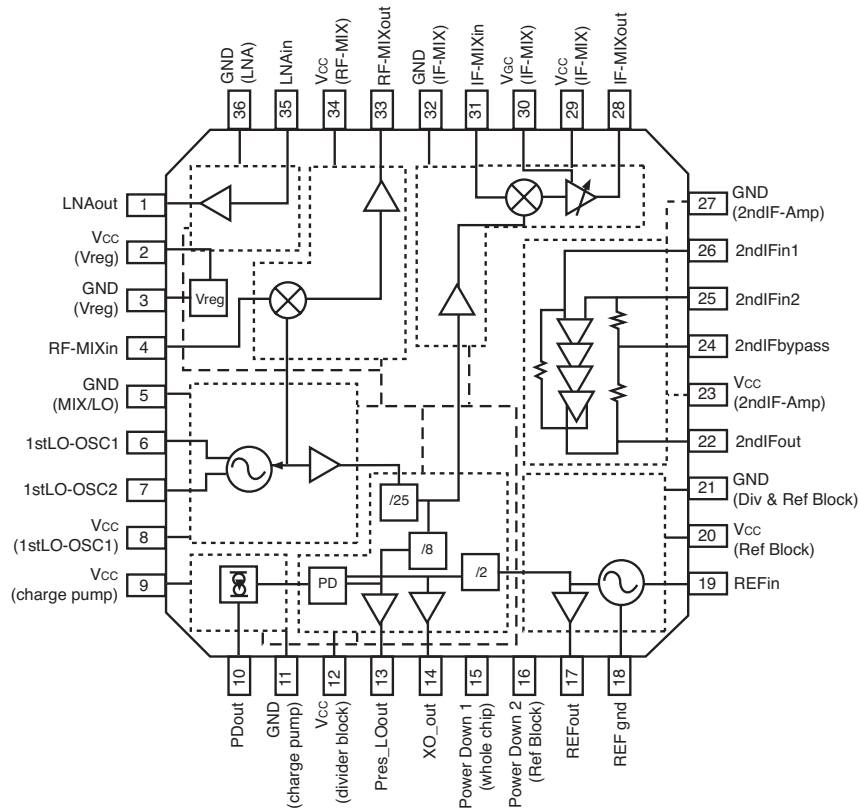
**PIN FUNCTIONS**

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
18	REF gnd	Differential oscillator input. This pin should be grounded via a capacitor.	
19	REF <sub>in</sub>	Input pin of the reference frequency buffer. This pin should be equipped with an external 16.368 MHz oscillator (e.g. TCXO).	
20	V <sub>cc</sub> (Ref Block)	Supply voltage pin of output charge pump of the oscillator.	
21	GND (Ref Block)	Ground pin of the oscillator, prescaler, phase detector and VCO.	
22	2nd IF <sub>out</sub>	Output pin of 2nd IF amplifier. This pin output 4.092 MHz clipped sinewave. This pin should be equipped with external inverter to adjust level to next stage on user's system.	
23	V <sub>cc</sub> 2ndIFAMP	Supply voltage pin of 2ndIF amplifier	
24	2ndIF bypass	Bypass pin of 2nd IF amplifier input. This pin should be grounded via a capacitor.	
25	2ndIF <sub>in1</sub>	Pin 1 of 2nd IF amplifier input . 2nd IF filter can be inserted between 25 & 28.	
26	2ndIF <sub>in2</sub>	Pin 2 of 2nd IF amplifier input. This pin should be grounded via a capacitor.	
27	GND (2ndIF AMP)	Ground pin of 2nd IF amplifier.	
28	IF MIX <sub>out</sub>	Output pin from IF mixer. IF mixer output signal goes through gain control amplifier before this emitter follower output port.	
29	V <sub>cc</sub> (IF MIX)	Supply voltage pin of IF mixer, gain control amplifier.	

**PIN FUNCTIONS**

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
30	V <sub>Gc</sub> (IF MIX)	Gain control voltage pin of IF mixer output amplifier. This voltage performs forward control, i.e., (V <sub>Gc</sub> up → Gain down).	
31	IF-MIXin	Input pin of IF mixer and IF VAGC.	
32	GND (IF-MIX)	Ground pin of IF mixer and IF VAGC.	
33	RF-MIXout	Output pin of RF mixer . 1st IF filter must be inserted between pins 31 and 33.	
34	V <sub>cc</sub> (RF-MIX)	Supply voltage pin of RF mixer block. This pin must be decoupled with capacitor (e.g. 1000 pF).	
35	LNAin	Input pin of low noise amplifier. Optimal input matching required for low noise performance.	See Pins 1-3
36	GND (LNA)	Ground pin of LNA.	

INTERNAL BLOCK DIAGRAM



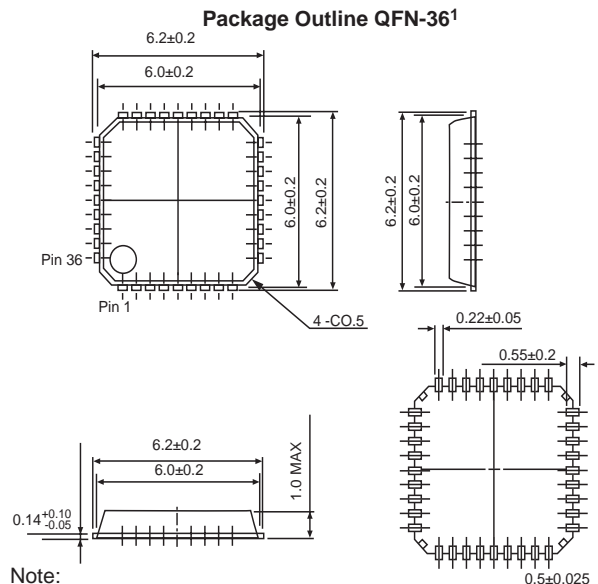
ORDERING INFORMATION

Part Number	Package
UPB1007K	36 Pin plastic QFN

OUTLINE DIMENSIONS (Units in mm)

ACTUAL SIZE (Units in mm)

Package Outline QFN-36



Note:  
1. The solder pads on each corner should be grounded.

Life Support Applications

These NEC products are not intended for use in life support devices, appliances, or systems where the malfunction of these products can reasonably be expected to result in personal injury. The customers of CEL using or selling these products for use in such applications do so at their own risk and agree to fully indemnify CEL for all damages resulting from such improper use or sale.

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