CEL

NEC's LOW POWER GPS RF RECEIVER BIPOLAR ANALOG + INTEGRATED CIRCUIT

UPB1009K

DESCRIPTION

The μPB1009K is a silicon monolithic IC developed for GPS receivers. This IC integrates a full VCO, second IF filter, 4-bit ADC, and digital control interface to reduce cost and mounting space. In addition, its power consumption is low.

Moreover, use of a TCXO with frequency of 16.368 MHz/16.384 MHz, 14.4 MHz, 19.2 MHz, or 26 MHz switchable with an on-chip divider is possible.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

FEATURES

- Double conversion : f_{REFin} = 16.368 MHz, $f_{1stIFin}$ = 61.380 MHz, $f_{2ndIFin}$ = 4.092 MHz
  : f_{REFin} = 14.4, 16.384, 19.2, 26 MHz, $f_{1stIFin}$ = 62.980 MHz, $f_{2ndIFin}$ = 2.556 MHz
- Multiple system clocks : On-chip switchable frequency divider (1/N = 100, 3/256, 9/1024, 65/4096)
- A/D converter : On-chip 4-bit A/D converter
- High-density RF block : On-chip VCO tank circuit and 2ndIF filter
- Supply voltage : V_{CC} = 2.7 to 3.3 V
- Low current consumption : I_{CC} = 26.0 mA TYP. @ V_{CC} = 3.0 V, N = 100
- High-density surface mountable : 44-pin plastic QFN

APPLICATIONS

- Consumer use GPS receiver of reference frequency 16.368 MHz, 2nd IF frequency 4.092 MHz
- Consumer use GPS receiver of reference frequency 14.4, 16.384, 19.2, 26 MHz, 2ndIF frequency 2.556 MHz

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

ORDERING INFORMATION

Part Number	Package	Supplying Form
μPB1009K-E1	44-pin plastic QFN	• 12 mm wide embossed taping • Pin 1 indicates pull-out direction of tape • Qty 1.5 kpcs/reel, Dry pack specification

Remark To order evaluation samples, contact your nearby sales office.
Part number for sample order: μPB1009K

PRODUCT LINE-UP (T_A = +25°C, V_{CC} = 3.0 V)

Type	Part Number	Functions (Frequency unit: MHz)	V_{CC} (V)	I_{CC} (mA)	CG (dB)	Package	Status
Clock Frequency Specific 1 chip IC	μPB1009K	Pre-amplifier + RF/IF down-converter + PLL synthesizer REF = 16.368 1stIF = 61.380/2ndIF = 4.092 REF = 14.4, 16.384, 19.2, 26 1stIF = 62.980/2ndIF = 2.556 On-chip 4-bit ADC	2.7 to 3.3	26.0		44-pin plastic QFN	New Device
	μPB1008K	LNA + Pre-amplifier + RF/IF down-converter + PLL synthesizer REF = 27.456 1stIF = 175.164/2ndIF = 0.132 On-chip 2-bit ADC	2.7 to 3.3	18.0	100 to 120	36-pin plastic QFN	
	μPB1007K	Pre-amplifier + RF/IF down-converter + PLL synthesizer REF = 16.368 1stIF = 61.380/2ndIF = 4.092	2.7 to 3.3	25.0	100 to 120	36-pin plastic QFN	Available
	μPB1005K	REF = 16.368 1stIF = 61.380/2ndIF = 4.092				36-pin plastic QFN	

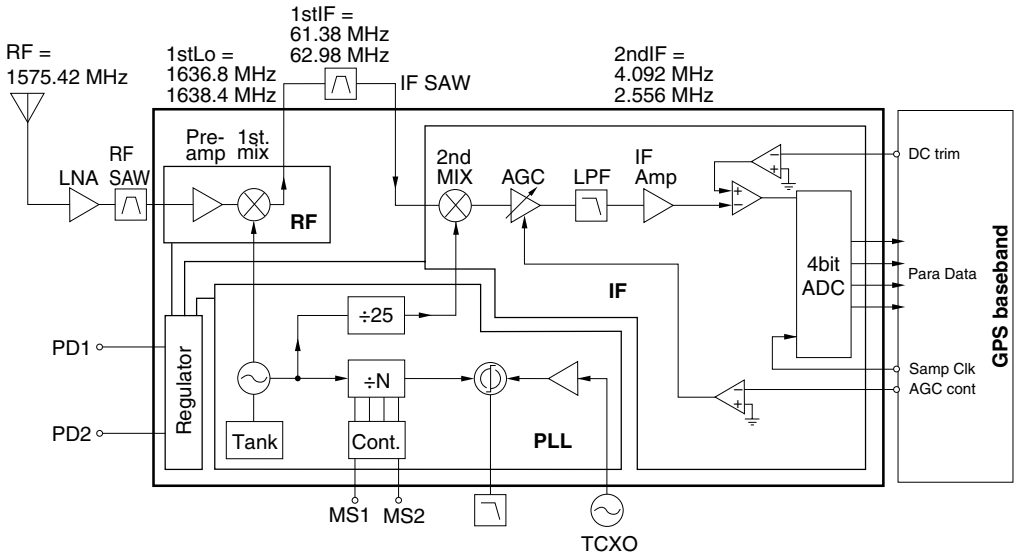
Remark Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.

SYSTEM APPLICATION EXAMPLE

GPS receiver RF block diagram

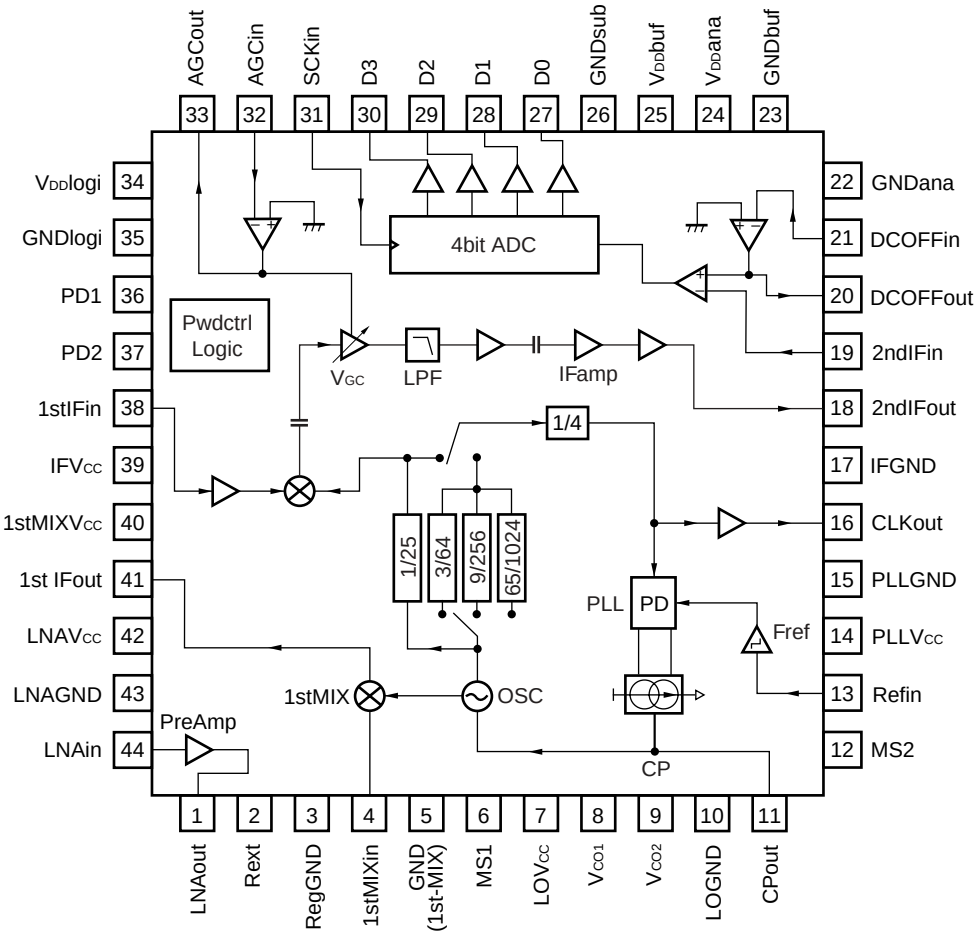
PD1 and PD2 in the figure are Power Save Mode control pins.

MS1 and MS2 in the figure are TXCO (GPS, W-CDMA, PDC, GSM) control pins.

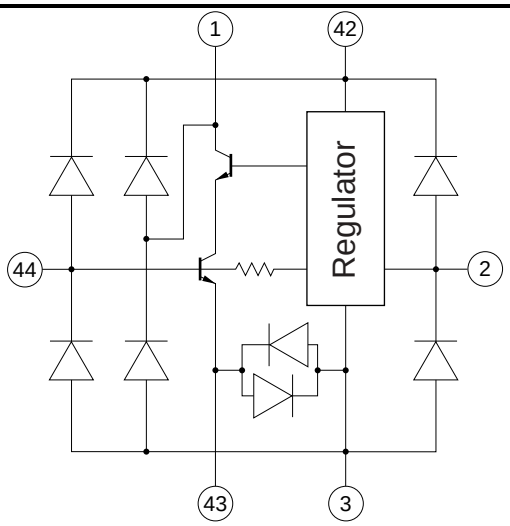
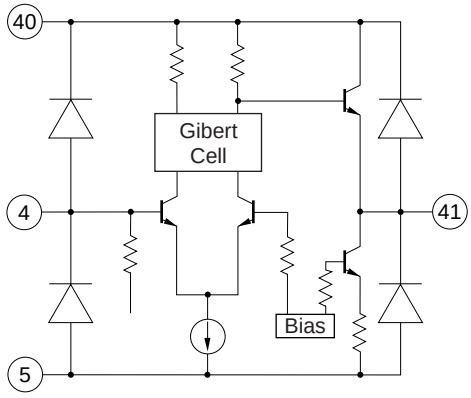


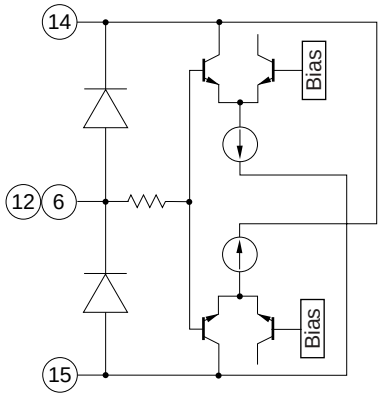
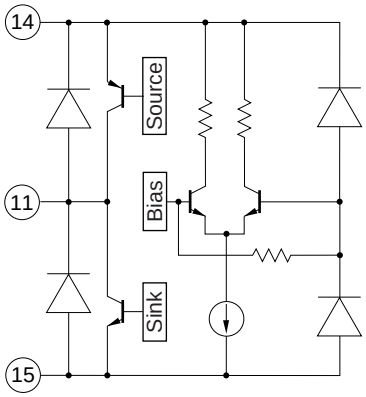
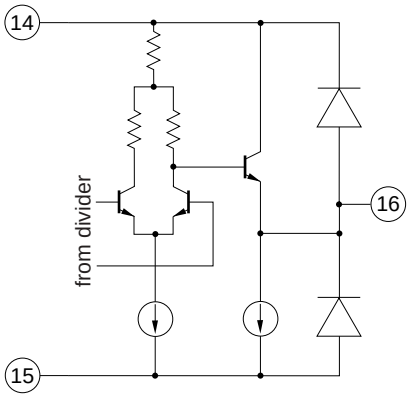
Caution This diagram schematically shows only the μPB1009K's internal functions on the system. This diagram does not present the actual application circuits.

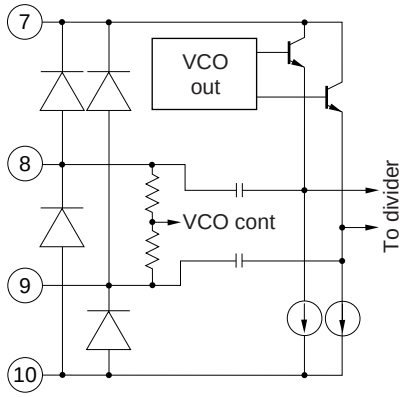
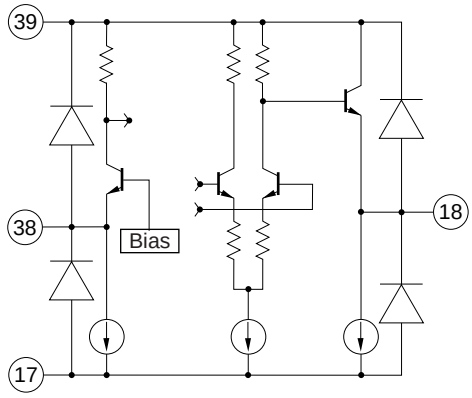
PIN CONNECTION AND INTERNAL BLOCK DIAGRAM

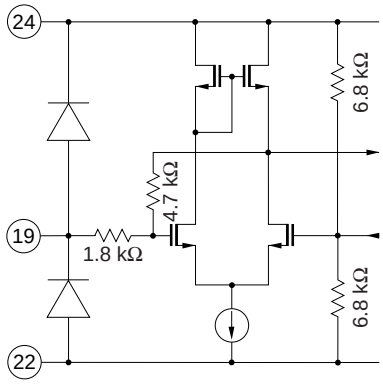
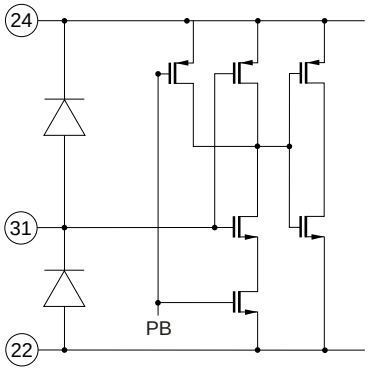
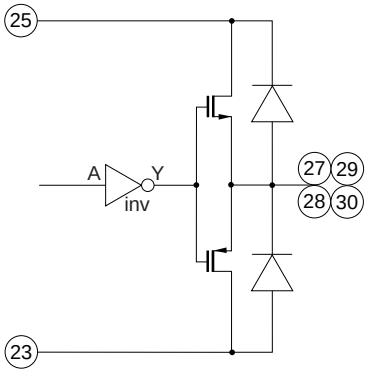
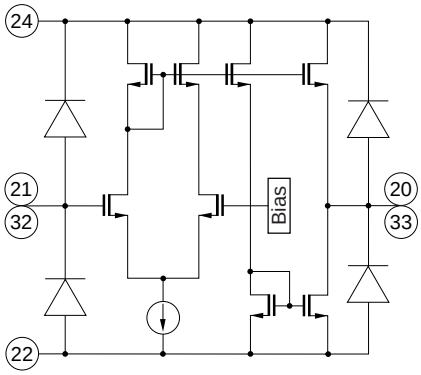


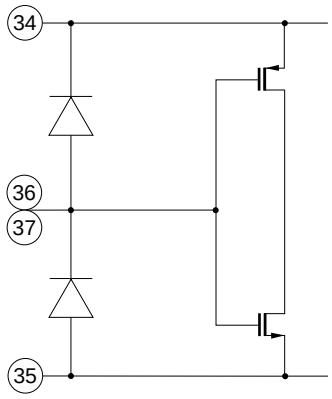
PIN EXPLANATION

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
1	PreAMPout	Output pin of preamplifier.	
2	Rext	Connect a resistor for the reference constant-current power supply to this pin. Ground this pin at 22 kΩ.	
3	RegGND	Ground pin for regulator.	
42	PreAmpV_{CC}	Power supply voltage pin for preamplifier. Connect a bypass capacitor to this pin to reduce the high-frequency impedance.	
43	PreAmpGND	Ground pin of preamplifier.	
44	PreAmpin	Input pin of preamplifier.	
4	1stMIXin	1stMIX input pin.	
5	1stMIXGND	Ground pin for first MIX.	
40	1stMIXV_{CC}	Power supply voltage pin for RF mixer. Connect a bypass capacitor to this pin to reduce the high-frequency impedance.	
41	1stIFout	Output pin of RF mixer. Insert an IFSAW filter between this pin and pin 37. The VCO oscillation signal can be monitored on this pin.	

Pin No.	Pin Name	Function and Application			Internal Equivalent Circuit
6 12	MS1 MS2	Low : 0 to 0.3 (V) High : V_{CC} – 0.3 to V_{CC} (V)	MS1 : L MS2 : L	TCXO : 16.368, 16.384 MHz	
			MS1 : L MS2 : H	TCXO : 19.2 MHz	
			MS1 : H MS2 : L	TCXO : 14.4 MHz	
			MS1 : H MS2 : H	TCXO : 26 MHz	
11	CPout	Output pin of charge pump. Connect external R and C to this pin to set a dumping factor and natural angular frequency (I_{sink} = I_{source} = 0.45 mA).			
13	Refin	Reference frequency input pin. Connect an external reference transmitter (such as TCXO) to this pin.			
14	PLLV_{CC}	Power supply voltage pin of PLL. Connect a bypass capacitor to this pin to reduce the high-frequency impedance.			
15	PLLGND	Ground pin of PLL.			
16	CLKout	Clock (f_{TCXO}) output pin (IC test pin).			

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
7	LoV_{CC}	Power supply voltage pin of VCO. Connect a bypass capacitor to this pin to reduce the high-frequency impedance.	
8 9	VCO1 VCO2	IC test pin. Leave this pin open when the μPB1009K is mounted on board.	
10	LoGND	Ground pin of VCO.	
17	IFGND	Ground pin of IF block.	
18	2ndIFout	Output pin of IF amplifier.	
38	1stIFin	Input pin of second IF mixer.	
39	IFV_{CC}	Power supply voltage pin of IF block.	

Pin No.	Pin Name	Function and Application	Internal Equivalent Circuit
19	2ndIFin	Input pin of ADC buffer amplifier.	
20	DCOFFout	Output pin of DC trimming OP amplifier.	
21	DCOFFin	DC trimming pulse input pin. Connect this pin to pin 20 via a capacitor to convert an input pulse signal into DC.	
22 23	GNDana GNDbuf	Ground pin for OP amplifier and ADC power supply.	
24	V_{DD}ana	Power supply pin for OP amplifier and ADC comparator.	
25	V_{DD}buf	Power supply pin for output driver amplifier of ADC. Connect this pin to the ground pin of the A/D converter via a bypass capacitor to reduce the high-frequency impedance.	
26	GNDsub	Ground pin of CMOS substrate.	
27 28 29 30	D0 D1 D2 D3	Digital signal output pins. LSB = D0, MSB = D3	
31	SCKin	Sampling clock signal input pin.	
32	AGCin	AGC control pulse signal input pin.	
33	AGCout	AGC control signal output pin.	

Pin No.	Pin Name	Function and Application			Internal Equivalent Circuit
34	V_{DD}logi	Power supply voltage pin for power control logic.			
35	GNDlogi	Ground pin for power control logic.			
36 37	PD1 PD2	Low : 0 to 0.3 (V) High : V_{CC} – 0.3 to V_{CC} (V)	PD1 : L PD2 : L	Sleep mode (all circuits off).	
			PD1 : L PD2 : H	Warm-up mode (PLL on).	
			PD1 : H PD2 : L	Calibration mode (PLL + IF + ADC on).	
			PD1 : H PD2 : H	Active mode (all circuits on).	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = +25°C	3.6	V
Total Circuit Current	$I_{CCTotal}$	T_A = +25°C	100	mA
Power Dissipation	P_D	T_A = +25°C **Note**	266	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +125	°C

Note Mounted on double-sided copper-clad 50 × 50 × 1.6 mm epoxy glass PWB

RECOMMENDED OPERATING RANGE

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
Operating Ambient Temperature	T_A	–30	+25	+85	°C
RF Input Frequency	f_{RFin}	–	1 575.42	–	MHz
1st LO Oscillating Frequency	$f_{1stLOin}$	–	1 636.8/1 638.4	–	MHz
1st IF Input Frequency	$f_{1stIFin}$	–	61.38/62.98	–	MHz
2nd LO Input Frequency	$f_{2ndLOin}$	–	65.472/65.536	–	MHz
2nd IF Input Frequency	$f_{2ndIFin}$	–	4.092/2.556	–	MHz
Reference Input/Output Frequency	f_{REFin} f_{REFout}	–	TCXO	–	MHz
Clock mode control voltage (Low Level)	V_{IL1}	0	–	0.3	V
Clock mode control voltage (High Level)	V_{IH1}	V_{CC} – 0.3	–	V_{CC}	V
Power-down control voltage (Low Level)	V_{IL2}	0	–	0.3	V
Power-down control voltage (High Level)	V_{IH2}	V_{CC} – 0.3	–	V_{CC}	V

POWER-DOWN CONTROL MODE

The μPB1009K consists of an RF block, an IF block, and a PLL block. By controlling reduction of power to each block (by applying a voltage to the PD1 and PD2 pins), the following four modes can be used.

Mode No.	Mode Name	Test Conditions		RF Block	IF Block (IF + ADC)	PLL Block
		PD1	PD2			
1	Active mode	L	H	ON	ON	ON
2	Calibration mode	H	H	OFF	ON	ON
3	Warm-up mode	H	L	OFF	OFF	ON
4	Sleep mode	L	L	OFF	OFF	OFF

Caution To use only the active mode and sleep mode, fix PD1 to L and select the desired mode with PD2.

REFERENCE CLOCK CONTROL MODE

The divided frequency can be selected as follows so that it can be shared with the TCXO of each system.

TCXO Frequency	Test Conditions		1/N	Phase Comparison Frequency
	PD1	PD2		
16.368 MHz (GPS) 16.384 MHz (GPS)	L	L	1/100	16.368 MHz 16.384 MHz
19.2 MHz (W-CDMA)	L	H	3/256	19.2 MHz
14.4 MHz (PDC)	H	L	9/1024	14.4 MHz
26 MHz (GSM)	H	H	65/4096	26 MHz

Caution When the reference clock frequency is 16.368 MHz, the 1stIF frequency and 2ndIF frequency are 61.38 MHz and 4.092 MHz, respectively. They are respectively 62.98 MHz and 2.556 MHz in all other cases.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Rest current of overall IC in each mode	Rest status without input signal, including sampling clock. MS1 = L, MS2 = L					
Sleep mode Note	I_s	PD1 = L, PD2 = L	1.3	2.2	3.5	mA
Warm-up mode	I_w	PD1 = H, PD2 = L	10.5	13.0	15.5	mA
Calibration mode	I_c	PD1 = H, PD2 = H	18.0	22.0	25.3	mA
Active mode	I_a	PD1 = L, PD2 = H	22.1	26.0	30.0	mA
Rest current of PLL block in each clock mode	Current of PLL block. Overall current in calibration mode and active mode increases from that in basic mode (MS1 = L, MS2 = L). PD1 = H, PD2 = L.					
Current when 1/100 divider is used	I_{w1}	MS1 = L, MS2 = L	5.3	6.5	7.6	mA
Current when 256/3 divider is used	I_{w2}	MS1 = L, MS2 = H	9.7	11.3	12.6	mA
Current when 1024/9 divider is used	I_{w3}	MS1 = H, MS2 = L	10.2	12.1	13.5	mA
Current when 4096/65 divider is used	I_{w4}	MS1 = H, MS2 = H	10.4	12.3	13.9	mA
Maximum mode control pin current						
6 pin	MS1	H application	–	–	20	μA
		L application	–20	–	–	μA
12 pin	MS2	H application	–	–	20	μA
		L application	–20	–	–	μA
36 pin	PD1	H application	–	–	1	μA
		L application	–1	–	–	μA
37 pin	PD2	H application	–	–	1	μA
		L application	–1	–	–	μA
<Pre-amplifier>	f_{RFin} = 1 575.42 MHz					
Circuit Current 1	I_{CC1}	No Signals, 1-pin current	1.9	2.3	2.7	mA
Power Gain	G_{LNA}	P_{RFin} = –40 dBm	12.5	15.0	17.5	dB
Noise Figure	NF_{LNA}	f_{RFin} = 1 575 MHz	–	3.0	3.5	dB
Saturated Output Power	$P_{O(SAT)LNA}$	P_{RFin} = –10 dBm	–4.0	–2.7	–	dBm
Input 1dB Compression Level	P_{LNA-1}	f_{RFin} = 1 575.42 MHz	–25	–21.8	–	dBm
Input 3rd Order Intercept Point	IIP_{3LNA}	f_{RFin} = 1 575.42 MHz, 1 576.42 MHz	–12	–9.5	–	dBm
Input Inpedance	Z_{inLNA}	Calculated from S-parameter where input DC cut capacitance = 1 nF, output load L = 100 n, and DC cut capacitance = 1 nF	–	11.2 – j21.5	–	Ω
Output Inpedance	Z_{outLNA}		–	16.4 – j136.6	–	Ω

Note Most of the current flows into the ADC ladder resistor (V_{DD}ana → GNDana) in the sleep mode, and the sleep mode current between other V_{CC} (V_{DD}) and GND is 10 μA maximum.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
<RF mixer>	f_{RF} = 1 575.42 MHz, $f_{1stLOin}$ = 1 636.80 MHz, f_{1stIF} = 61.38 MHz						
Circuit Current 2	I_{CC2}	No Signals, 40 pin current		2.0	2.5	3.0	mA
RF Conversion Gain	CG_{RF}	$P_{RFMIXin}$ = –40 dBm		14.0	16.1	19.0	dB
Noise Figure	$SSBNF_{RFMIX}$	SSBNF = 10*log (2*DSBNF (Linear value) –1) MHz		–	12.8	16.0	dB
Maximum IF Output	$P_{O\ (SAT)\ RFMIX}$	$P_{RFMIXin}$ = –10 dBm		–4.0	–0.8	–	dBm
Input 1dB Compression Level	$P_{RFMIX-1}$	$f_{RFMIXin}$ = 1 575.42 MHz		–29.0	–25.5	–	dBm
Input 3rd Order Intercept Point	IIP_{3RFMIX}	$f_{RFMIXin}$ = 1 575.42 MHz, 1 576.42 MHz f_{1stLO} = 1 636.8 MHz		–19.0	–17.2	–	dBm
LO Leakage to IF Pin	LO_{IF}	Leakage of 1 636.8 MHz frequency when VCO oscillates correctly.		–	–34.5	–30	dBm
LO Leakage to RF Pin	LO_{RF}			–	–54.7	–30	dBm
Input Inpedance	Z_{inMIX}	Calculated from S-parameter where input DC cut capacitance = 1 nF and output DC cut capacitance = 1 nF		–	50.1 – j22.3	–	Ω
Output Inpedance	Z_{outMIX}			–	57.3 + j2.6	–	Ω
<IF mixer, LPF, IFamp>	f_{1stFin} = 61.38 MHz, $f_{2ndLOin}$ = 65.472 MHz, Z_L = 2 kΩ						
Circuit Current 3	I_{CC3}	No Signals, 39 pin current		6.3	7.3	8.5	mA
IF Conversion Gain	$CG_{(GV)\ IF}$	V_{AGC} = 0.5 V		66.0	70.3	75.0	dB
		V_{AGC} = 1.5 V		45.0	51.2	58.0	dB
		V_{AGC} = 2.5 V		19.5	26.4	33.5	dB
In Band Gain Fluctuation	⊿CG1	3.092 to 5.092 MHz		–	0.7	1.0	dB
Out Of Band Attenuation	⊿CG2	Gain difference at 4.092 MHz and 9.092 MHz, V_{AGC} = 0.5 V		20.0	25.0	–	dB
Conversion Gain Range	CG_{Range}	V_{AGC} = 0 to 2.5 V		32.5	43.9	–	dB
IF · SSB Noise Figure	NF_{IF}	V_{AGC} = 0.5 V (at maximum gain)		–	13.7	17.5	dB
Maximum 2ndIF Output	$V_{O\ (SAT)\ IF}$	P_{in} = –50 dBm, V_{AGC} = 0.5 V		1.0	1.3	–	V_{PP}
Input 1dB Compression Level	P_{IF-1}	$f_{1stIFin}$ = 61.38 MHz	V_{AGC} = 0.5 V	–70.5	–64.4	–	dBm
			V_{AGC} = 1.5 V	–53.5	–44.9	–	dBm
			V_{AGC} = 2.5 V	–37.0	–30.6	–	dBm
Input 3rd Order Intercept Point	IIP_{3IF}	$f_{1stIFin1}$ = 61.28 MHz	V_{AGC} = 0.5 V	–56.0	–51.3	–	dBm
		$f_{1stIFin2}$ = 61.38 MHz	V_{AGC} = 1.5 V	–38.0	–30.7	–	dBm
		f_{2ndLO} = 65.472 MHz	V_{AGC} = 2.5 V	–27.0	–21.4	–	dBm
Input Inpedance	Z_{inIF}	Calculated from S-parameter where input DC cut capacitance = 1 nF and output DC cut capacitance = 100 nF		–	69.3 – j4.8	–	Ω
Output Inpedance	Z_{outIF}			–	163 + j3.8	–	Ω

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.0 V)

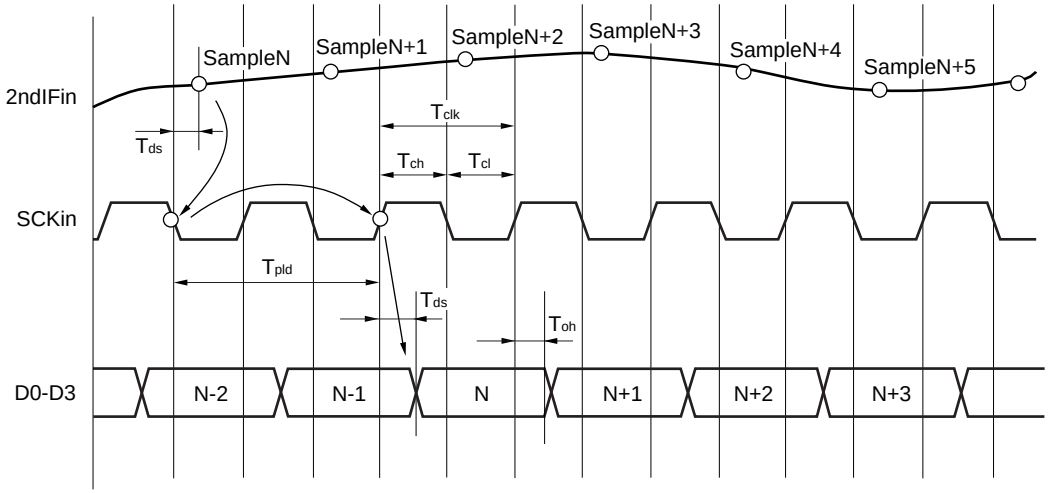
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
<PLL Synthesizer>						
Circuit Current 4	I_{CC4}	PLL, VCO current, MS1 = L, MS2 = L	8.0	9.5	10.6	mA
Charge Pump Output Current	I_{cpsink}	$V_{13\ pin} = V_{CC}/2$	–0.55	–0.45	–0.35	mA
	$I_{cpsource}$		0.35	0.45	0.55	mA
Loop Filer Output (High Level)	V_{OH}		V_{CC}–0.3	–	–	V
Loop Filer Output (Low Level)	V_{OL}		–	–	0.2	V
Reference Input Level	V_{REFin}		–	0.2	1.6	V_{PP}
VCO Modulation Sensitivity	KV	Center frequency	–	100	–	MHz
VCO Control Voltage	VT	When PLL is Locked	0.5	1.3	2.0	V
C/N	C/N	⊿10 kHz	70.0	81.0	–	dBc/Hz
<A/D Converter>						
Circuit Current 5	I_{CC5}		3.1	4.1	5.4	mA
Resolution	ResAD		–	4	–	bits
Sampling Clock	fs		–	–	20	MHz
Input Band Width	ADBW		5.1	–	–	MHz
Integral Non-linear Error	INL	DC characteristics	–	0.2	1.0	LSB
Signal-to-noise Ratio	SNR	IF = 5.17 MHz, fs = 20.48 MHz	22.0	25.3	–	dB
Signal-to-noise + Distortion Ratio	SINAD	IF = 5.17 MHz, fs = 20.48 MHz	20.0	25.1	–	dB
Number	ENOB	ENOB = (SINAD–1.763)/6.02	3.0	3.9	–	bits
Total Harmonic Distortion Ratio	THD	IF = 5.17 MHz, fs = 20.48 MHz Second-degree to fifth-degree distortion components	–	–40	–30	dBc

Remarks 1. Timing characteristics of ADC during normal operation

A buffer amplifier is internally inserted before the ADC core of the μPB1009K. The bias of this buffer amplifier is controlled by the signal input from the DC trim pin, and is used to eliminate the DC offset of the ADC. Because the ladder resistor of the ADC is directly connected between V_{DD}ana and GNDana, changes in V_{DD}ana affect the resolution of the ADC.

As illustrated in the operation timing chart below, the data of SampleN is pipeline delayed by 1.5 clocks during normal operation, and is output at the rising edge of the sample clock with output delay time Tod. When the operation is changed from normal operation to power-down operation, the status of the output data immediately before the power-down operation is retained (drive status).

(a) Normal Operation



○: Analog signal sampling timing

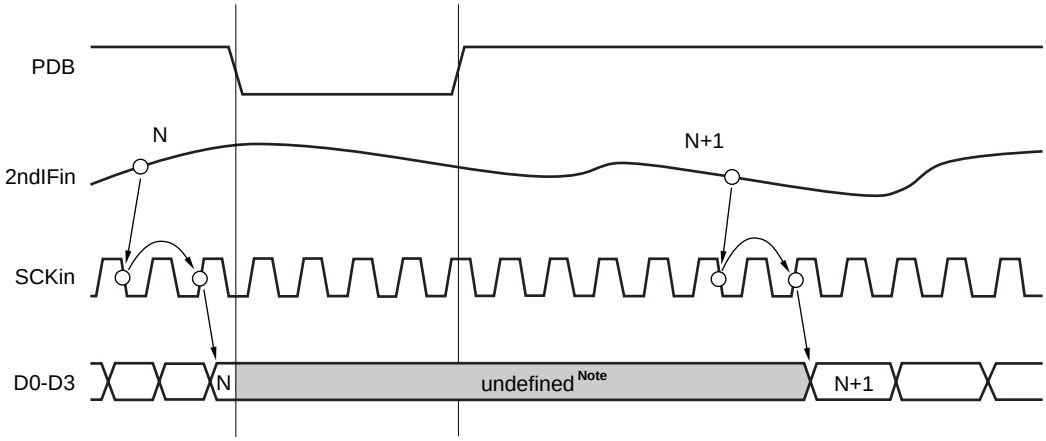
The following table shows each timing parameter for reference purposes.

Symbol	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
T_{od}	Output Delay	C_L = 10 pF, f_{clk} = 19.2 MHz	–	–	12	ns
T_{pld}	Pipeline Delay		–	1.5	–	clock
T_{ds}	Sampling Delay (Aperture Delay)		–	2	–	ns
T_{oh}	Output Hold Time		2	–	–	ns

Remarks 2. Power-down timing characteristics of ADC

The output code of the ADC of the μPB1009K is undefined for 7.5 clocks after the power-down signal is cleared when the ADC returns from the power-down status to normal operation.

(b) Power-down Operation



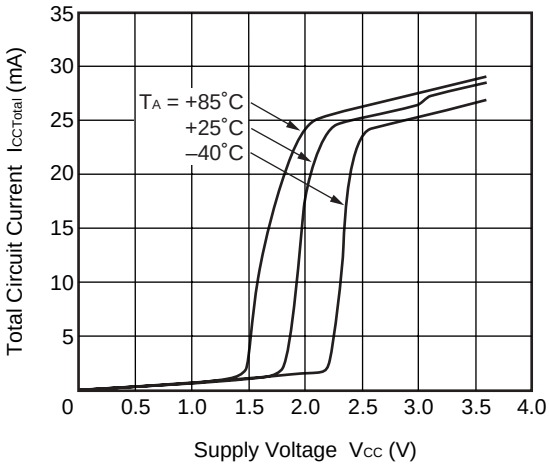
○: Analog signal sampling timing

Note The output data is undefined from the start of the power-down operation to the 7.5th clock from the falling edge of the clock at which the power-down operation is cleared.

TYPICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.0 V, unless otherwise specified)

— IC TOTAL CHARACTERISTICS —

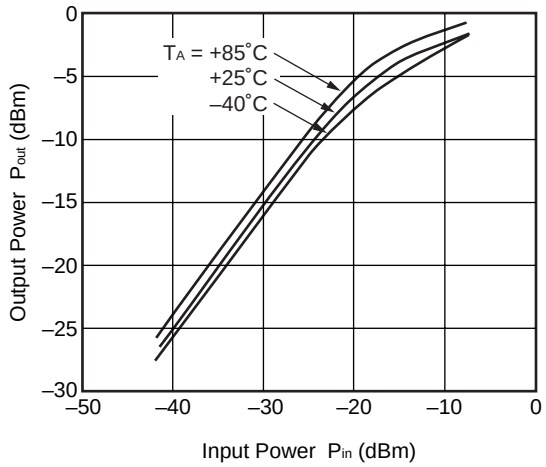
TOTAL CIRCUIT CURRENT
vs. SUPPLY VOLTAGE



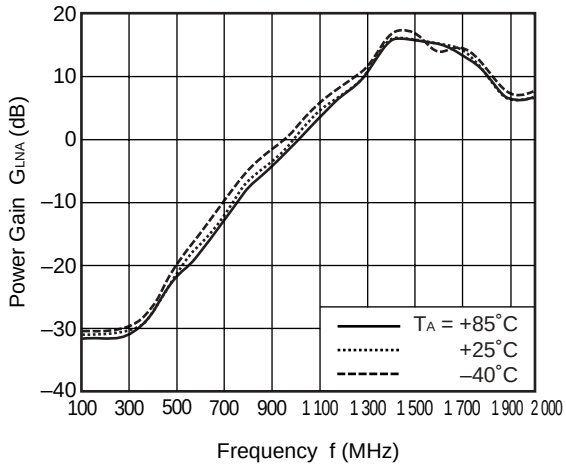
Remark The graphs indicate nominal characteristics.

— PRE-AMPLIFIER BLOCK CHARACTERISTICS —

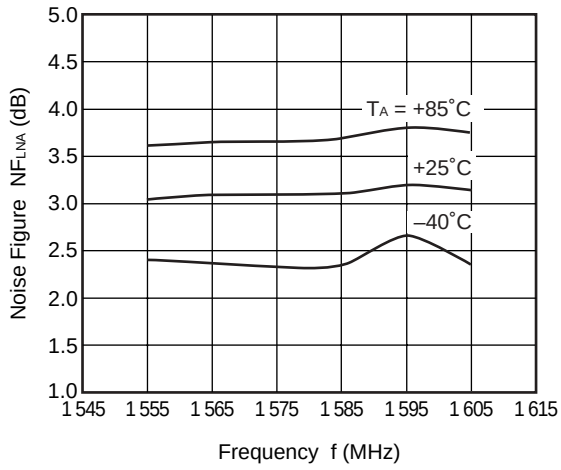
OUTPUT POWER vs. INPUT POWER



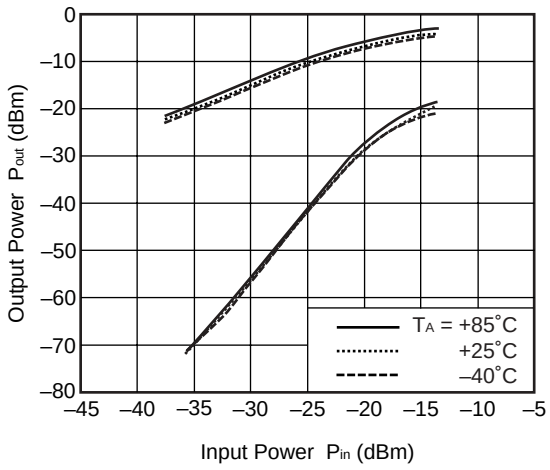
PREAMP GAIN vs. FREQUENCY



PREAMP NOISE FIGURE vs. FREQUENCY



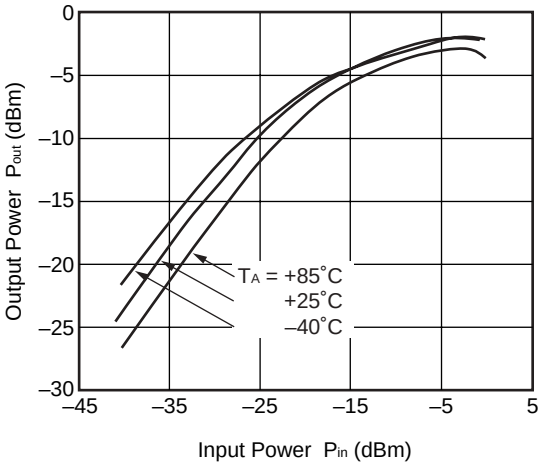
PREAMP IM CHARACTERISTICS



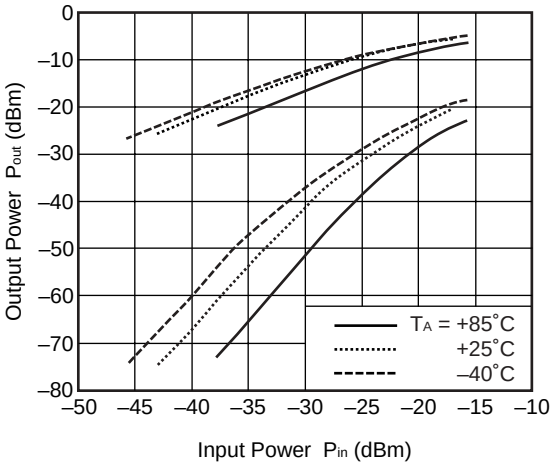
Remark The graphs indicate nominal characteristics.

— RF MIX BLOCK CHARACTERISTICS —

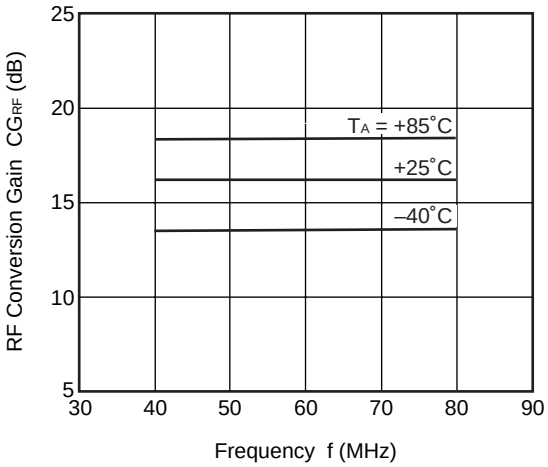
OUTPUT POWER vs. INPUT POWER



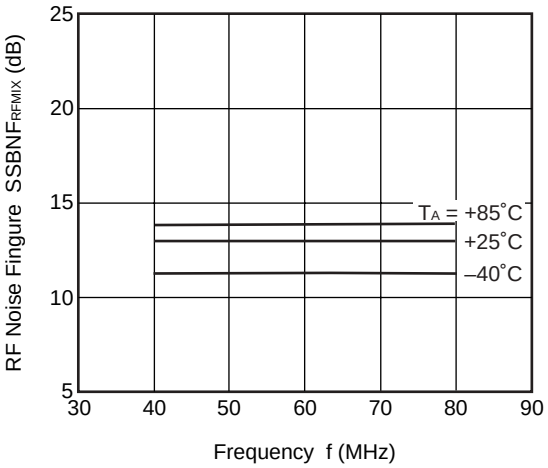
RF MIX IM CHARACTERISTICS



RF CONVERSION GAIN vs.
FREQUENCY CHARACTERISTICS



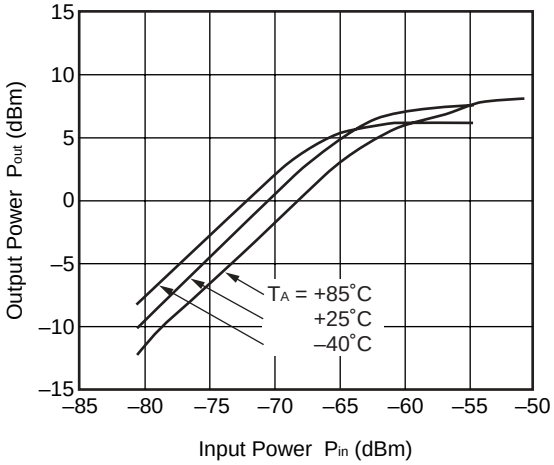
RF NOISE FIGURE vs.
FREQUENCY CHARACTERISTICS



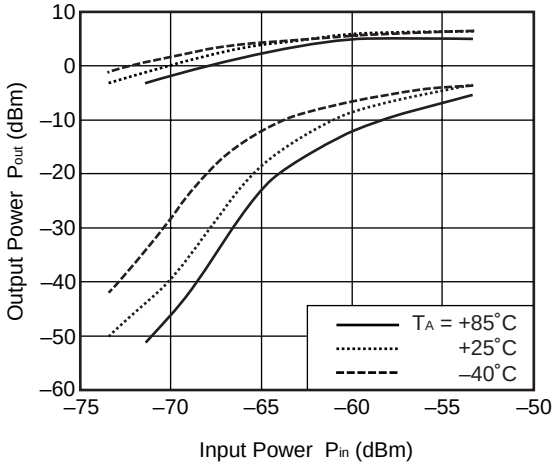
Remark The graphs indicate nominal characteristics.

— IF BLOCK CHARACTERISTICS —

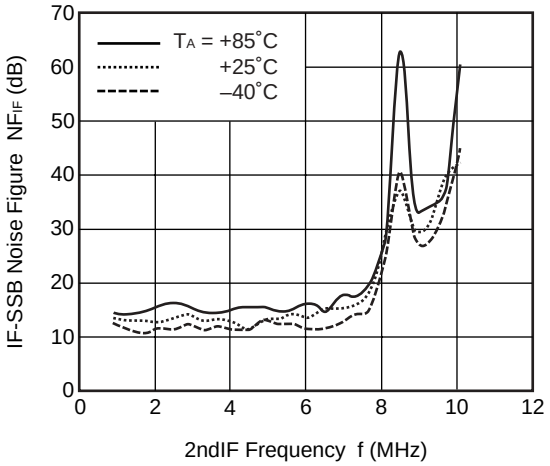
OUTPUT POWER vs. INPUT POWER



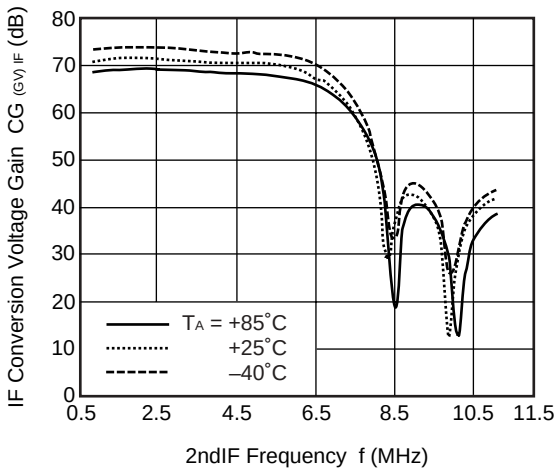
IF IM CHARACTERISTICS



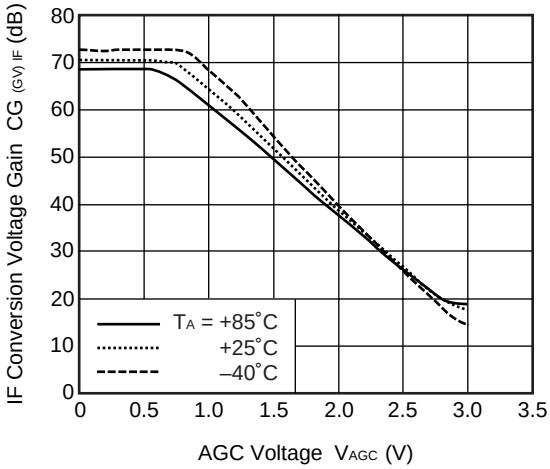
IF-SSB NOISE FIGURE vs. 2ndIF FREQUENCY



IF CONVERSION VOLTAGE GAIN vs. 2ndIF FREQUENCY



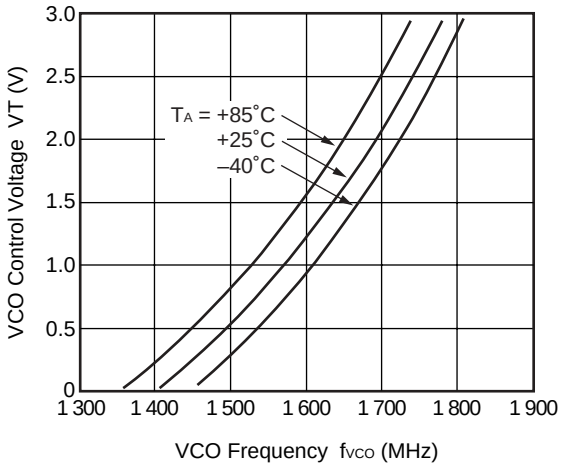
IF CONVERSION VOLTAGE GAIN vs. AGC VOLTAGE



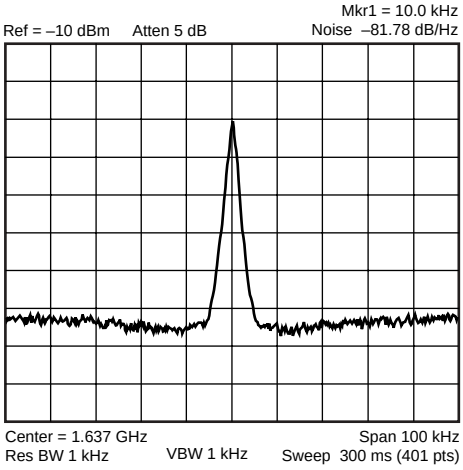
Remark The graphs indicate nominal characteristics.

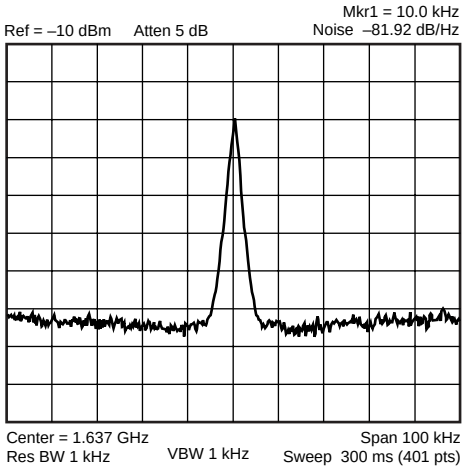
— VCO MODULATION SENSITIVITY CHARACTERISTICS —

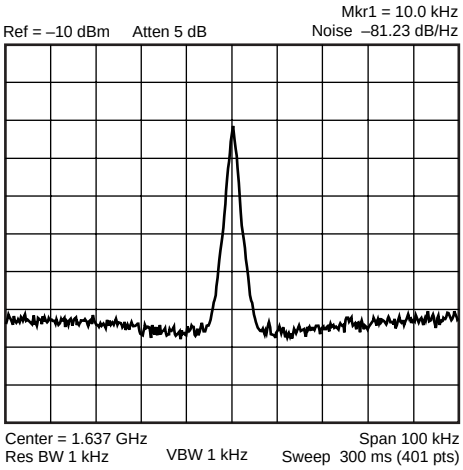
VCO CONTROL VOLTAGE vs.
VCO FREQUENCY



— C/N CHARACTERISTICS —

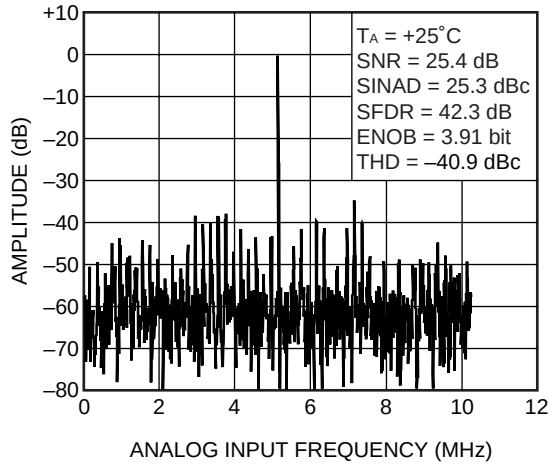


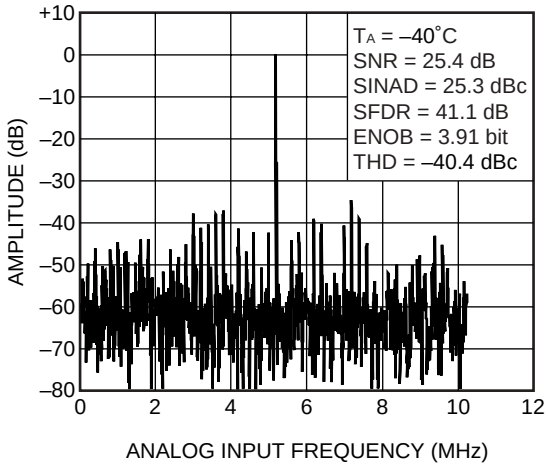


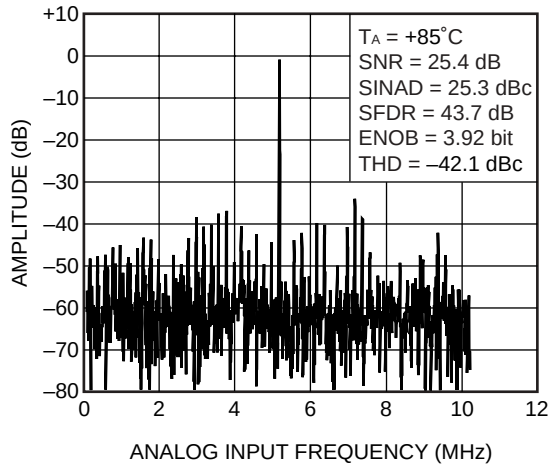


Remark The graphs indicate nominal characteristics.

— SINAD CHARACTERISTICS OF A/D CONVERTOR (IFin = 5.17 MHz, SCLKin = 20.48 MHz) —

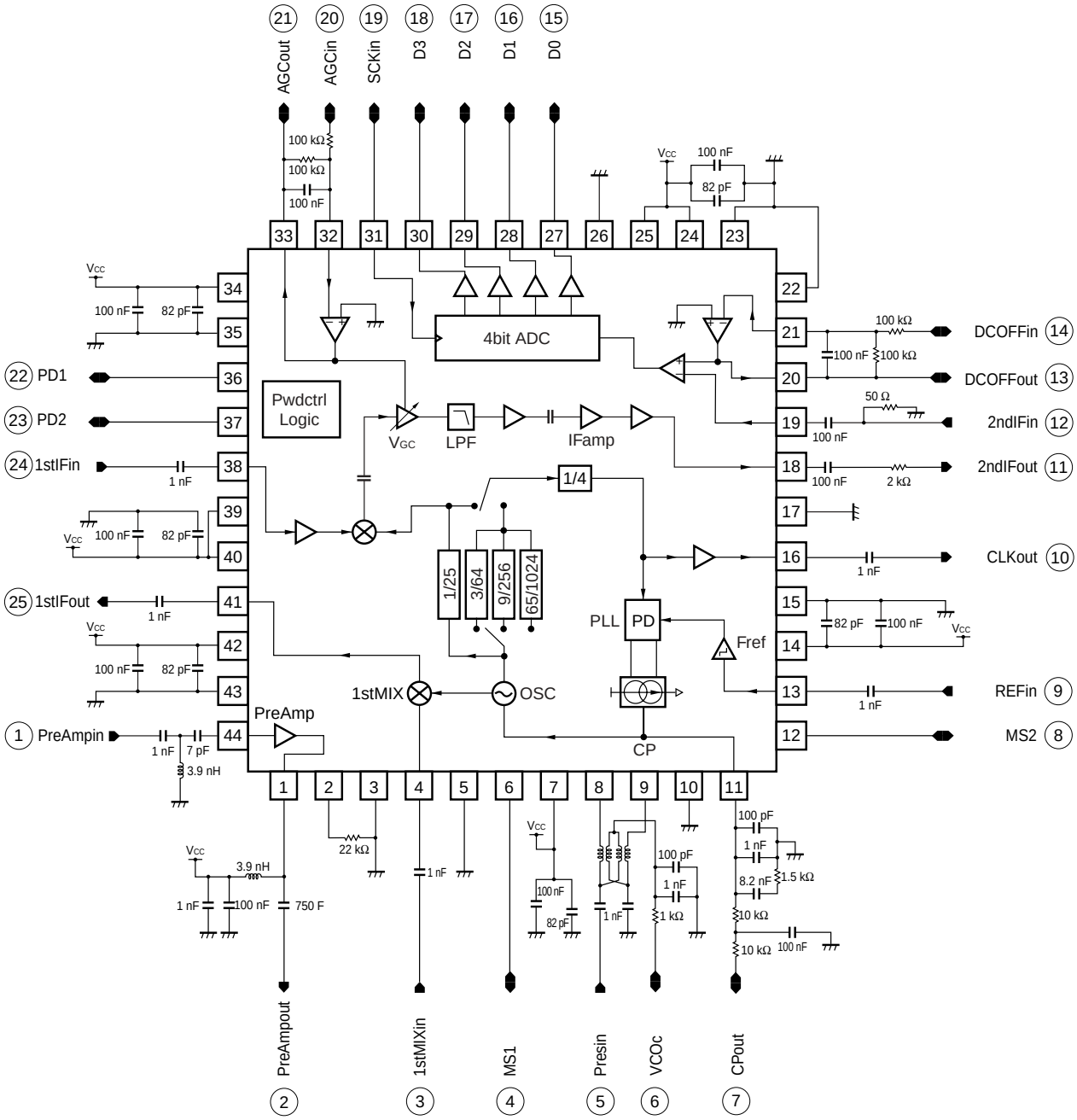






Remark The graphs indicate nominal characteristics.

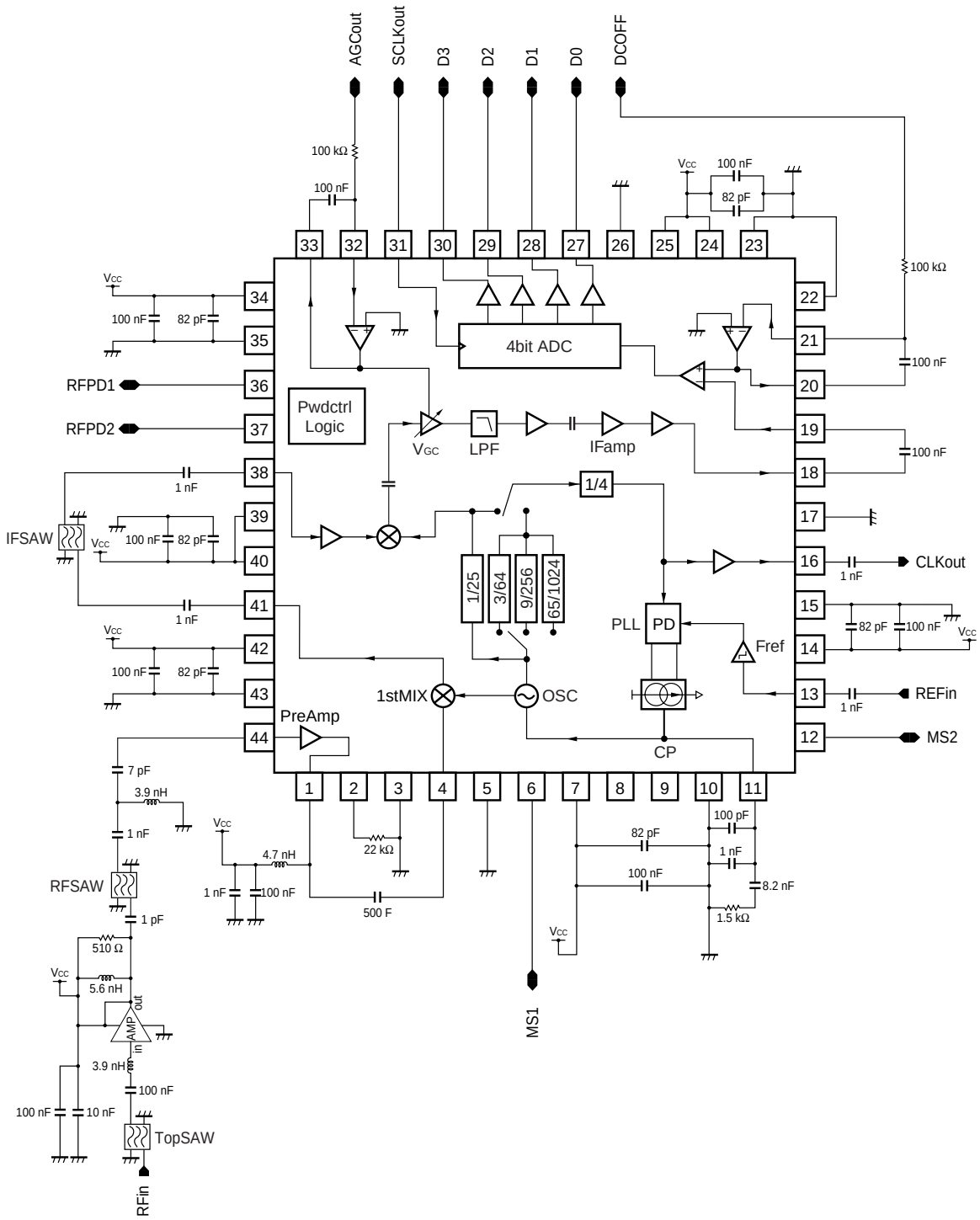
MEASUREMENT CIRCUIT



DESCRIPTION OF PINS OF TEST CIRCUIT

Pin No.	Pin Function	Pin Name	Pin No.	Pin Function	Pin Name
①	Preamplifier Input	PreAmpin	⑭	DC Offset Input	DCOFFin
②	Preamplifier Output	PreAmpout	⑮	Digital Signal Output Pin	D0
③	RF Mixer Input	1stMIXin	⑯		D1
④	MS1	MS1	⑰		D2
⑤	Prescaler Input	Presin	⑱		D3
⑥	VCO Power Control Pin	VCOc	⑲	Sampling Signal Input	SCKin
⑦	VT Measurement Pin (Charge Pump Output)	CPout	⑳	AGC Input	AGCin
⑧	MS2	MS2	㉑	AGC Control Voltage Output	AGCout
⑨	Reference Clock Input	REFin	㉒	PD1 Output (Default onboard : GND)	PD1
⑩	Clock Output	CLKout	㉓	PD1 Output (Default on board : V_{CC})	PD2
⑪	2ndIF Output	2ndIFout	㉔	1stIF Input	1stIFin
⑫	2ndIF Input	2ndIFin	㉕	1stIF Output	1stIFout
⑬	DC Offset Output	DCOFFout			

APPLICATION CIRCUIT

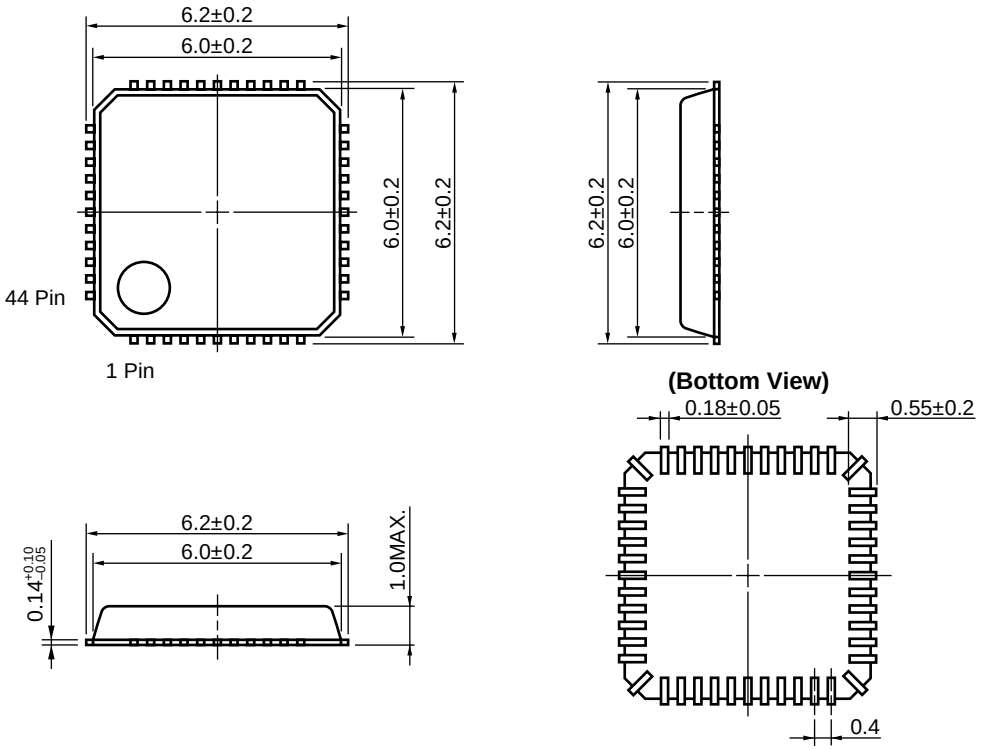


PD1	PD2	Power-down mode
0	0	Sleep mode (full off)
1	0	Warm-up mode (PLL on)
1	1	Calibration mode (PLL on)
0	1	Active mode (full on)

MS1	MS2	TCXO	N
0	0	16.368/16.384 MHz	100
0	1	19.2 MHz	256/3
1	0	14.4 MHz	1024/9
1	1	26.0 MHz	4096/65

PACKAGE DIMENSIONS

44-PIN PLASTIC QFN (UNIT: mm)



Caution The island pins located on the corners are needed to fabricate products in our plant, but do not serve any other function. Consequently the island pins should not be soldered and should remain non-connection pins.

NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent abnormal oscillation).
(3) Keep the wiring length of the ground pins as short as possible.
(4) Connect a bypass capacitor to the V_{CC} pin.
(5) High-frequency signal I/O pins must be coupled with the external circuit using a coupling capacitor.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature)	: 260°C or below	IR260
	Time at peak temperature	: 10 seconds or less	
	Time at temperature of 220°C or higher	: 60 seconds or less	
	Preheating time at 120 to 180°C	: 120±30 seconds	
	Maximum number of reflow processes	: 3 times	
	Maximum chlorine content of rosin flux (% mass)	: 0.2%(Wt.) or below	
VPS	Peak temperature (package surface temperature)	: 215°C or below	VP215
	Time at temperature of 200°C or higher	: 25 to 40 seconds	
	Preheating time at 120 to 150°C	: 30 to 60 seconds	
	Maximum number of reflow processes	: 3 times	
	Maximum chlorine content of rosin flux (% mass)	: 0.2%(Wt.) or below	
Wave Soldering	Peak temperature (molten solder temperature)	: 260°C or below	WS260
	Time at peak temperature	: 10 seconds or less	
	Preheating temperature (package surface temperature)	: 120°C or below	
	Maximum number of flow processes	: 1 time	
	Maximum chlorine content of rosin flux (% mass)	: 0.2%(Wt.) or below	
Partial Heating	Peak temperature (pin temperature)	: 350°C or below	HS350
	Soldering time (per side of device)	: 3 seconds or less	
	Maximum chlorine content of rosin flux (% mass)	: 0.2%(Wt.) or below	

Caution Do not use different soldering methods together (except for partial heating).