4096-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

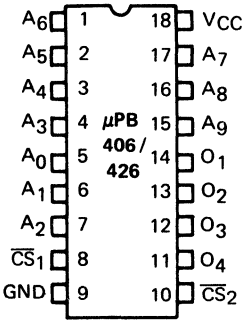
DESCRIPTION

The μPB406 and μPB426 are high-speed, electrically programmable, fully-decoded 4096-bit TTL read-only memories. On-chip address decoding, two chip-enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB406 and μPB426 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 1024 WORD X 4 BIT Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 50 ns max. (μPB406-2, μPB426-2)
- Medium Power Consumption: 500 mW TYP.
- Two Chip Select Inputs for Memory Expansion
- Open-Collector Output (μPB406)/Three-State Outputs (μPB426)
- Ceramic and Plastic 18-Lead Dual In-Line Packages
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: HPROM HM-7642/7643 type and Equivalent Devices (as a ROM)
- A.I.M. (Avalanche Induced Migration) Technology

PIN CONFIGURATION



PIN NAMES

A_0-A_9	Address Inputs
O_1-O_4	Data Outputs
$\overline{CS_1}$, $\overline{CS_2}$	Chip Selects
V_{CC}	Power (+5V)
GND	Ground

OPERATION

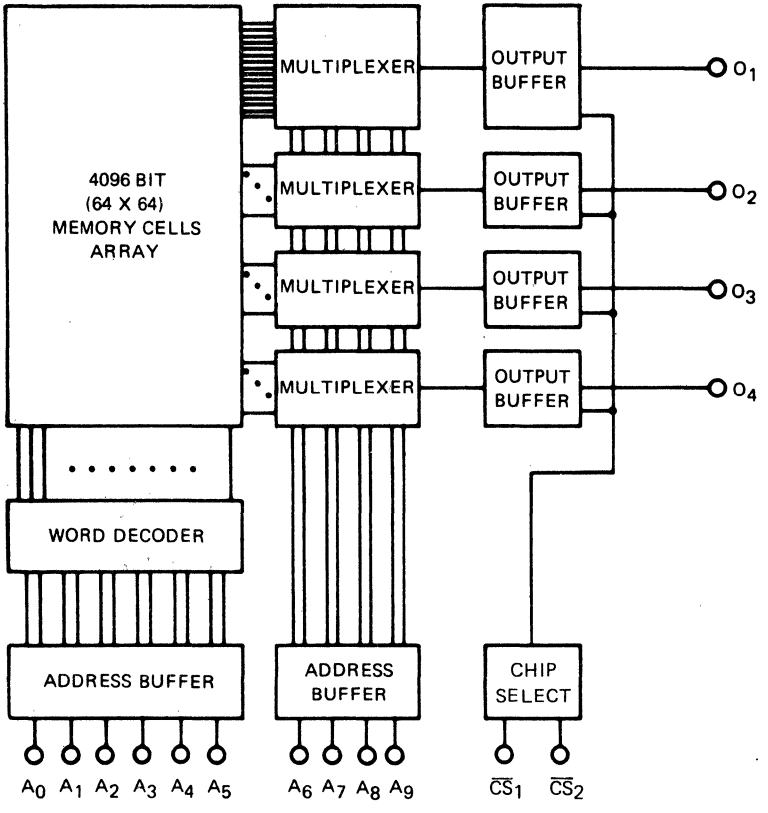
Programming

A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip select inputs must be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

To read the memory, both of the two chip select inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip select inputs are at logic one (high), all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-25°C to +75°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +5.5 Volts
All Input Voltages	-0.5 to +5.5 Volts
Supply Voltage V_{CC}	-0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB406 and μPB426. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state. Either or both of the two chip enable inputs must be at a logic one (high).

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse pass the limit. When this condition has been met, four additional pulses are applied, then the sense current is terminated.

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CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% – 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% – 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% – 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

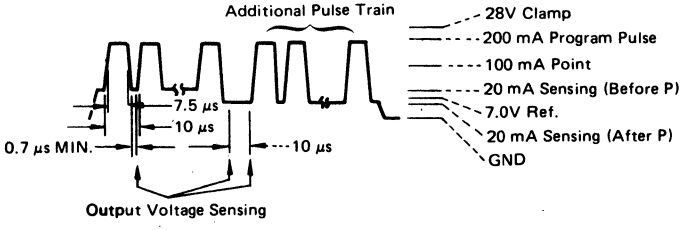

Figure 2 – Typical Output Voltage Waveform

DC CHARACTERISTICS

T_a = 0°C to +75°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IL}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$	40			μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE: ① Applicable to μPB426 only.

CAPACITANCE

T_a = 25°C, f = 1 MHz, V_{CC} = 5V, V_{IN} = 2.5V

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

AC CHARACTERISTICS

T_a = 0°C to +75°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	μPB406/426		μPB406/426-1		μPB406/426-2		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
Address Access Time	t_{AA}		70		60		50	ns	①②③④
Chip Select Access Time	t_{ACS}		45		40		30	ns	
Chip Select Disable Time	t_{DCS}		45		40		30	ns	

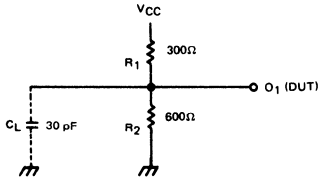

Figure 1

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

PACKAGE OUTLINE μPB406/426D

CERDIP

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01