NEC Electronics Inc.

μPB8216/26
4-BIT PARALLEL BIDIRECTIONAL BUS DRIVERS

Description

The μPB8216 and μPB8226 are 4-bit parallel bidirectional bus drivers specifically designed to buffer microcomputer system components. All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65 volts (V_{OH}); for high-capacitance terminated bus structures, the DB outputs provide a high 55 mA (I_{OL}) capability. The noninverting μPB8216 and the inverting μPB8226 bus drivers are available to meet a wide variety of applications for buffering in microcomputer systems.

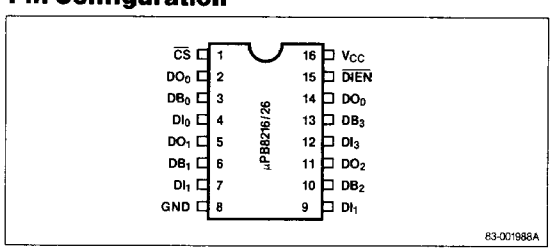
Features

- ☐ Low input load current; 0.25 mA maximum
- ☐ High output drive capability for driving system data bus
- ☐ 3.65 V output high voltage for direct interface to CPU
- ☐ Three-state outputs
- ☐ Reduces system package count

Ordering Information

Part Number	Package Type
μPB8216C	16-pin plastic DIP
μPB8226C	16-pin plastic DIP

Pin Configuration



Pin Identification

No.	Symbol	Function
1	$\overline{CS}$	Chip select input
2	DO_0	Data output, bit 0
3	DB_0	Data bus, bit 0
4	DI_0	Data input, bit 0
5	DO_1	Data output, bit 1
6	DB_1	Data bus, bit 1
7	DI_1	Data input, bit 1
8	ND	Ground
9	2	Data input, bit 2
10	2	Data bus, bit 2
11	2	Data output, bit 2
12	3	Data input, bit 3
13	B_3	Data bus, bit 3
14	O_3	Data output, bit 3
15	$\overline{DIEN}$	Data in enable
16	V_{CC}	+5 V power supply

Pin Functions

DB_0-DB_3 (Bidirectional Data Bus)

Three-state data lines that interface with the system data bus. Data direction and high impedance output are functions of the $\overline{CS}$ and $\overline{DIEN}$ control signals.

DI_0-DI_3 (Data Input)

The four data input lines receive data from the CPU and make it available to the system data bus when both $\overline{CS}$ and $\overline{DIEN}$ are active low.

DO_0-DO_3 (Data Output)

The four data output lines make data available to the CPU from the system data bus when $\overline{CS}$ is active low and $\overline{DIEN}$ is active high.

$\overline{CS}$ (Chip Select)

Chip select enables the chip's I/O capability when active low. When $\overline{CS}$ is high, the output drivers go to a high impedance state.

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$\overline{DIEN}$ (Data In Enable)

$\overline{DIEN}$ is the data flow direction control signal. When low, data on the chip's input lines (DI_0-DI_3) from the CPU is made available to the system data bus (DB_0-DB_3). When high, data on the chip's data bus lines (DB_0-DB_3) is output to the CPU (providing $\overline{CS}$ is active low enabled).

V_{CC} (Power Supply)

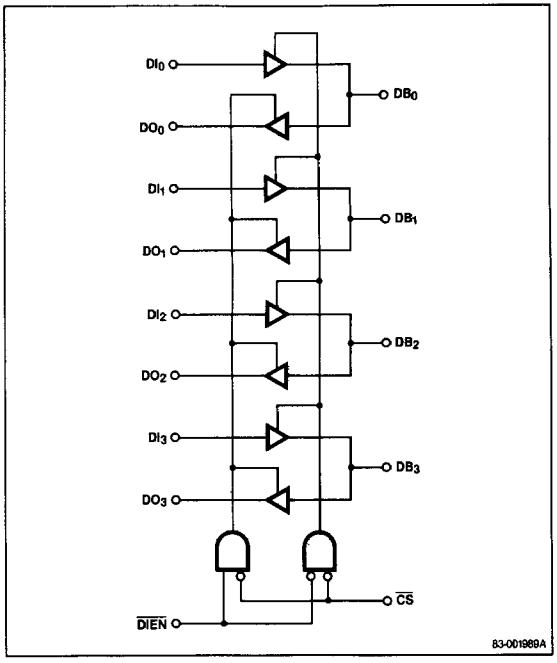
+5 V power supply input.

GND (Ground)

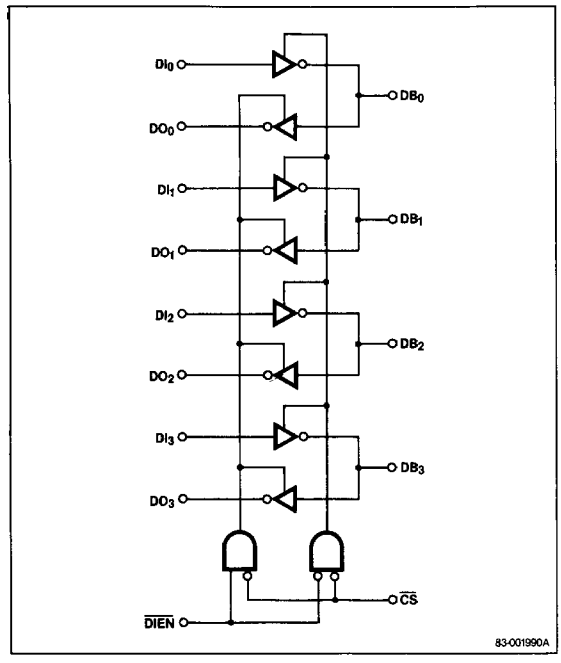
Ground.

Block Diagrams

μPB8216



μPB8226



Functional Description

Microprocessors like the μPD8080A are MOS devices and are generally capable of driving a single TTL load. This also applies to MOS memory devices. This type of drive is sufficient for small systems with a few components, but often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multiboard system.

Bidirectional Driver

Each buffered line of the μPB8216/26 4-bit driver consists of two separate buffers. They are three-state in nature to achieve direct bus interface and bidirectional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB). This is used to interface to the system side components such as memories, I/O, etc. Its interface is directly TTL-compatible and it has a high drive (55 mA). For maximum flexibility on the other side of the driver, the inputs and outputs are separate. They can be tied together so that the driver can be used to buffer a true bidirectional bus such as the 8080A data bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65 V) so that direct interface to the 8080A processor is achieved with a maximum noise level of 650 mV.

Control Gating $\overline{CS}$, $\overline{DIEN}$

The $\overline{CS}$ input is used for device selection. When $\overline{CS}$ is high, the output drivers are all forced to their high impedance state. When it is low, the device is selected (enabled) and the data flow direction is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the data flow direction (see block diagrams for complete truth table). This directional control is accomplished by forcing one of the pair of buffers to its high impedance state. This allows the other to transmit its data. This is accomplished by a simple two-gate circuit.

The μPB8216/26 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	−0.5 V to +7.0 V
Input voltage, V_I	−1.0 V to +5.5 V
Output voltage, V_O	−1.0 V to +5.5 V
Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Output current, I_O	125 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance (Note 1)

$T_A = 25°C$, $V_{CC} = 5$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			8	pF	f = 1.0 MHz
Output capacitance	C_{O1}			10(2)	pF	$V_{BIAS} = 2.5$ V
Output capacitance	C_{O2}			18(3)	pF	

Note:

(1) This parameter is not 100% tested.

(2) DO output.

(3) DB output.

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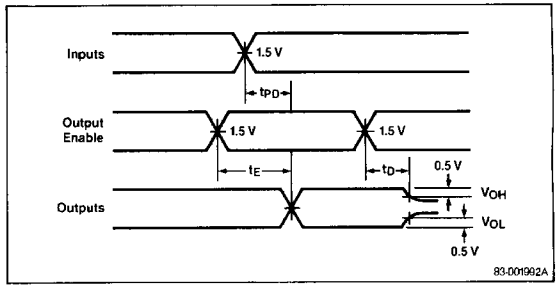
DC Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}			0.95	V	
Input voltage high	V_{IH}	2.0			V	
Output voltage low	V_{OL1}			0.48	V	DO outputs; $I_{OL} = 15$ mA
				0.48	V	DB outputs $I_{OL} = 25$ mA
	V_{OL2}			0.7	V	8216; DB outputs; $I_{OL} = 55$ mA
				0.7	V	8226; DB outputs $I_{OL} = 50$ mA
Output voltage high	V_{OH1}	3.65			V	DO outputs; $I_{OH} = -1$ mA
	V_{OH2}	2.4			V	DB outputs; $I_{OH} = -10$ mA
Input forward voltage clamp	V_C			−1.0	V	$I_C = -5$ mA
Input load current	I_{F1}			−0.5	mA	($\overline{DIEN}$, $\overline{CS}$); $V_F = 0.45$ V
	I_{F2}			−0.25	mA	(All other inputs); $V_F = 0.45$ V
Input leakage current	I_{R1}			20	μA	($\overline{DIEN}$, $\overline{CS}$); $V_R = 5.25$ V
	I_{R2}			10	μA	(DI inputs); $V_R = 5.25$ V
Output leakage current (3-state)	I_O			20	μA	DO outputs; $V_O = 0.45 / 5.25$ V
				100	μA	DB outputs
Output short circuit current	I_{OS}	−15		−65	mA	DO outputs; $V_O = 0$ V
		−30		−120	mA	DB outputs $V_{CC} = 5.0$ V
Power supply current	I_{CC}			130	mA	8216
				120	mA	8226

Timing Waveform



AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ (Note 1)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input to output delay DO outputs	t_{PD1}			25	ns	$C_L = 30$ pF, $R_1 = 300\,\Omega$, $R_2 = 600\,\Omega$, (Note 4)
Input to output delay DB outputs	t_{PD2}			30	ns	8216; $C_L = 300$ pF, $R_1 = 90\,\Omega$, $R_2 = 180\,\Omega$, (Note 4)
				25	ns	8226; $C_L = 300$ pF, $R_1 = 90\,\Omega$, $R_2 = 180\,\Omega$, (Note 4)
Output enable time	t_E			65	ns	8216; (Notes 2 & 4)
				54	ns	8226; (Notes 2 & 4)
Output disable time	t_D			35	ns	(Notes 3 & 4)

Note:

(1) Typical values are for $T_A = 25°C$, $V_{CC} = +5.0$ V.

(2) DO outputs, $C_L = 30$ pF, $R_1 = 300/10$ kΩ, $R_2 = 600/1$ kΩ
DB outputs, $C_L = 300$ pF, $R_1 = 90/10$ kΩ, $R_2 = 180/1$ kΩ.

(3) DO outputs, $C_L = 5$ pF, $R_1 = 300/10$ kΩ, $R_2 = 600/1$ kΩ
DB outputs, $C_L = 5$ pF, $R_1 = 90/10$ kΩ, $R_2 = 180/1$ kΩ.

(4) Input pulse amplitude: 2.5 V
Input rise and fall times of 5 ns between 1 and 2 V.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 V levels.

Test Load Circuit