# INPUT/OUTPUT EXPANDER FOR μPD8048/8748/8035

## DESCRIPTION

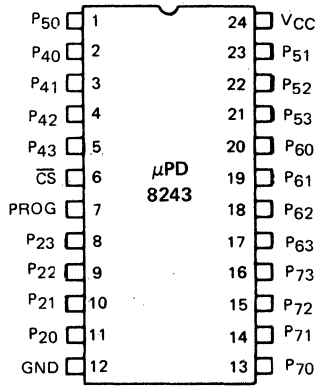
The μPD8243 input/output expander is directly compatible with the μPD8048 family of single-chip microcomputers. Using NMOS technology the μPD8243 provides high drive capabilities while requiring only a single +5V supply voltage.

The μPD8243 interfaces to the μPD8048 family through a 4-bit I/O port and offers four 4-bit bi-directional static I/O ports. The ease of expansion allows for multiple μPD8243's to be added using the bus port.

The bi-directional I/O ports of the μPD8243 act as an extension of the I/O capabilities of the μPD8048 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

## FEATURES

- Four 4-Bit I/O Ports
- Fully Compatible with μPD8048 Microcomputer Family
- High Output Drive
- NMOS Technology
- Single +5V Supply
- Direct Extension of Resident μPD8048 I/O Ports
- Logical AND and OR Directly to Ports
- Compatible with Industry Standard 8243
- Available in a 24-Pin Plastic Package




9

FUNCTIONAL DESCRIPTION

### General Operation

The I/O capabilities of the μPD8048/8748/8035 can be enhanced in four 4-bit I/O port increments using one or more μPD8243's. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND Accumulator to Port.
- Logical OR Accumulator to Port.
- Transfer Port to Accumulator.
- Transfer Accumulator to Port.

Port 2 ($P_{20}$-$P_{23}$) forms the 4-bit bus through which the μPD8243 communicates with the host processor. The PROG output from the μPD8048/8748/8035 provides the necessary timing to the μPD8243. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the op-code and port address followed by the second nibble containing the 4-bit data. Multiple μPD8243's can be used for additional I/O. The output lines from the μPD8048/8748/8035 can be used to form the chip selects for the additional μPD8243's.

### Power On Initialization

Applying power to the μPD8243 sets ports 4-7 to the tri-state mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high-to-low transition in order to exit from the power on mode. The power on sequence is initiated any time $V_{CC}$ drops below 1V. The table below shows how the 4-bit nibbles on Port 2 correspond to the μPD8243 operations.

| Port Address | | | Op-Code | | |
|---|---|---|---|---|---|
| $P_{21}$ | $P_{20}$ | Address Code | $P_{23}$ | $P_{22}$ | Instruction Code |
| 0 | 0 | Port 4 | 0 | 0 | Read |
| 0 | 1 | Port 5 | 0 | 1 | Write |
| 1 | 0 | Port 6 | 1 | 0 | ORLD |
| 1 | 1 | Port 7 | 1 | 1 | ANLD |

For example an 0010 appearing on $P_{20}$-$P_{23}$, respectively, would result in a Write to Port 4.

### Read Mode

There is one Read mode in the μPD8243. A falling edge on the PROG pin latches the op-code and port address from input Port 2. The port address and Read operation are then decoded causing the appropriate outputs to be tri-stated and the input buffers switched on. The rising edge of PROG terminates the Read operation. The Port (4,5,6, or 7) that was selected by the Port address ($P_{21}$-$P_{20}$) is returned to the tri-state mode, and Port 2 is switched to the input mode.

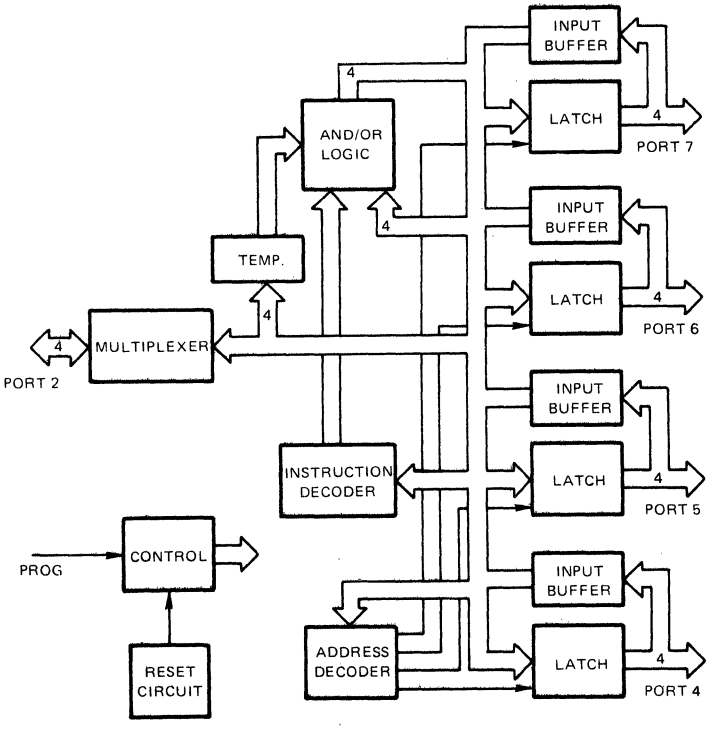
Generally, in the read mode, a port will be an input and in the write mode it will be an output. If during program operation, the μPD8243's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

### Write Modes

There are three write modes in the μPD8243. The MOVD $P_p$,A instruction from the μPD8048/8748/8035 writes the new data directly to the specified port (4,5,6, or 7). The old data previously latched at that port is lost. The ORLD Pp,A instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD Pp,A instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.

## BLOCK DIAGRAM




## PIN IDENTIFICATION

| PIN NO. | PIN SYMBOL | FUNCTION |
|---|---|---|
| 2-5<br>1, 21-23<br>17-20<br>13-16 | $P_{40}$-$P_{43}$<br>$P_{50}$-$P_{53}$<br>$P_{60}$-$P_{63}$<br>$P_{70}$-$P_{73}$ | The four 4-bit static bi-directional I/O ports. They are programmable into the following modes: input mode (during a Read operation); low impedance latched output mode (after a Write operation); and the tri-state mode (following a Read operation). Data appearing on I/O lines $P_{20}$-$P_{23}$ can be written directly. That data can also be logically ANDed or ORed with the previous data on those lines. |
| 6 | $\overline{CS}$ | Chip Select input (active-low). When the μPD8343 is deselected ($\overline{CS}$ = 1), output or internal status changes are inhibited. |
| 7 | PROG | Clock input pin. The control and address information are present on port lines $P_{20}$-$P_{23}$ when PROG makes a high-to-low transition. Data is present on port lines $P_{20}$-$P_{23}$ when PROG makes a low-to-high transition. |
| 8-11 | $P_{20}$-$P_{23}$ | $P_{20}$-$P_{23}$ form a 4-bit bi-directional port. Refer to PROG function for contents of $P_{20}$-$P_{23}$ at the rising and falling edges of PROG. Data from a selected port is present on $P_{20}$-$P_{23}$ prior to the rising edge of PROG if during a Read operation. |
| 12 | GND | The μPD8041/8741 ground potential. |
| 24 | $V_{CC}$ | +5 volt supply. |

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Operating Temperature | 0°C to +70°C |
| Storage Temperature (Ceramic Package) | −65°C to +150°C |
| Storage Temperature (Plastic Package) | −65°C to +125°C |
| Voltage on Any Pin | − 0.5 to +7 Volts ① |
| Power Dissipation | 1 W |

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*$T_a$ = 25°C

## DC CHARACTERISTICS

$T_a$ = 0°C to +70°C; $V_{CC}$ = +5V ± 5%

| PARAMETER | SYMBOL | LIMITS MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | −0.5 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ + 0.5 | V | |
| Output Low Voltage (Ports 4-7) | $V_{OL1}$ | | | 0.45 | V | $I_{OL}$ = 5 mA ① |
| Output Low Voltage (Port 7) | $V_{OL2}$ | | | 1 | V | $I_{OL}$ = 20 mA |
| Output Low Voltage (Port 2) | $V_{OL3}$ | | | 0.45 | V | $I_{OL}$ = 0.6 mA |
| Output High Voltage (Ports 4-7) | $V_{OH1}$ | 2.4 | | | V | $I_{OH}$ = 240 μA |
| Output High Voltage (Port 2) | $V_{OH2}$ | 2.4 | | | V | $I_{OH}$ = 100 μA |
| Sum of All $I_{OL}$ From 16 Outputs | $I_{OL}$ | | | 100 | mA | 5 mA Each Pin |
| Input Leakage Current (Ports 4-7) | $I_{IL1}$ | −10 | | 20 | μA | $V_{IN}$ = $V_{CC}$ to 0V |
| Input Leakage Current (Port 2, $\overline{CS}$, PROG) | $I_{IL2}$ | −10 | | 10 | μA | $V_{IN}$ = $V_{CC}$ to 0V |
| $V_{CC}$ Supply Current | $I_{CC}$ | | 10 | 20 | mA | |

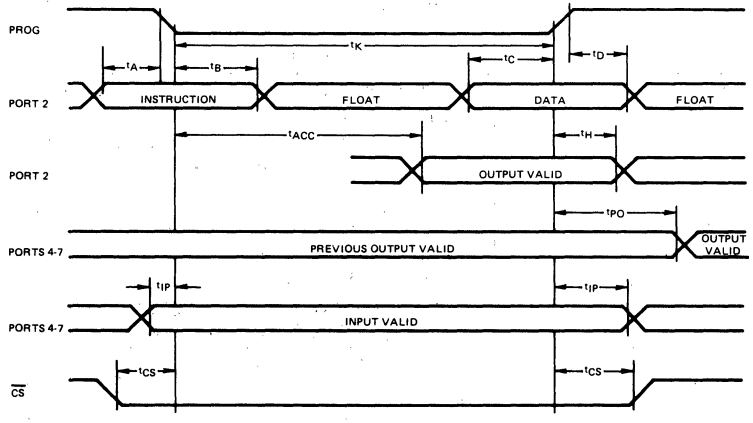
**Note:** ① Refer to graph of additional sink current drive.

## AC CHARACTERISTICS

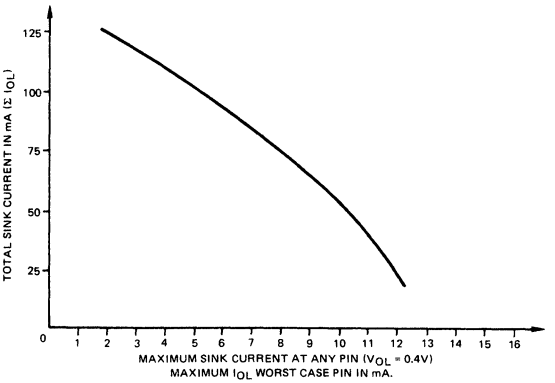
$T_a$ = 0°C to +70°C; $V_{CC}$ = +5V ± 5%

| PARAMETER | SYMBOL | LIMITS MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Code Valid Before PROG | $t_A$ | 100 | | | ns | 80 pF Load |
| Code Valid After PROG | $t_B$ | 60 | | | ns | 20 pF Load |
| Data Valid Before PROG | $t_C$ | 200 | | | ns | 80 pF Load |
| Data Valid After PROG | $t_D$ | 20 | | | ns | 20 pF Load |
| Port 2 Floating After PROG | $t_H$ | 0 | | 150 | ns | 20 pF Load |
| PROG Negative Pulse Width | $t_K$ | 900 | | | ns | |
| Ports 4-7 Valid After PROG | $t_{PO}$ | | | 700 | ns | 100 pF Load |
| Ports 4-7 Valid Before/After PROG | $t_{LP1}$ | 100 | | | ns | |
| Port 2 Valid After PROG | $t_{ACC}$ | | | 750 | ns | 80 pF Load |
| $\overline{CS}$ Valid Before/After PROG | $t_{\overline{CS}}$ | 50 | | | ns | |

## TIMING WAVEFORMS

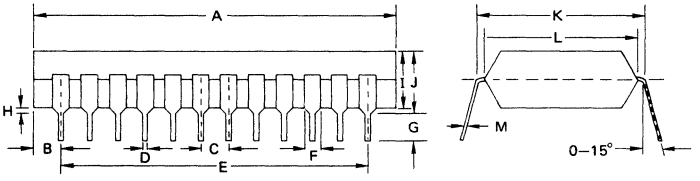


## CURRENT SINKING CAPABILITY ①




**Note:** ① This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins. The μPD8243 is capable of sinking 5 mA (for $V_{OL}$ = 0.4V) through each of the 16 I/O lines simultaneously. The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded.

## PACKAGE OUTLINES μPD8243C




**(PLASTIC)**

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 33 MAX | 1.3 MAX |
| B | 2.53 | 0.1 |
| C | 2.54 | 0.1 |
| D | 0.5 ± 0.1 | 0.02 ± 0.004 |
| E | 27.94 | 1.1 |
| F | 1.5 | 0.059 |
| G | 2.54 MIN | 0.1 MIN |
| H | 0.5 MIN | 0.02 MIN |
| I | 5.22 MAX | 0.205 MAX |
| J | 5.72 MAX | 0.225 MAX |
| K | 15.24 | 0.6 |
| L | 13.2 | 0.52 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.01^{+0.004}_{-0.0019}$ |

9