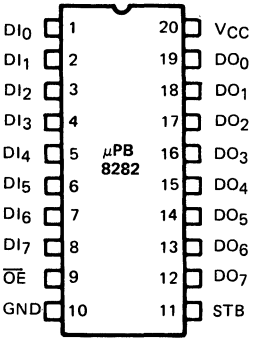
OCTAL LATCH

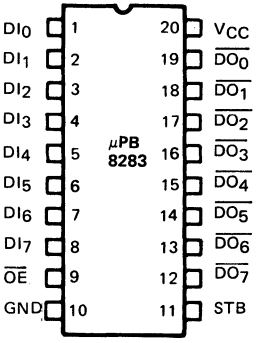
DESCRIPTION

The μPB8282/8283 are 8-bit latches with tri-state output buffers. The 8282 is non-inverting and the 8283 inverts the input data. These devices are ideal for demuxing the address/data buses on the 8085A/8086 microprocessors.
The 8282/8283 are fabricated using NEC's Schottky bipolar process.

FEATURES

- Supports 8080, 8085A, 8048, 8086 Family Systems
- Transparent During Active Strobe
- Fully Parallel 8-Bit Data Register and Buffer
- High Output Drive Capability (32 mA) for Driving the System Data Bus
- Tri-State Outputs
- 20-Pin Package





PIN NAMES

DI_0-DI_7	DATA IN
$DO_0$$DO_7$	DATA OUT
$\overline{OE}$	OUTPUT ENABLE
STB	STROBE

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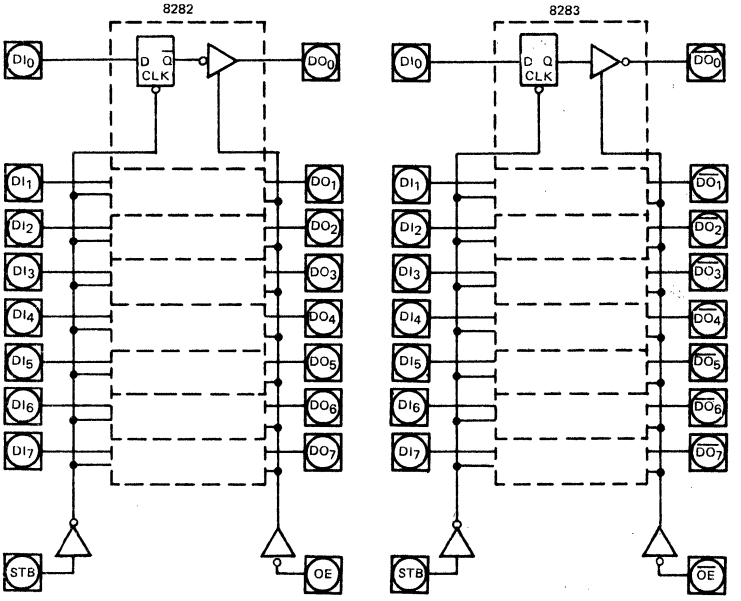
FUNCTIONAL DESCRIPTION

The μPB8282/8283 are 8-bit latches with tri-state output buffers. Data on the inputs is latched into the data latches on a high to low transition of the STB line. When STB is high, the latches appear transparent. The OE input enables the latched data to be transferred to the output pins. When OE is high, the outputs are put in the tri-state condition. OE will not cause transients to appear on the data outputs.

μPB8282/8283

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to 5.5V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

Conditions: V_{CC} = 5V ± 5%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Clamp Voltage	V_C		−1	V	I_C = −5 mA
Power Supply Current	I_{CC}		160	mA	
Forward Input Current	I_F		−0.2	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = 5.25V
Output Low Voltage	V_{OL}		0.50	V	I_{OL} = 32 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −5 mA
Output Off Current	I_{OFF}		±50	μA	V_{OFF} = 0.45 to 5.25V
Input Low Voltage	V_{IL}		0.8	V	V_{CC}=5.0V①
Input High Voltage	V_{IH}	2.0		V	V_{CC}=5.0V① F=1 MHz
Input Capacitance	C_{IN}		12	pF	V_{BIAS}=2.5V, V_{CC}=5V T_a=25°C

Notes: ① Output Loading I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

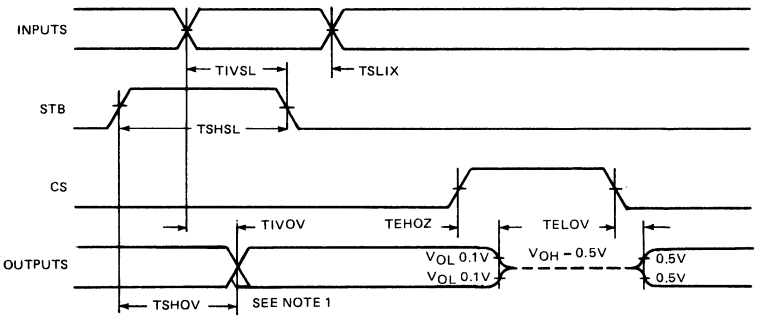
AC CHARACTERISTICS

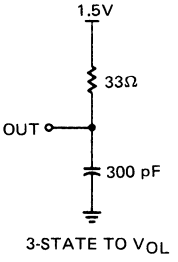
Conditions: V_{CC} = 5V ± 5%, T_a = 0°C to 70°C

Loading: Outputs – I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

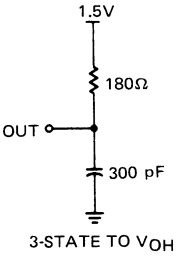
PARAMETER	SYMBOL	MIN	MAX	UNITS
Input to Output Delay	TIVOV			
—Inverting			25	ns
—Non-Inverting			35	ns
STB to Output Delay	TSHOV			
—Inverting			45	ns
—Non-Inverting			55	ns
Output Disable Time	TEHOZ		25	ns
Output Enable Time	TELOV	10	50	ns
Input to STB Setup Time	TIVSL	0		ns
Input to STB Hold Time	TSLIX	25		ns
STB High Time	TSHSL	15		ns

TIMING WAVEFORMS

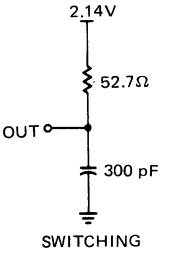




3-STATE TO V_{OL}



3-STATE TO V_{OH}



SWITCHING

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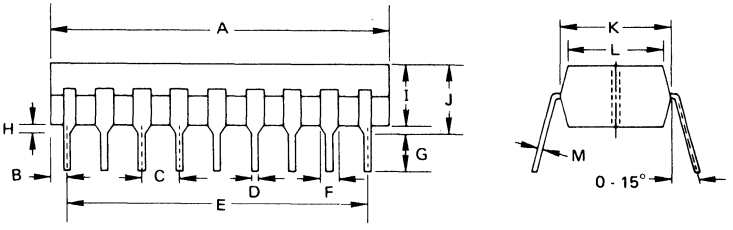
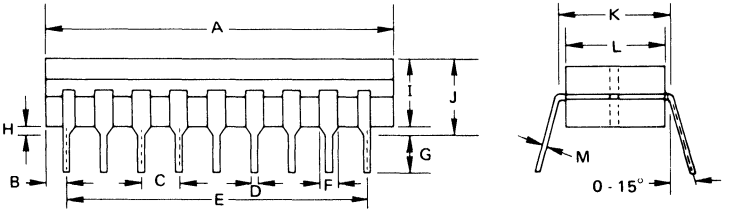
PACKAGE OUTLINES
μPB8282C
μPB8283C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPB8282D
μPB8283D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01