CLOCK GENERATOR AND DRIVER FOR 8086/8088 MICROPROCESSORS

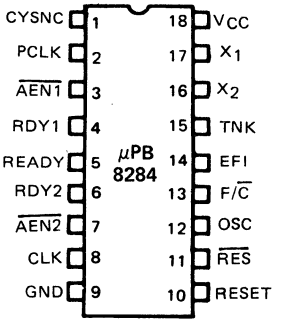
DESCRIPTION

The μPB8284 is a clock generator and driver for the 8086 and 8088 microprocessors This bipolar driver provides the microprocessor with a reset signal and also provides properly synchronized READY timing. A TTL clock is also provided for peripheral devices.

FEATURES

- Generate System Clock for the 8086 and 8088
- Frequency Source can be a Crystal or a TTL Signal
- MOS Level Output for the Processor
- TTL Level Output for Peripheral Devices
- Power-Up Reset for the Processor
- READY Synchronization
- +5V Supply
- 18 Pin Package

PIN CONFIGURATION



PIN NAMES

X_1, X_2	Crystal Connections
TANK	For Overtone Crystal
F/$\overline{C}$	Clock Source Select
EFI	External Clock Input
CSYNC	Clock Synchronization Input
RDY1, RDY2	Ready Signal from Multibus™* Systems
$\overline{AEN1}$, $\overline{AEN2}$	Address Enable Qualifiers for the two RDY Signals
$\overline{RES}$	Reset Input
RESET	Synchronized Reset Output
OSC	Oscillator Output
CLK	MOS Clock for the Processor
PCLK	TTL Clock for Peripherals
READY	Synchronized Ready Output

*TM - Multibus is a trademark of Intel Corporation.

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PIN IDENTIFICATION

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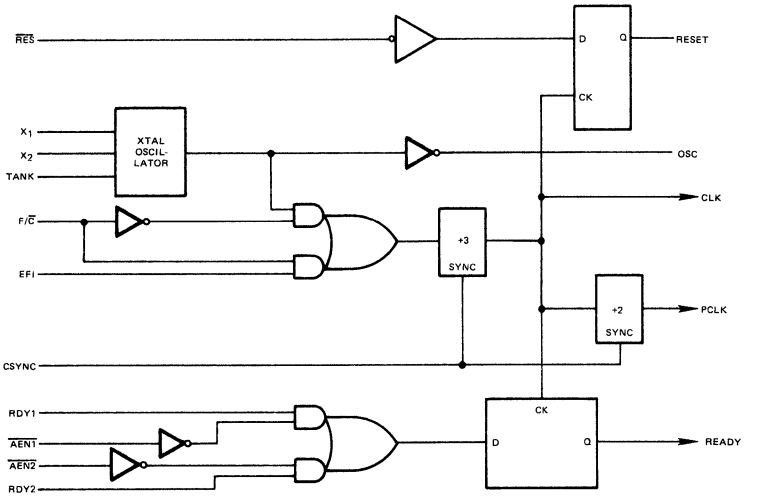
NO.	SYMBOL	NAME	FUNCTION
1	CSYNC	Clock Synchronization	An active high signal which allows multiple 8284s to be synchronized. When CYSNC is low, the internal counters count and when high the counters are reset. CYSNC should be grounded when the internal oscillator is used.
2	PCLK	Peripheral Clock	A TTL level clock for use with peripheral devices. This clock is one-half the frequency of CLK.
3, 7	$\overline{AEN}1$, $\overline{AEN}2$	Address Enable	This active low signal is used to qualify its respective RDY inputs. If there is only one bus to interface to, $\overline{AEN}$ inputs are to be grounded.
4, 6	RDY1, RDY2	Bus Ready	This signal is sent to the 8284 from a peripheral device on the bus to indicate that data has been received or data is available to be read.
5	READY	Ready	The READY signal to the microprocessor is synchronized by the RDY inputs to the processor CLK. READY is cleared after the guaranteed hold time to the processor has been met.
8	CLK	Processor Clock	This is the MOS level clock output of 33% duty cycle to drive the microprocessor and bipolar support devices (8288) connected to the processor. The frequency of CLK is one third of the crystal or EFI frequency.
10	RESET	Reset	This is used to initialize the processor. Its input is derived from an RC connection to a Schmitt trigger input for power up operation.
11	$\overline{RES}$	Reset In	This Schmitt trigger input is used to determine the timing of RESET out via an RC circuit.
12	OSC	Oscillator Output	This TTL level clock is the output of the oscillator circuit running at the crystal frequency.
13	F/$\overline{C}$	Frequency Crystal Select	F/$\overline{C}$ is a strapping option used to determine where CLK is generated. A low is for the EFI input, and a high is for the crystal.
14	EFI	External Frequency In	A square wave in at three times the CLK output. A TTL level clock to generate CLK.
16, 17	X_1, X_2	Crystal In	A crystal is connected to these inputs to generate the processor clock. The crystal chosen is three times the desired CLK output.
15	TNK	Tank	This is used for overtone type crystals. (See diagram below.)
18	VCC	VCC	+5V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

Conditions: T_a = 0°C to 70°C; V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Forward Input Current	I_F		-0.5	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C		-1.0	V	I_C = -5 mA
Power Supply Current	I_{CC}		140	mA	
Input Low Voltage	V_{IL}		0.8	V	V_{CC} = 5.0V
Input High Voltage	V_{IH}	2.0		V	V_{CC} = 5.0V
Reset Input High Voltage	V_{IHR}	2.6		V	V_{CC} = 5.0V
Output Low Voltage	V_{OL}		0.45	V	5 mA = I_{OL}
Output High Voltage CLK Other Outputs	V_{OH}	4 2.4		V V	-1 mA -1 mA } I_{OH}
$\overline{RES}$ Input Hysteresis	V_{IHR}-V_{ILR}	0.25		V	V_{CC} = 5.0V

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FUNCTIONAL DESCRIPTION

The clock generator can provide the system clock from either a crystal or an external TTL source. There is an internal divide by three counter which receives its input from either the crystal or TTL source (EFI Pin) depending on the state of the F/$\overline{C}$ input strapping. There is also a clear input (C SYNC) which is used for either inhibiting the clock, or synchronizing it with an external event (or perhaps another clock generator chip). Note that if the TTL input is used, the crystal oscillator section can still be used for an independent clock source, using the OSC output.

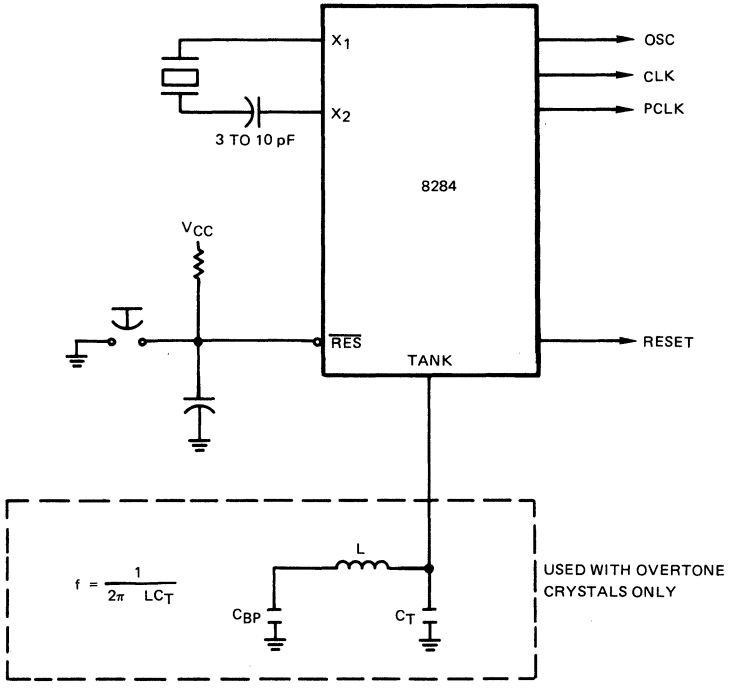
For driving the MOS output level, there is a 33% duty cycle MOS output (CLK) for the microprocessor, and a TTL output (PCLK) with a 50% duty cycle for use as a peripheral clock signal. This clock is at one half of the processor clock speed.

Reset timing is provided by a Schmitt Trigger input ($\overline{RES}$) and a flip-flop to synchronize the reset timing to the falling edge of CLK. Power-on reset is provided by a simple RC circuit on the $\overline{RES}$ input.

There are two READY inputs, each with its own qualifier ($\overline{AEN1}$, $\overline{AEN2}$). The unused $\overline{AEN}$ signal should be tied low.

The READY logic in the 8284 synchronizes the RDY1 and RDY2 asynchronous inputs to the processor clock to insure proper set up time, and to guarantee proper hold time before clearing the ready signal.

TANK INSERT CIRCUIT DIAGRAM



The tank input to the oscillator allows the use of overtone mode crystals. The tank circuit shunts the crystal's fundamental and high overtone frequencies and allows the third harmonic to oscillate. The external LC network is connected to the TANK input and is AC coupled to ground.

AC CHARACTERISTICS

Conditions: $T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

TIMING REQUIREMENTS

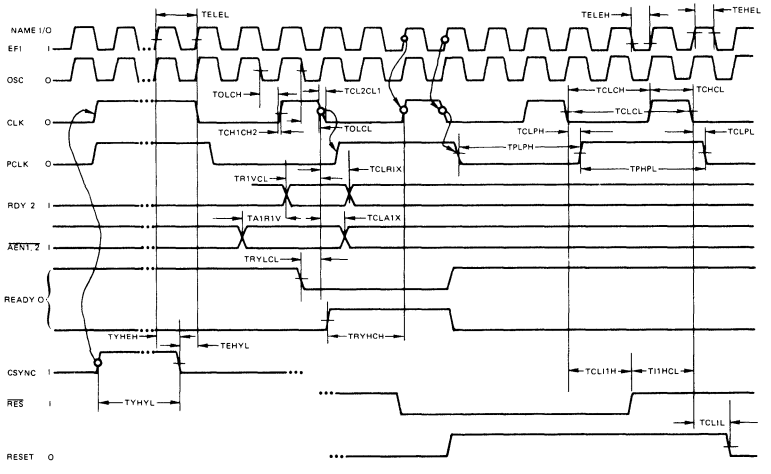
PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
External Frequency High Time	TEHEL	20		ns	90%-90% V_{IN}
External Frequency Low Time	TELEH	20		ns	10%-10% V_{IN}
EFI Period	TELEL	TEHEL + TELEH + δ		ns	①
XTAL Frequency		12	25	MHz	
RDY1, RDY2 Set-Up to CLK	TR1VCL	35		ns	
RDY1, RDY2 Hold to CLK	TCLR1X	0		ns	
AEN1, AEN2 Set-Up to RDY1, RDY2	TA1VR1V	15		ns	
AEN1, AEN2 Hold to CLK	TCLA1X	0		ns	
CSYNC Set-Up to EFI	TYHEH	20		ns	
CSYNC Hold to EFI	TEHYL	20		ns	
CSYNC Width	TYHYL	2 TELEL		ns	
RES Set-Up to CLK	TI1HCL	65		ns	②
RES Hold to CLK	TCLI1H	20		ns	②

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
CLK Cycle Period	TCLCL	125		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2.0		ns	Figure 3 and Figure 4
CLK Low Time	TCLCH	(2/3 TCLCL) −15.0		ns	Figure 3 and Figure 4
CLK Rise and Fall Time	TCH1CH2 TCL2CL1		10	ns	1.0V to 3.5V
PCLK High Time	TPHPL	TCLCL −20		ns	
PCLK Low Time	TPLPH	TCLCL −20		ns	
Ready Inactive to CLK ④	TRYLCL	−8		ns	Figure 5 and Figure 6
Ready Active to CLK ③	TRYHCH	(2/3 TCLCL) −15.0		ns	Figure 5 and Figure 6
CLK To Reset Delay	TCLIL		40	ns	
CLK to PCLK High Delay	TCLPH		22	ns	
CLK to PCLK Low Delay	TCLPL		22	ns	
OSC to CLK High Delay	TOLCH	−5	12	ns	
OSC to CLK Low Delay	TOLCL	2	20	ns	

Notes: ① δ = EFI rise (5 ns max) + EFI fall (5 ns max).
② Set up and hold only necessary to guarantee recognition at next clock.
③ Applies only to T3 and TW states.
④ Applies only to T2 states.

TIMING WAVEFORMS*



*ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

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AC TEST CIRCUITS

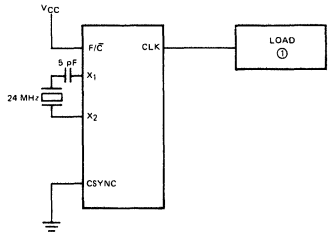


FIGURE 1
CLOCK HIGH AND LOW TIME

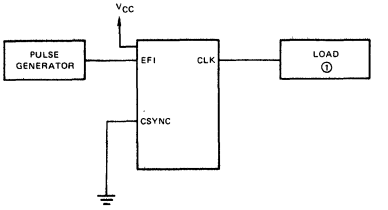


FIGURE 2
CLOCK HIGH AND LOW TIME

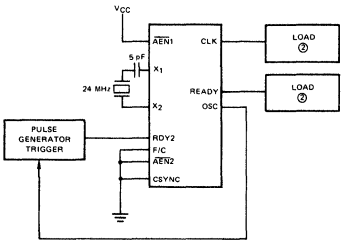


FIGURE 3
READY TO CLK

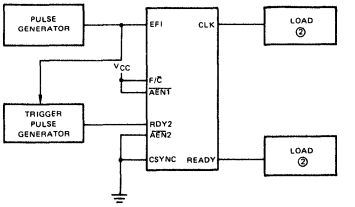
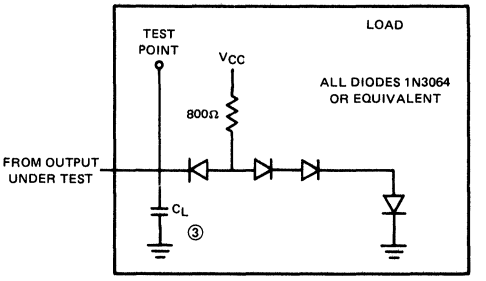


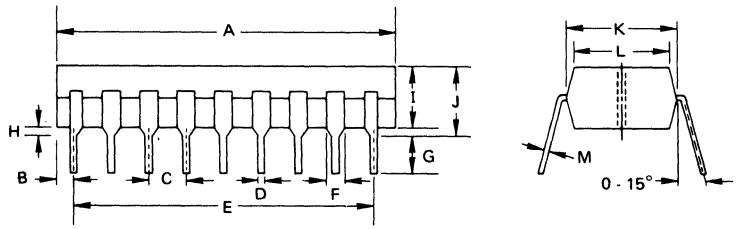
FIGURE 4
READY TO CLK



OUTPUT

NOTES: ① C_L = 100 pF
② C_L = 30 pF
③ C_L INCLUDES PROBE AND JIG CAPACITANCE

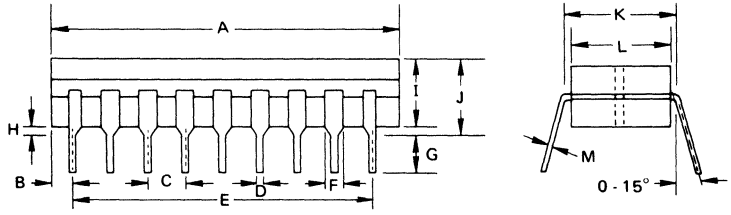
PACKAGE OUTLINES
μPB8284C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPB8284D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

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