8-BIT BUS TRANSCEIVER

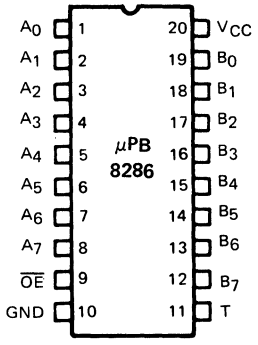
DESCRIPTION

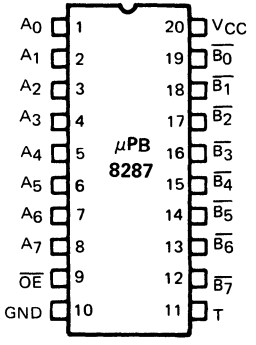
The 8286 and 8287 are octal bus transceivers used for buffering microprocessor bus lines. Being bi-directional, they are ideal for buffering the data bus lines on 8 or 16 bit microprocessors. Each B output is capable of driving 32 mA low or 5 mA high.

FEATURES

- Data Bus Buffer Driver for μCOM-8 (8080, 8085A, 780) and μCOM-16 (8086) families
- Low Input Load Current — 0.2 mA max.
- High Output Drive Capability for Driving System Data Bus
- Tri-State Outputs
- 20 Pin Package with Fully Parallel 8-Bit Transceivers

PIN CONFIGURATIONS





PIN NAMES

A_0-A_7	Local Bus Data
B_0-B_7	System Bus Data
OE	Output Enable
T	Transmit

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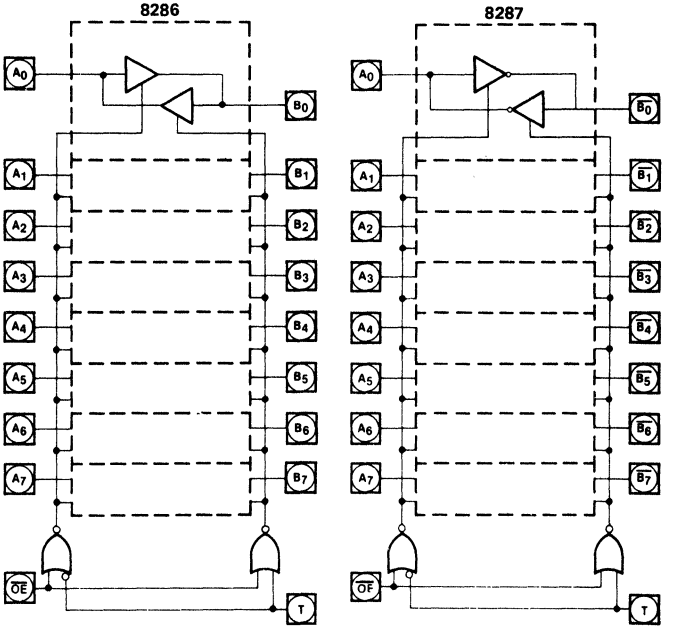
BLOCK DIAGRAMS



$\overline{OE}$	T	RESULT
0	0	B → A
0	1	A → B
1	0	A and B HIGH IMPEDANCE
1	1	A and B HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Power Dissipation . . . . . 1 W

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER		SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Clamp Voltage		V_C		−1	V	I_C = −5 mA
Power Supply Current	− 8287	I_{CC}		130	mA	
	− 8286	I_{CC}		160	mA	
Forward Input Current		I_F		−0.2	mA	V_F = 0.45V
Reverse Input Current		I_R		50	μA	V_R = 5.25V
Output Low Voltage	− B Outputs	V_{OL}		0.5	V	I_{OL} = 32 mA
	− A Outputs			0.5	V	I_{OL} = 10 mA
Output High Voltage	− B Outputs	V_{OH}	2.4		V	I_{OH} = −5 mA
	− A Outputs		2.4		V	I_{OH} = −1 mA
Output Off Current		I_{OFF}		I_F		V_{OFF} = 0.45V
Output Off Current		I_{OFF}		I_R		V_{OFF} = 5.25V
Input Low Voltage	− A Side	V_{IL}		0.8	V	V_{CC} = 5.0V ①
	− B Side	V_{IL}		0.9	V	V_{CC} = 5.0V ①
Input High Voltage		V_{IH}	2.0		V	V_{CC} = 5.0V ① F = 1 MHz
Input Capacitance	− A Side	C_{IN}		16	pF	V_{BIAS} = 2.5V, V_{CC} = 5V
	− B Side			22		T_a = 25°C

Note: ① B Outputs − I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
A Outputs − I_{OL} = 10 mA, I_{OH} = −1 mA, C_L = 100 pF

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I		5	8	pF	V_I = 0V
Output Capacitance	C_O		8	12	pF	V_O = 0V

AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

SYMBOL	PARAMETER	MIN	MAX	UNITS
TIVOV	Input to Output Delay			
	Inverting		25	ns
	Non-Inverting		35	ns
TEHTV	Transmit/Receive Hold Time	TEHOZ		ns
TTVEL	Transmit/Receive Setup	30		ns
TEHOZ	Output Disable Time		25	ns
TELOV	Output Enable Time	10	50	ns

Notes: See waveforms and test load circuit.
B Outputs − I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
A Outputs − I_{OL} = 10 mA, I_{OH} = −1 mA, C_L = 100 pF

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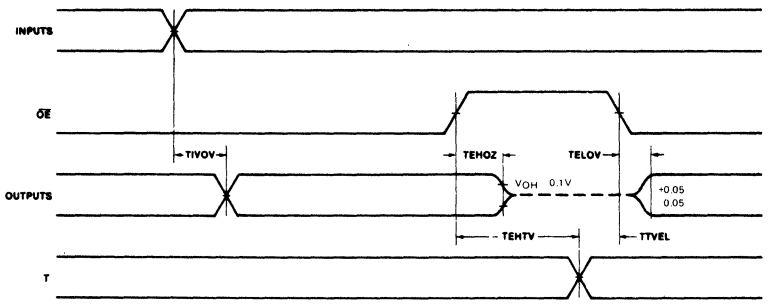
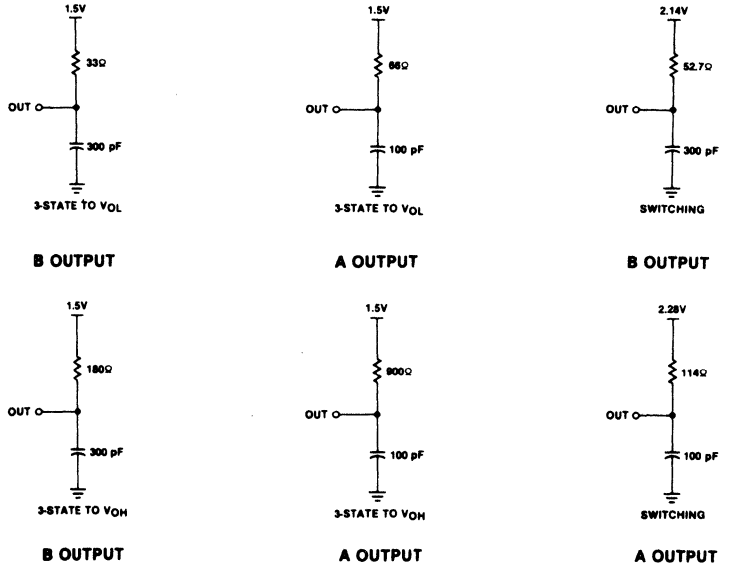
WAVEFORMS



TEST LOAD CIRCUITS



FUNCTIONAL DISCRIPTION

MOS microprocessors like the 8080/8085A/8086 are generally capable of driving a single TTL load. This also applies to MOS memory devices. While sufficient for minimum type small systems on a single PC board, it is usually necessary to buffer the microprocessor and memory signals when a system is expanded or signals go to other PC boards.
These octal bus transceivers are designed to do the necessary buffering.

Bi-Directional Driver

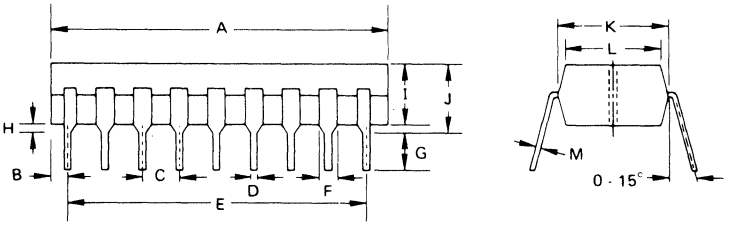
Each buffered line of the octal driver consists of two separate tri-state buffers. The B side of the driver is designed to drive 32 mA and interface the system side of the bus to I/O, memory, etc. The A side is connected to the microprocessor.

Control Gating, $\overline{OE}$, T

The $\overline{OE}$ (output enable) input is an active low signal used to enable the drivers selected by T on to the respective bus.

T is an input control signal used to select the direction of data through the transceivers. When T is high, data is transferred from the A_0-A_7 inputs to the B_0-B_7 outputs, and when low, data is transferred from B_0-B_7 to the A_0-A_7 outputs.

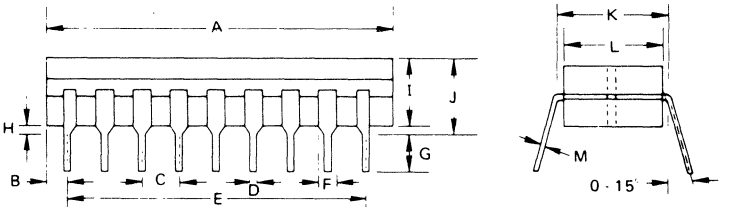
PACKAGE OUTLINE
μPD8286C
μPD8287C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPD8286D
μPD8287D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
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G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

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