μPD8086/8088 CPU SYSTEM BUS CONTROLLER

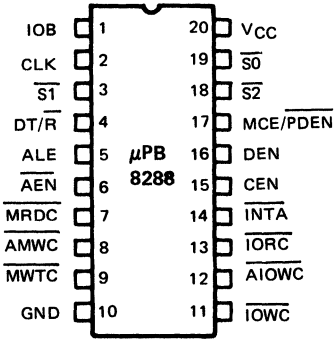
DESCRIPTION

The μPB8288 bus controller is for use in medium to large μPD8086/8088 systems. This 20-pin bipolar component provides command and control timing generation, plus bipolar drive capability and optimal system performance. It provides both Multibus™ command signals and control outputs for the microprocessor system. There is an option to use the controller with a multi-master system bus and separate I/O bus.

FEATURES

- System Controller for μPD8086/8088 Systems
- Bipolar Drive Capability
- Provides Advanced Commands
- Tri-State Output Drivers
- Can be used with an I/O Bus
- Enables Interface to One or Two Multi-Master Buses
- 20-Pin Package

PIN CONFIGURATION



PIN NAMES

S0-S2	Status Input Pins
CLK	Clock
ALE	Address Latch Enable
DEN	Data Enable
DT/R	Data Transmit/Receive
AEN	Address Enable
CEN	Command Enable
IOB	I/O Bus Mode
AIOWC	Advanced I/O Write
IOWC	I/O Write Command
IORC	I/O Read Command
AMWC	Advanced Memory Write
MWTC	Memory Write Command
MRDC	Memory Read Command
INTA	Interrupt Acknowledge
MCE/PDEN	Master Cascade/Peripheral Data Enable

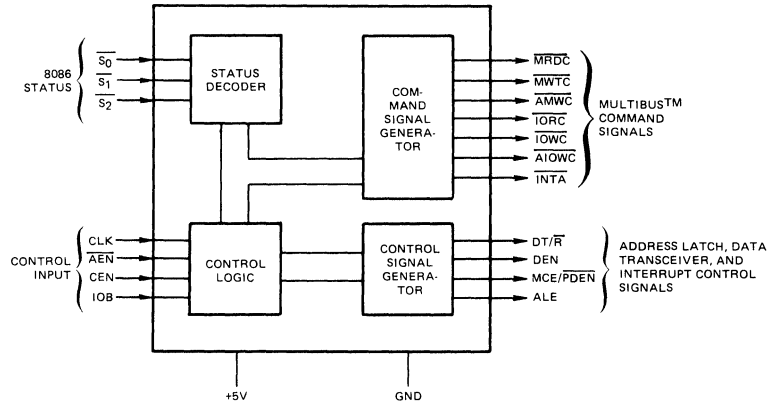
9

TM — Multibus is a trademark of Intel Corp.

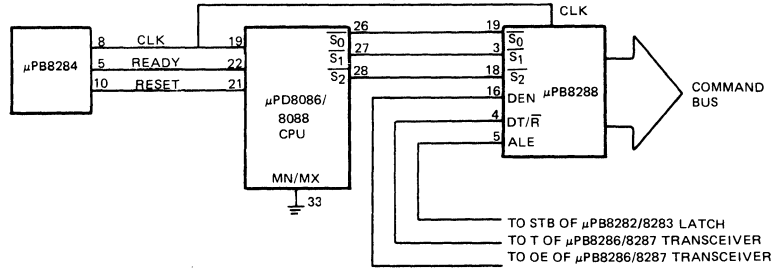
PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1	IOB	I/O Bus Mode	Sets mode of μPB8288, high for the I/O bus mode and low for the system bus mode.
2	CLK	Clock	The clock signal from the μPB8284 clock generator synchronizes the generation of command and control signals.
3, 19, 18	$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Status Input Pins	The μPB8288 decodes these status lines from the μPB8086 to generate command and control signals. When not in use, these pins are high.
4	DT/$\overline{R}$	Data Transmit/Receive	This signal is used to control the bus transceivers in a system. A high for writing to I/O or memory and a low for reading data.
5	ALE	Address Latch Enable	This signal is used for controlling transparent D type latches (μPB8282/8283). It will strobe in the address on a high to low transition.
6	$\overline{AEN}$	Address Enable	In the I/O system bus mode, AEN enables the command outputs of the μPB8288 105 ns after it becomes active. If AEN is inactive, the command outputs are tri-stated.
7	$\overline{MRDC}$	Memory Read Command	This active low signal is for switching the data from memory to the data bus.
8	$\overline{AMWC}$	Advanced Memory Write Command	This is an advanced write command which occurs early in the machine cycle, with timing the same as the read command.
9	$\overline{MWTC}$	Memory Write Command	This is the memory write command to transfer data bus to memory, but not as early as $\overline{AMWC}$. (See timing waveforms.)
11	$\overline{IOWC}$	I/O Write Command	This command is for transferring information to I/O devices.
12	$\overline{AIOWC}$	Advanced I/O Write Command	This write command occurs earlier in the machine cycle than $\overline{IOWC}$.
13	$\overline{IORC}$	I/O Read Command	This signal enables the CPU to read data from an I/O device.
14	$\overline{INTA}$	Interrupt Acknowledge	This is to signal an interupting device to put the vector information on the data bus
15	CEN	Command Enable	This signal enables all command and control outputs. If CEN is low, these outputs are inactive.
16	DEN	Data Enable	This signal enables the data transceivers onto the bus.
17	MCE/$\overline{PDEN}$	Master Cascade Enable Peripheral Data Enable	Dual function pin system. MC/E – In the bus mode, this signal is active during an interrupt sequence to read the cascade address from the master interrupt controller onto the data bus. $\overline{PDEN}$ – In the I/O bus mode, it enables the transceivers for the I/O bus just as DEN enables bus transceivers in the system bus mode.

BLOCK DIAGRAM



CONNECTING THE BUS CONTROLLER TO THE CPU



ABSOLUTE MAXIMUM RATINGS*

OPERATING TEMPERATURE	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages ①	−0.5V to +7V
All Input Voltages ①	−1.0V to +5.5V
Power Dissipation	1.5W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9

FUNCTIONAL DESCRIPTION

The three status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) from the μPD8086 CPU are decoded by the command logic to determine which command is to be issued. The following chart shows the decoding:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	μPD8086 State	μPB8288 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

There are two ways the command is issued depending on the mode of the μPB8288.

The I/O bus mode is enabled if the IOB pin is pulled high. In this mode, all I/O command lines are always enabled and not dependent upon $\overline{AEN}$. When the processor sends out an I/O command, the μPB8288 activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control any bus transceivers.

This mode is advantageous if I/O or peripherals dedicated to one microprocessor are in a multiprocessor system, allowing the μPB8288 to control two external buses. No waiting is required when the CPU needs access to the I/O bus, as an $\overline{AEN}$ low signal is needed to gain normal memory access.

If the IOB pin is tied to ground, the μPB8288 is in the system bus mode. In this mode, command signals are dependent upon the $\overline{AEN}$ line. Thus the command lines are activated 105 ns after the $\overline{AEN}$ line goes low. In this mode, there must be some bus arbitration logic to toggle the $\overline{AEN}$ line when the bus is free for use. Here, both memory and I/O are shared by more than one processor, over one bus, with both memory and I/O commands waiting for bus arbitration.

Among the command outputs are some advanced write commands which are initiated early in the machine cycle and can be used to prevent the CPU from entering unnecessary wait states.

The $\overline{INTA}$ signal acts as an I/O read during an interrupt cycle. This is to signal the interrupting device that its interrupt is being acknowledged, and to place the interrupt vector on the data bus.

The control outputs of the μPB8288 are used to control the bus transceivers in a system. DT/$\overline{R}$ determines the direction of the data transfer, and $\overline{DEN}$ is used to enable the outputs of the transceiver. In the IOB mode the MCE/$\overline{PDEN}$ pin acts as a dedicated data enable signal for the I/O bus.

The MCE signal is used in conjunction with an interrupt acknowledge cycle to control the cascade address when more than one interrupt controller (such as a μPD8259A) is used. If there is only one interrupt controller in a system, MCE is not used as the $\overline{INTA}$ signal gates the interrupt vector onto the processor bus. In multiple interrupt controller systems, MCE is used to gate the μPD8259A's cascade address onto the processors local bus, where ALE strobes it into the address latches. This occurs during the first $\overline{INTA}$ cycle. During the second $\overline{INTA}$ cycle the addressed slave μPD8259A gates its interrupt vector onto the processor bus.

The ALE signal occurs during each machine cycle and is used to strobe data into the address latches and to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into the μPB8288. ALE also occurs during a halt state to accomplish this.

The CEN (Command Enable) is used to control the command lines. If pulled high the μPB8288 functions normally and if grounded all command lines are inactive.

DC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Input Clamp Voltage	V_C		−1	V	I_C = −5 mA
Power Supply Current	I_{CC}		230	mA	
Forward Input Current	I_F		−0.7	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	$V_R = V_{CC}$
Output Low Voltage — Command Outputs Control Outputs	V_{OL}		0.5 0.5	V V	I_{OL} = 32 mA I_{OL} = 16 mA
Output High Voltage — Command Outputs Control Outputs	V_{OH}	2.4 2.4		V V	I_{OH} = −5 mA I_{OH} = −1 mA
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.0		V	
Output Off Current	I_{OFF}		100	μA	V_{OFF} = 0.4 to 5.25V

AC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

TIMING REQUIREMENTS

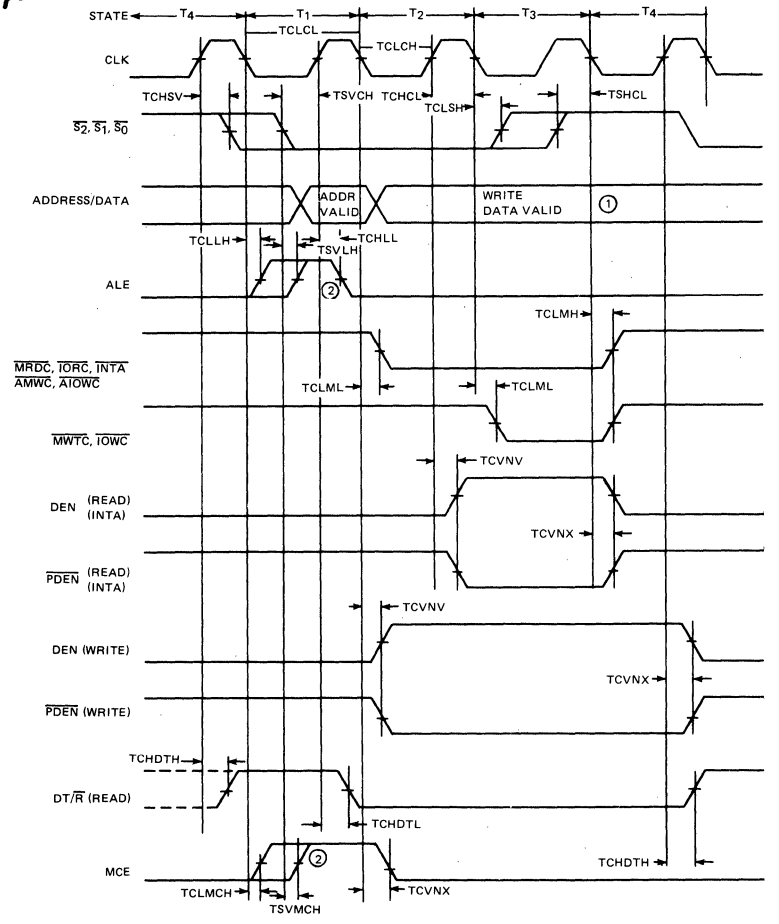
PARAMETER	SYMBOL	MIN	MAX	UNIT	LOADING
CLK Cycle Period	TCLCL	125		ns	
CLK Low Time	TCLCH	66		ns	
CLK High Time	TCHCL	40		ns	
Status Active Setup Time	TSVCH	65		ns	
Status Active Hold Time	TCHSV	10		ns	
Status Inactive Setup Time	TSHCL	55		ns	
Status Inactive Hold Time	TCLSH	10		ns	

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNIT	LOADING
Control Active Delay	TCVNV	5	45	ns	
Control Inactive Delay	TCVNX	10	45	ns	
ALE MCE Active Delay (from CLK)	TCLLH, TCLMCH		15	ns	
ALE MCE Active Delay (from Status)	TSVLH, TSVMCH		15	ns	$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
ALE Inactive Delay	TCHLL		15	ns	
Command Active Delay	TCLML	10	35	ns	
Command Inactive Delay	TCLMH	10	35	ns	
Direction Control Active Delay	TCHDTL		50	ns	
Direction Control Inactive Delay	TCHDTH		30	ns	
Command Enable Time	TAELCH		40	ns	
Command Disable Time	TAEHCZ		40	ns	
Enable Delay Time	TAELCV	105	275	ns	Other: I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 80 pF
AEN to DEN	TAEVNV		20	ns	
CEN to DEN, PDEN	TCEVNV		20	ns	
CEN to Command	TCELRH		TCLML	ns	

9

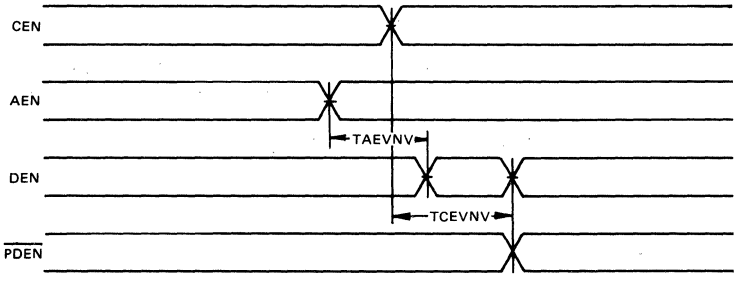
TIMING WAVEFORMS



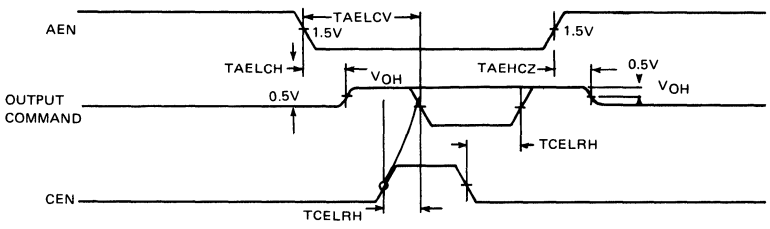
NOTES:

1. ADDRESS/DATA BUS IS SHOWN ONLY FOR REFERENCE PURPOSES.
2. LEADING EDGE OF ALE AND MCE IS DETERMINED BY THE FALLING EDGE OF CLK OR STATUS GOING ACTIVE, WHICHEVER OCCURS LAST.
3. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS SPECIFIED OTHERWISE.

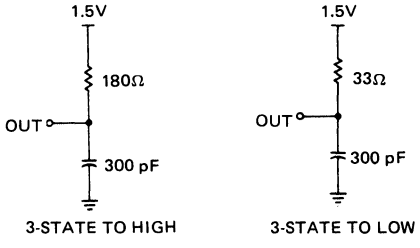
DEN, $\overline{\text{PDEN}}$ QUALIFICATION TIMING



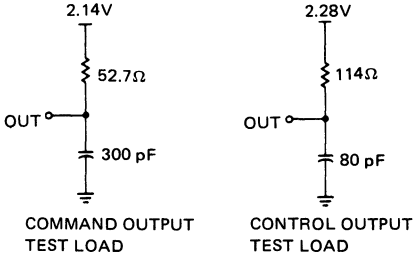
μPB8288 ADDRESS ENABLE ($\overline{AEN}$) TIMING (3-STATE ENABLE/DISABLE)



TEST LOAD CIRCUITS



3-STATE COMMAND OUTPUT TEST LOAD



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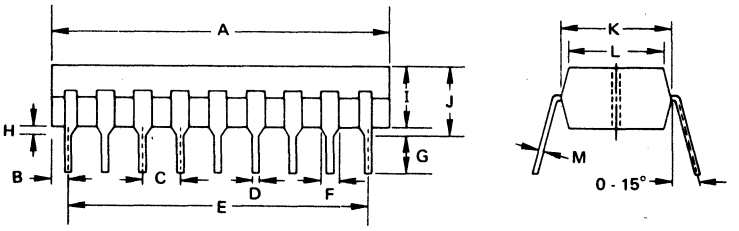
PACKAGE OUTLINES
μPB8288C



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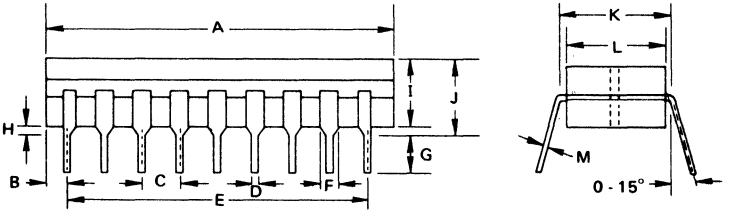
ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPB8288D



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ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01