# μPC1477C

## FM DEMODULATOR FOR DBS RECEIVER

## SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

### DESCRIPTION

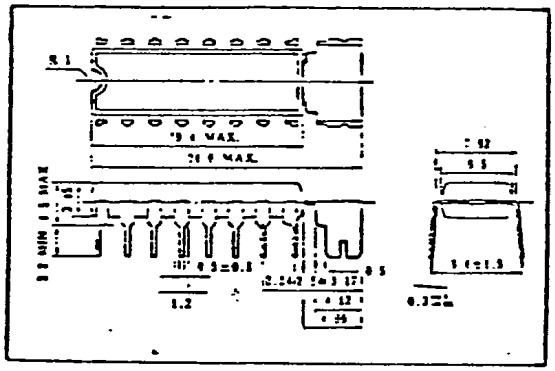
μPC1477C is designed for PLL demodulator in DBS receivers(Indoor Unit). μPC1477C have the functions of phase detector, DC amplifier, and VCO with buffer amplifier.

μPC1477C is able to operate as high as 600MHz for 2nd IF of DBS receiver by incorporating high $f_T$ transistors into the circuit,and it is obtained wide PLL capture range with external variable capacitance diode.

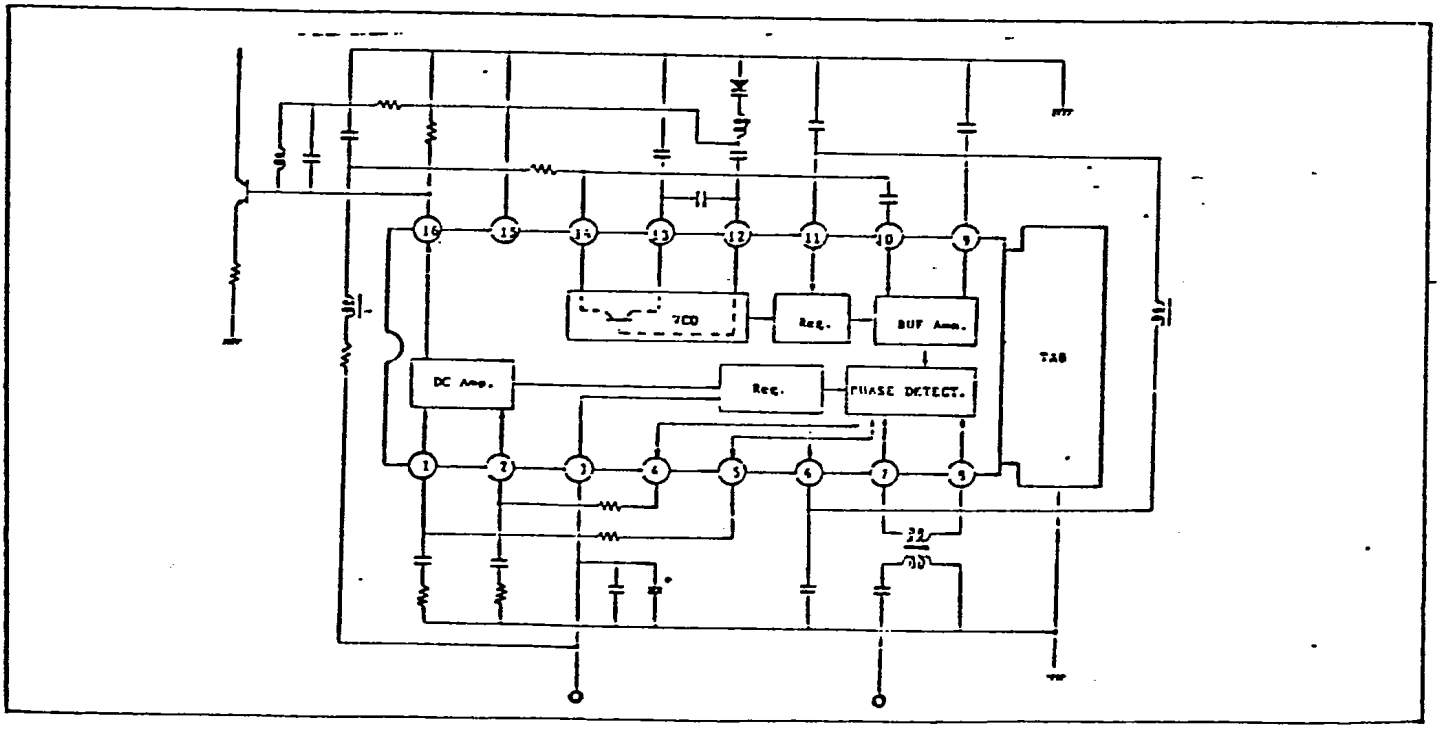
### FEATURES

- Low differential gain and low differential phase(2%,2° typ.)
- High S/N ratio(60dB typ.)
- Wide PLL capture range(±20MHz typ.@ $f_0$=400MHz)

### PACKAGE DIMENSIONS(Unit;mm)



### BLOCK DIAGRAM






NEC Corporation

APPLICATION OF THE uPC1477C

# DESIGN OF FM DEMODULATOR FOR THE DBS RECEIVER

## 1. INTRODUCTION

The uPC1477C is a monolithic integrated circuit designed for demodulation of high-frequency,wide-band FM signals. It is the most suitable for the FM demodulator in the DBS receiver.



There are three factors that must be given special consideration when designing the FM demodulator for the DBS receiver:

- Low C/N (approaching the threshold level of the FM demodulator).
- Wide frequency daviation
- Few 2nd IF frequencies to choose from

Although there are various FM demodulating method, the following are most commonly used:

- Dual synchronization
- Delayed detection
- PLL detection

Each of these method can be used for FM demodulation of wide frequency deviation signal. The PLL detection method in paticlar provides a filter to limit the noise band in the loop, and has good demodulation characteristics at low C/N. It is also suitable for use in an IC. Therefore, the uPC1477C utilizes PLL detection.

## 2. DESCRIPTION OF THE uPC1477C

The uPC1477C have multiplier which is designed by using dual differential amplifiers for the phase detector.
The VCO is colpitts type oscillator which is used external varicap diode in order to cover wide deviation.
The VCO output signal is injected into the phase detector with ±180° phase difference by the buffer amplifier for the VCO.
The uPC1477C also contains DC amplifier in order to get enough loop gain.



## 3. SELECTING THE 2ND IF FREQUENCY

If we look at the 2nd IF frequencies used in Japan for the DBS receiver, we find that there are just two, 130MHz and 400MHz. However, in the rest of the world, various other frequencies are also used, including 70MHz, 480MHz, 612MHz.

Selection of the best 2nd IF frequency depends primarily on image rejection and the characteristics of the filter to be used in the 2nd IF stage. However, this 2nd IF frequency will have influence on the characteristics of the FM demodulator.

For example, the primary consideration when using the uPC1477C is selection of an appropriate varicap diode for the VCO. If the same item is used at 130MHz and 400MHz, the feed back voltage will be much larger in order to cover regulate FM deviation at 130MHz application. Therefore, the non-linearity of varicap diode will adversely influence various characteristics after demodulation. The following products are recommended for use with each 2nd IF frequency:

* 130MHz : 1SV184
* over 400MHz : 1S2208(B)

The characteristics of the uPC1477C as described in this application note based on use of a 400MHz 2nd IF frequency.

## 4. LPF DESIGN

In designing a PLL demodulator, the most important point is design of the LPF. Generaly, there are three kind of LPF (lag, lag/lead, active filter). Here, we will use a lag/lead filter.



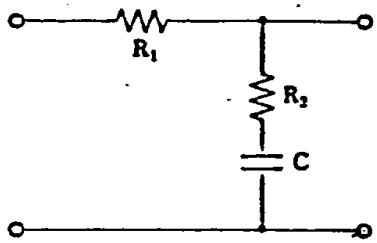



Figure 1 Lag/Lead Filter

The trasfer function for the lag/lead filter shown in Figure 1 can be given as :

$$H(S)=\frac{W_n^2+W_n\left(2\zeta-\frac{W_n}{K\phi K_V K_D}\right)S}{S^2+2\zeta W_n S+W_n^2}$$

Where

$$W_n=\sqrt{\frac{K\phi K_V K_D}{T_1+T_2}} \quad \cdots\cdots ①$$

$$\zeta=\frac{W_n}{2}\left(T_2+\frac{1}{K\phi K_V K_D}\right) \quad \cdots\cdots ②$$

Kφ : Phase detector gain

$K_V$ : VCO gain

$K_D$ : DC Amp gain

Wn : Natural loop frequency

ζ : Loop damping factor

### 4.1 Wn

The Wn can be determined by the relation Wn = Wn t/t in Fig.2 which described as PLL indicial response. In this case, the optional lock-up time is necessary to determine initially. However, when using a PLL for the demodulator, it is also necessary to limit the loop noise band. Thus, Wn must be initialized.

In Japan, it is recommended that the 2nd IF in the DBS receiver have a bandwidth of 27MHz at -3dB.

Therefore, this value can be used as Wn (=2πf).

Care must be exercised in setting the value of Wn. If a small Wn is chosen to make the noise band narrower, this will also attenuate the signal around the maximum frequency deviation and decrease C/N.

This could easily generate truncation noise.

On the other hand, if a large Wn is chosen to increase the capture range, the noise band will be made wider, therefore, degrade S/N after demodulation. In general, Wn should be set to twice the muximum modulation frequency + Δf (the frequency deviation). Thus, for a video signal, Wn should be 17MHzp-p + 4.5MHz x 2 = 26MHz.

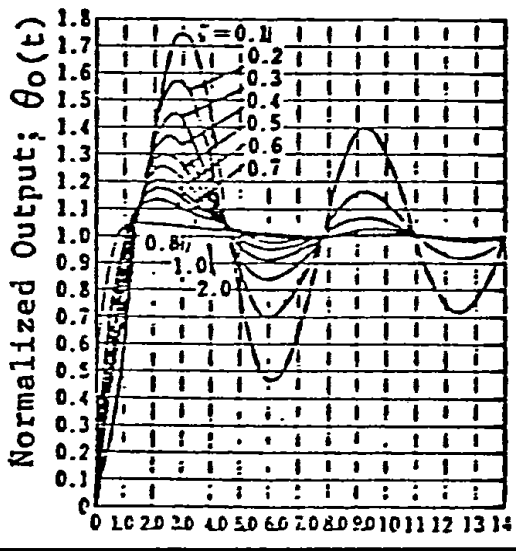
Therefore, the 27MHz 2nd IF bandwidth value quoted above is a proper value, and gives the Wn as follows.

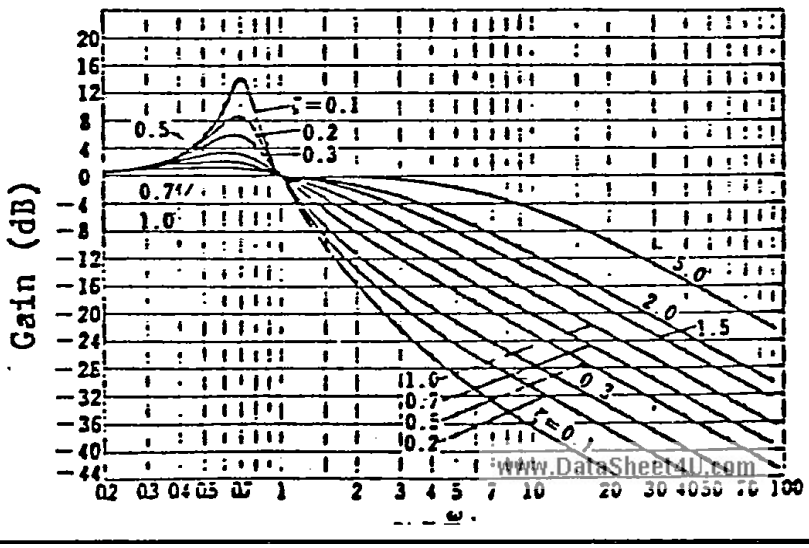
$$Wn = 2 \times 27 \times 10^6$$

$$= 1.7 \times 10^8$$

## 4.2 ζ (DAMPING FACTOR)

It is also necessary to determine the initial damping factor. Figures 2 and 3 show the indicial response and the closed-loop frequency characteristics for a lag/lead filter applied to a PLL circuit, respectively.



According to Figures 2 and 3, the $\zeta$ should be chosen large value in order to get stable loop, but it decreases the amount of attenuation at the out of the band ($\frac{W}{Wn}$ >1), and increases noise in the loop. The figures also show that reducing $\zeta$ is a good way to increase attenuation of the signal at the out of the band, however, Wnt will be large until the loop stabilizes, so overshoot will be larger.

A $\zeta$ of 0.707 is often used (however any $\zeta$ of more than 0.3 will cause no trouble).

4.3 PHASE DETECTOR GAIN

The gain of the phase detector in the uPC1477C can be determined as follows.

$$K_\phi = \alpha \cdot V_{in} \cdot A_\phi \cdot \frac{2}{\pi} \text{ (V/rad)} \quad \cdots\cdots\cdots \text{③}$$

$$\alpha = \frac{h_{fe}}{1 + h_{fe}} = \frac{4}{1 + 4} = 0.8$$

; $f_T$ of a transistor in the uPC1477C is 1.5GHz. When an operating frequency of 0.4GHz is applied, ∴ hfe = 4

Vin : The input voltage is set by AGC Amplifier. Thid voltage is normary 200mVp-p (-10dBm).

$A\phi$ : The gain of the phase detector can be found from the $R_L/r_e + R_E$ for the circuit.

From Figure 4

$$r_e = \frac{26\ mV}{3.8\ mA} = 6.8\ \Omega$$

$$R_E = 240/3 = 80\ \Omega$$

$$R_L = 180\ \Omega$$

$$\therefore A_\phi = \frac{180}{6.8+80} = 2.07$$

From equation ③

$$K_\phi = 0.8 \times 0.2 \times 2.08 \times 2/\pi$$

$$= 0.211\ V/rad$$

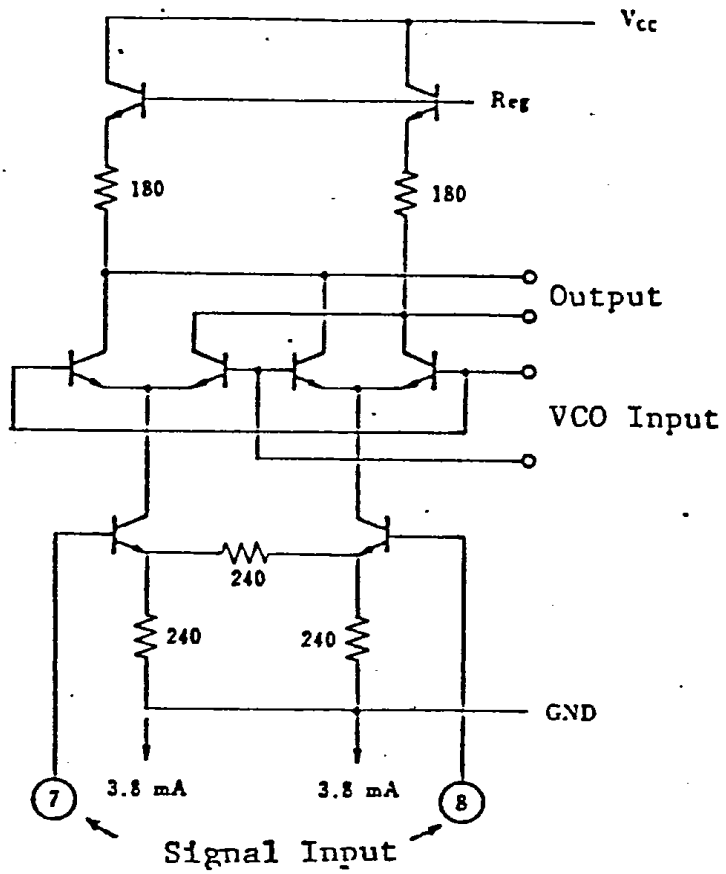


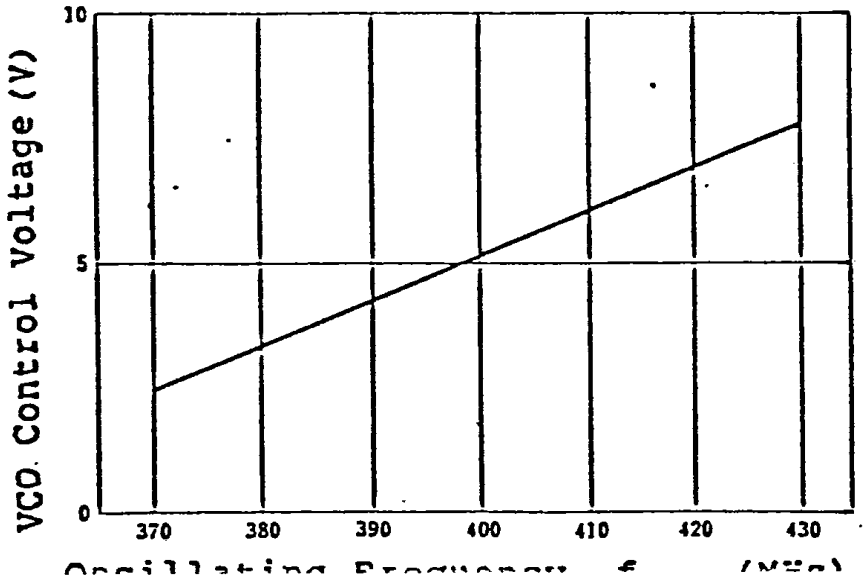

Figure 4 Phase detector Equivalent Circuit

4.4 VCO GAIN

The gain for the VCO is calculated from the following equation

$$K_V = \frac{\Delta f}{\Delta V} \cdot 2\pi\ (rad/v.s)$$

As shown in Figure 5, the VCO frequency change is 10MHz per volt.



## 4.5 DC AMP. GAIN

As shown in Figure 6, the DC Amp. gain is 27dB (22.4 times).

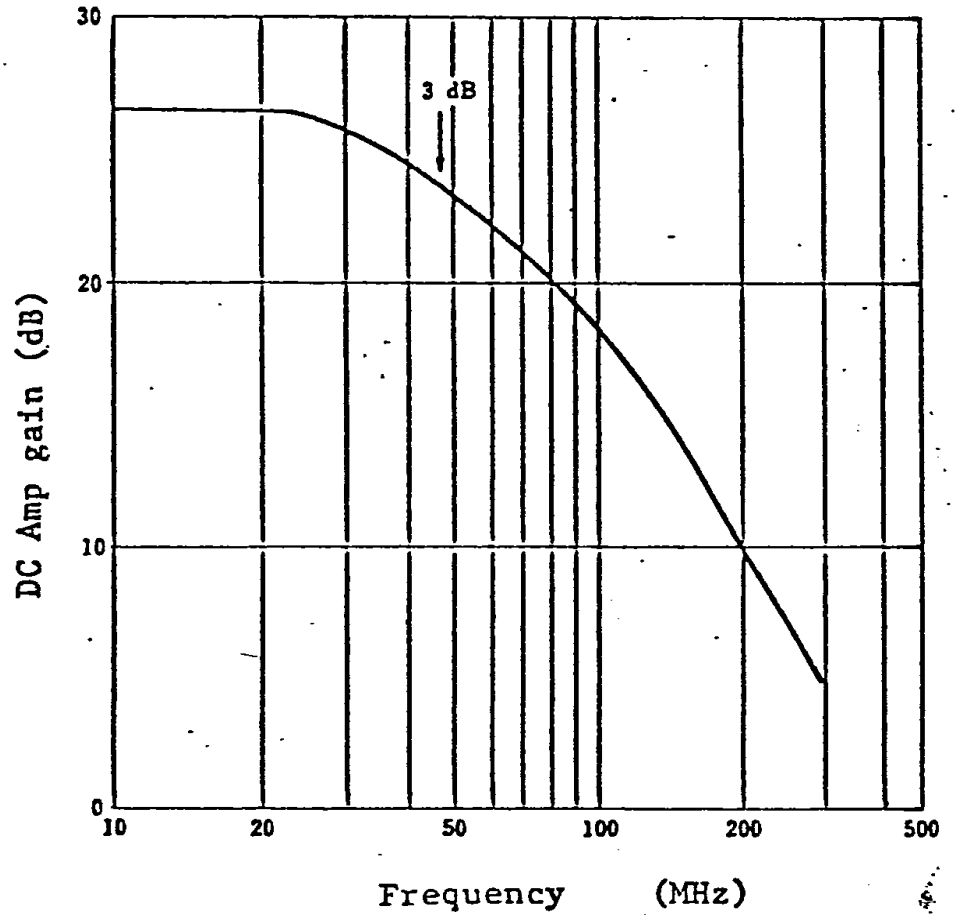



Figure 6 DC Amp Gain vs. Frequency

## 4.6 DETERMINING THE LPF CONSTANT VALUES

First, $T_2$ must be determined from Equation ②:

$$\zeta = \frac{W_n}{2}\left(T_2 + \frac{1}{K\phi K_V K_D}\right)$$

$$T_2 = \frac{2\zeta}{W_n} - \frac{1}{K\phi K_V K_D} \quad \text{Additionally,} \quad T_2 = R_2 C \quad \cdots\cdots ④$$

$$= \frac{2 \times 0.707}{1.7\times10^{6}} - \frac{1}{0.211\times6.28\times10^{7}\times22.4}$$

$$= 4.95\times10^{-9}$$

Next, we insert the value of $T_2$ into Equation ① to determine $T_1$.

$$W_n=\sqrt{\frac{K_\phi K_V K_D}{T_1+T_2}}$$

$$T_1=\frac{K_\phi K_V K_D}{W_n^2}-T_2 \quad \text{Where } T_1=R_1C \quad \cdots\cdots\cdots\cdots\cdots\cdots ⑤$$

$$=\frac{0.211\times 6.28\times 10^7\times 22.4}{(1.7\times 10^8)^2}-4.95\times 10^{-9}$$

$$=5.32\times 10^{-9}$$

Then, we determine the value of C or $R_2$ using Equation ④, $T_2 = R_2C$. If C = 100pF, then



$$R_2=\frac{4.95\times 10^{-9}}{100\times 10^{-12}}$$

$$=49.5(\fallingdotseq 50\ \Omega)$$

From Equation ⑤,

$$T_1=R_1C$$

$$R_1=\frac{5.32\times 10^{-9}}{100\times 10^{-12}}$$

$$=53.2(\fallingdotseq 50\ \Omega)$$

Thus, from the above calculations, the components in the lag/lead filter shown in Figure 1 have the following constant values:

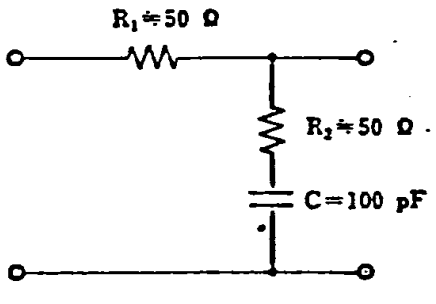



Figure 7 Lag/Lead Filter Values

The LPF is applied at two places to the uPC1477C: between terminals 4 and 2, and between terminals 5 and 1. The series rasistor, $R_1$, is also used as the bias resistor for the DC Amp.

## 5. INPUT LEVEL TO THE uPC1477C

The data shown in Figure 8 correlates uPC1477C input level to capture and lock ranges. The capture range should be higher than the 27MHz 2nd IF bandwidth.
As show in the figure, Pin ≧ -13dBm achieves this requirement.

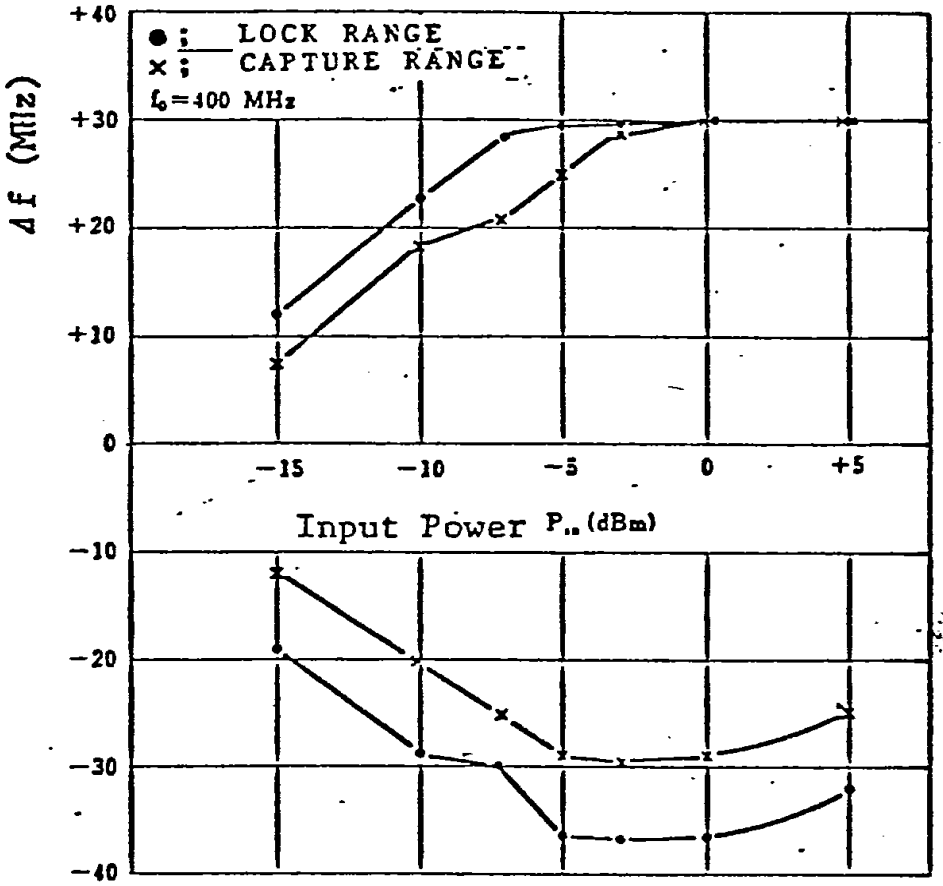



Figure 8 Capture/Lock Range vs. Input power

One method of determining the best input level is to look the triangular noise after demodulation. This triangular noise is a paticular FM noise which increases at a high-frequency area, therefore the S/N will degrade at a high-frequency area of the video dignal.

It is called triangular noise because it takes the shape shown in Figure 9.

This type of noise is usually prevented by the use of pre-emphasis (strengthening of the high-frequency ingredients in the video signal before modulating the carrier) during transmission, and the high-frequency of the demodulated video signal is reduced by the de-emphasis.

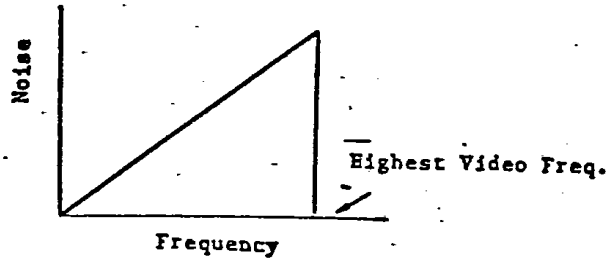



Figure 9 Noise spectrum

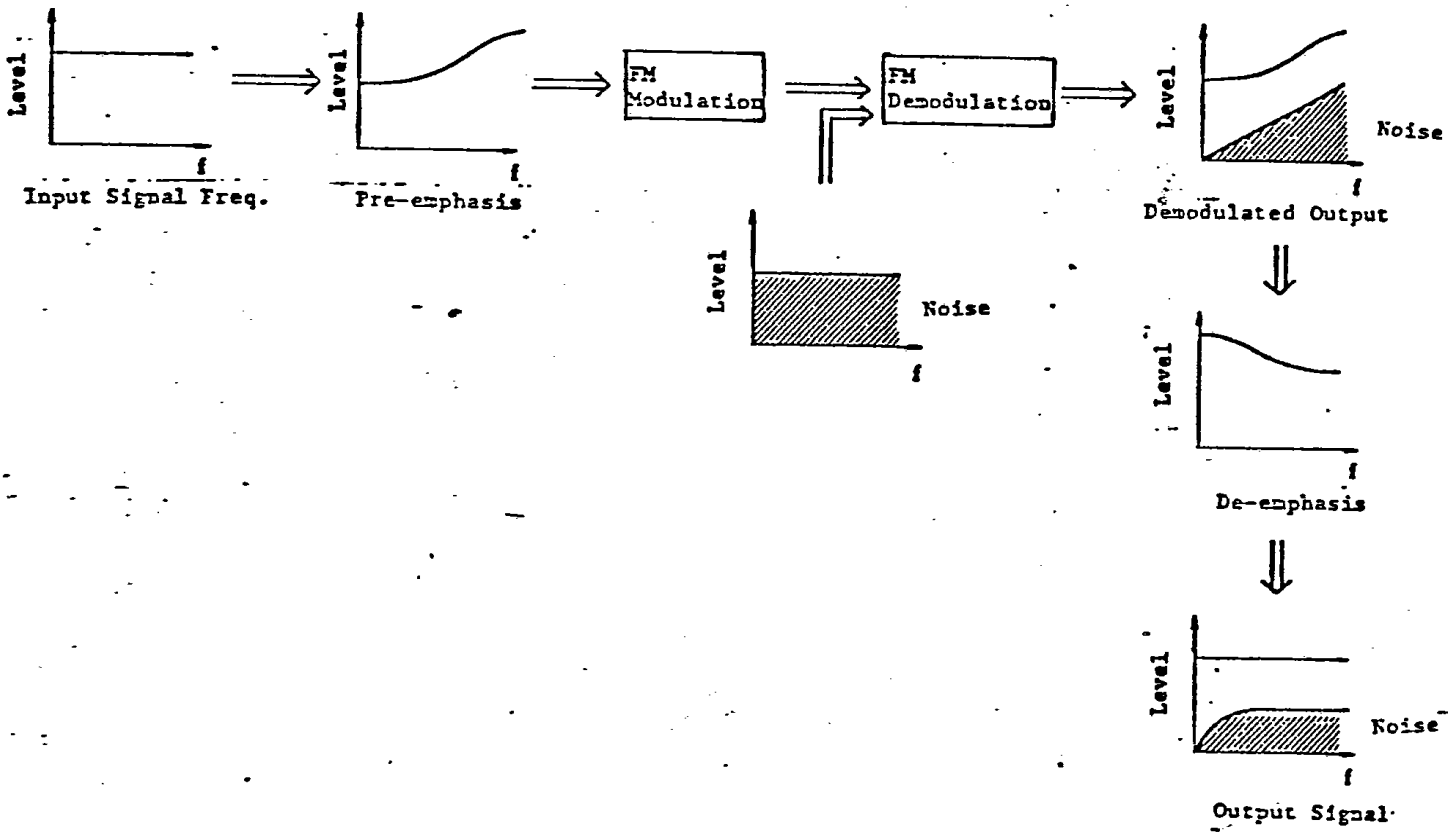



Figure 10 Effect of Pre-emphasis on Triangular Noise

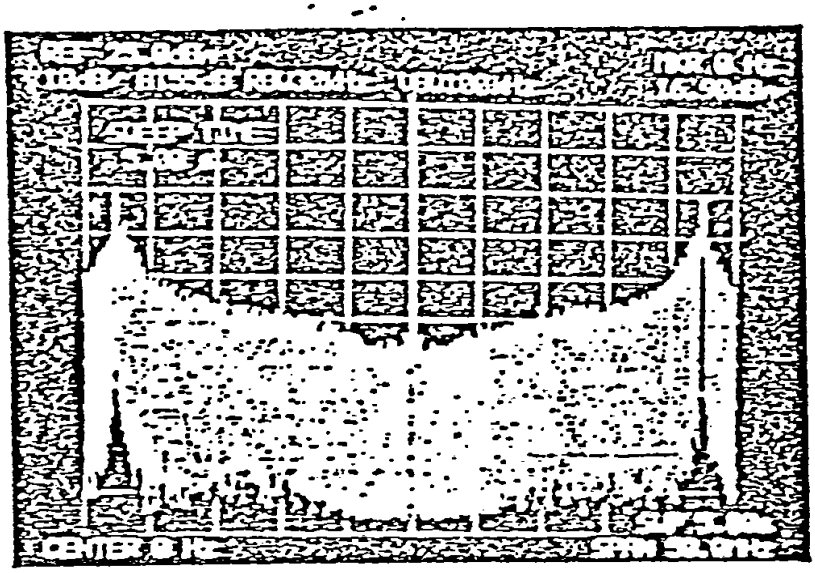
The trianglar noise spectrum is determined by input signal level to the demodulator. It is the most suitable input signal level when the ideal trianglar nois spectrum is observed.

The output triangular noise spectrum for various input levels to the uPC1477C are shown in picture 1. These pictures are observed at the white noise on the unmodulated carrier.

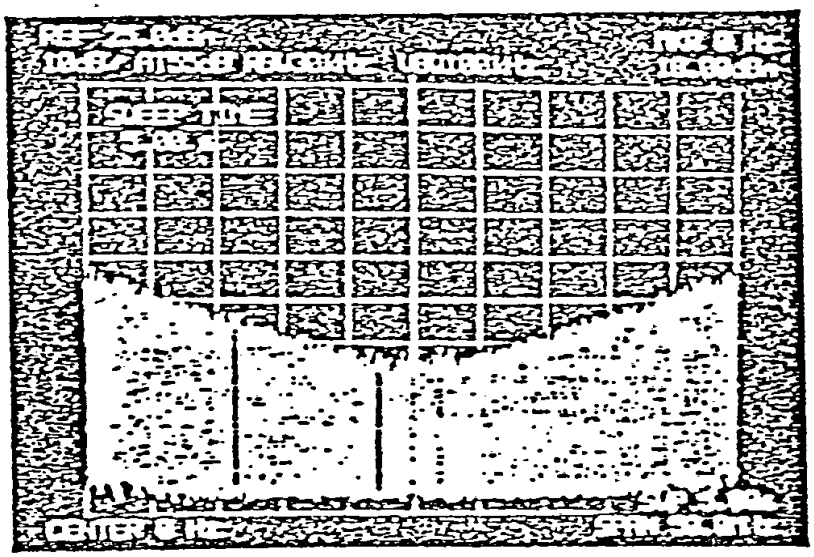
From the viewpoint of capture or lock range, an input level at least -13dBm is sufficient but, as shown by the pictures, if the input level is more than 0dB, the increase in triangular noise at the high end of the band becomes excessive.

Because, the uPC1477C is not included a limitter in front of the phase detector. Thus, the gain of the loop is increased to get the output voltage proportional to the input level, if the input level is set too high, it will generate to parasitic oscillation of the loop.

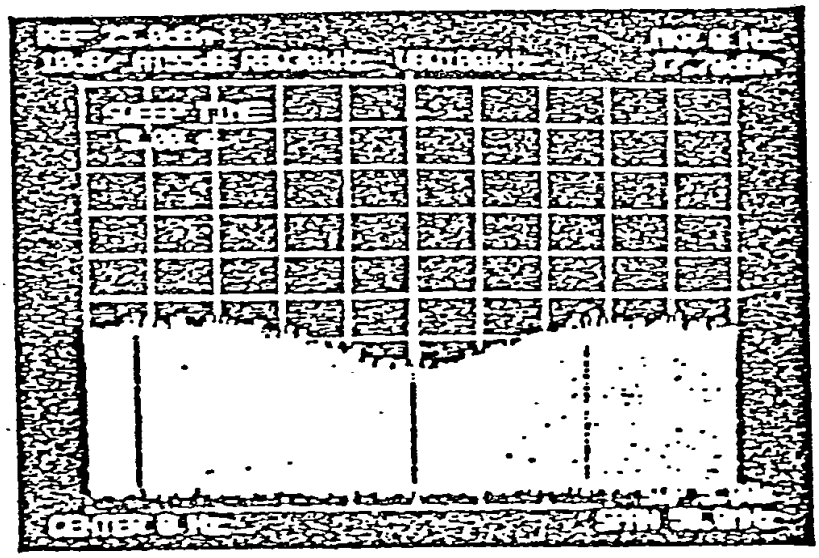
It has been found that the best input level for the uPC1477C uPC1477C is between -7 and -10dBm.



(a) $P_{in}$ = +5 dBm



(b) $P_{in}$ = −7 dBm



(c) $P_{in}$ = −13 dBm

Picture 1 Trianglar Noise Spectrum

## 6. THRESHOLD LEVEL

The carrier is transmited through space which is approxinately 36,000km away from the satellite.
This destance greatly attenuates the carrier and decreases C/N. Even though a C/N of 14dB could be ensured in an ordinary receiving, C/N could still be degraded by various unexpected conditions between the satellite and receiver.

Therefore, the FM demodulator requires a type of threshold extention. Usaually, this threshold extention is described as the C/N value at that point on the S/N (after demodulation) vs. C/N curve where the S/N is 1dB degraded than the change in C/N.

To confirm the threshold level for the uPC1477C, set up the mesurement system show in Figurell. The data for S/N vs. C/N should be as shown in Figures 12 and 13.

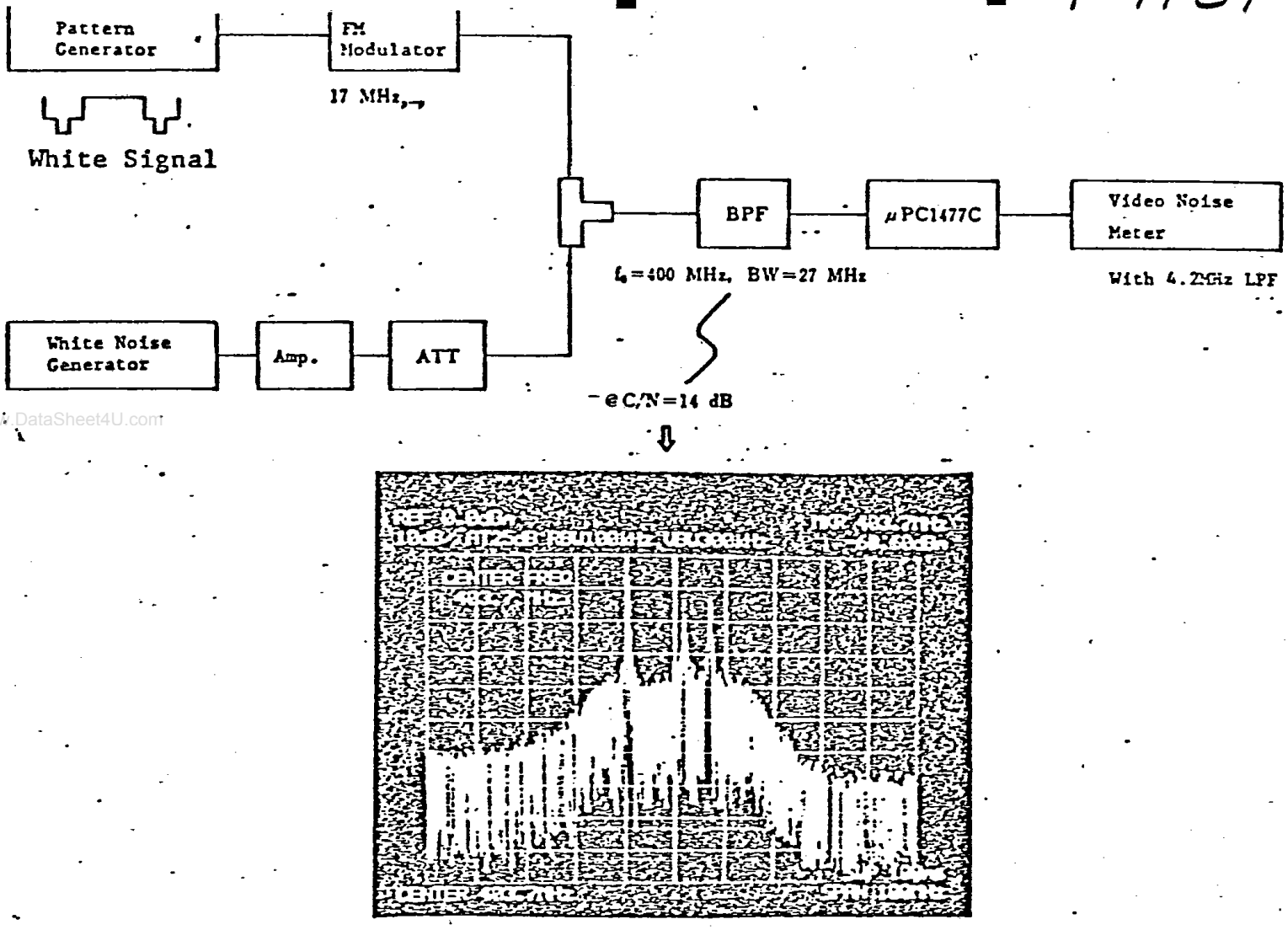







Figure 11 Block-Diagram for C/N, S/N Measurement

Figure 11 shows block-diagram for C/N, S/N measurement. The FM modulator output signal is made 17MHz modulation by white signal. Generate the white noise on a sparate line containing an attenuator that can be used to vary the white noise level. Make a composite of these signals and supply them through a 27MHz BPF to the uPC1477C. Measure the S/N ratio after demodulation using a video noise meter. The LPF in this meter should be set to 4.2MHz.

Figure 12 shows the demodulated S/N curve which is changed C/N values at wide range.

As shown in Figure 12, S/N saturates at about 60dB when the C/N is increased exceedingly.

The data shown in Figure 13 which is confirmed the threshold level.

According to Figure 13, the threshold C/N level is 7dB, so the uPC1477c is extended 3dB than conventional FM demodulator which has the threshold C/N level of 10dB.



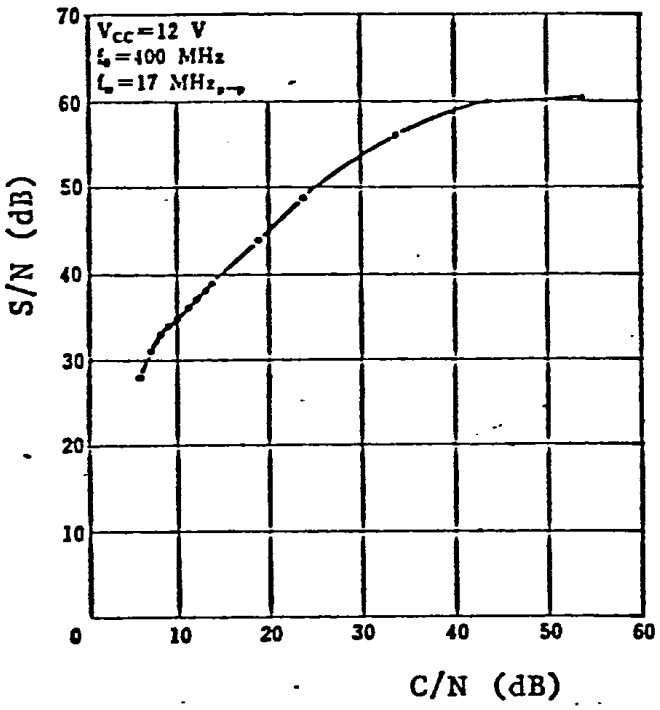



Figure 12 C/N vs. S/N

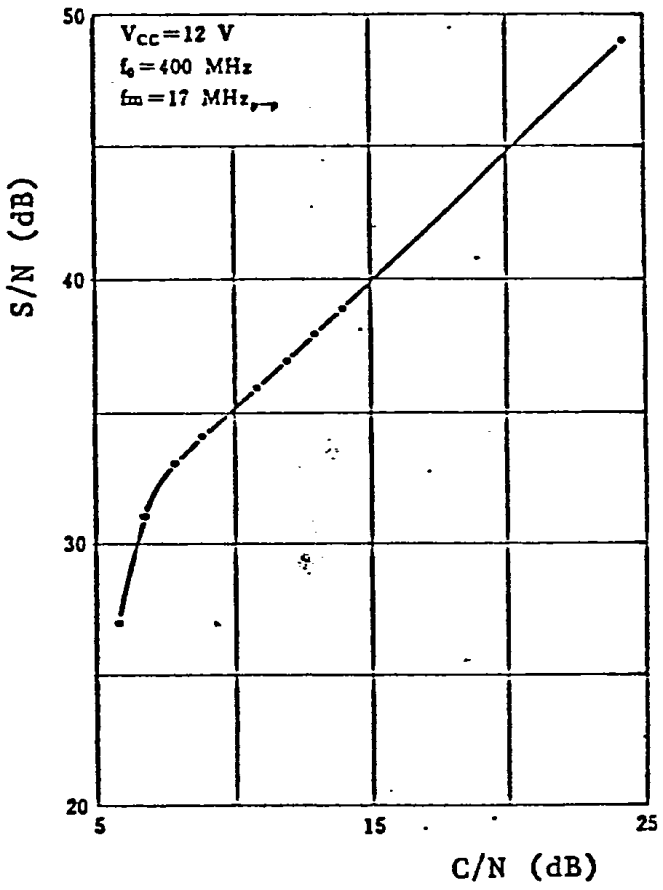
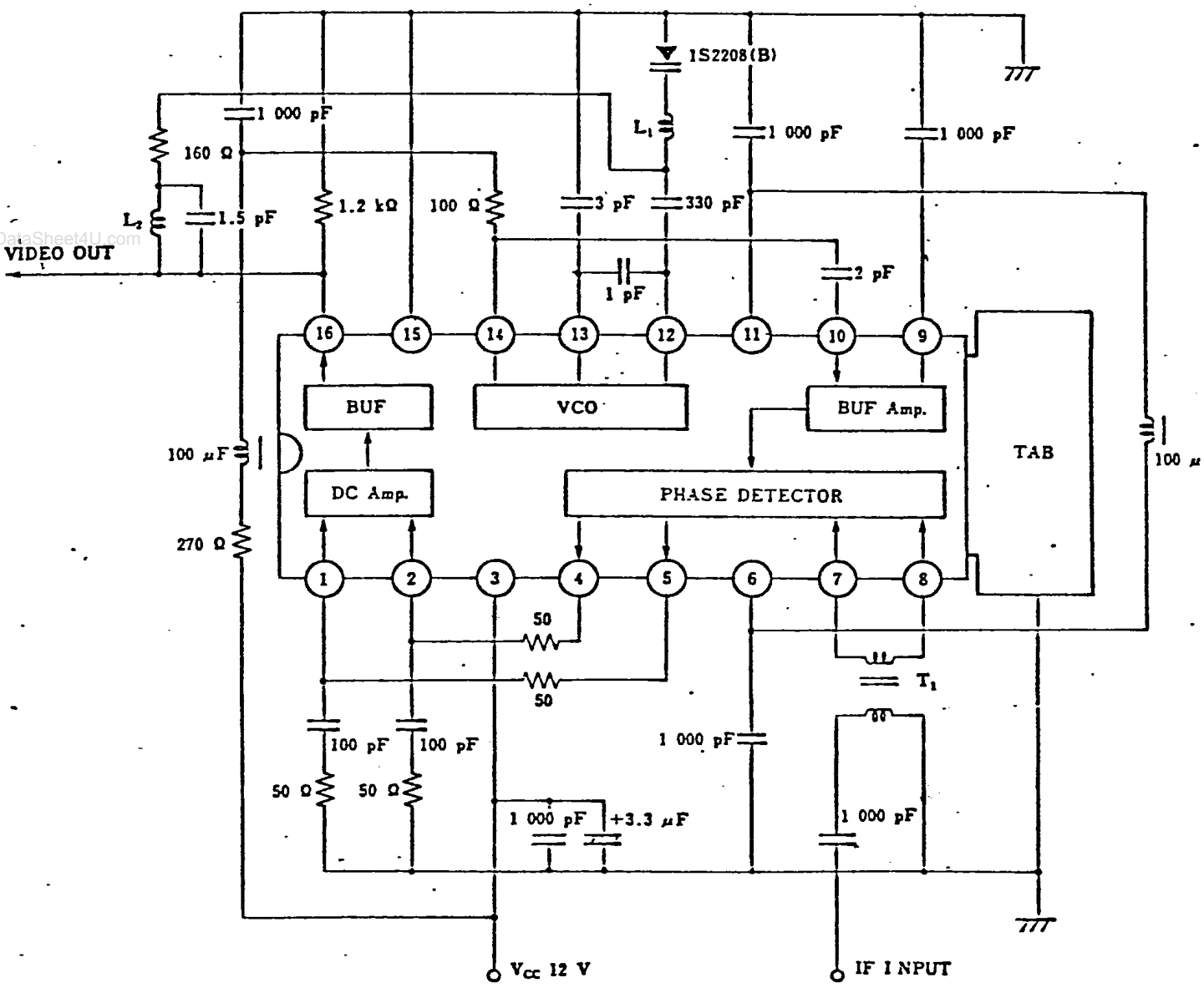



Figure 13 C/N vs. S/N




$L_1$ ; 2 Turns , Core Diameter 5mm
Wire Diameter 1mm

$L_2$ ; TOKO YTKENBS-28905NY

$T_1$ ; TDK WBT5.5P5-C10129A

Figure 14 Typical Application Circuit

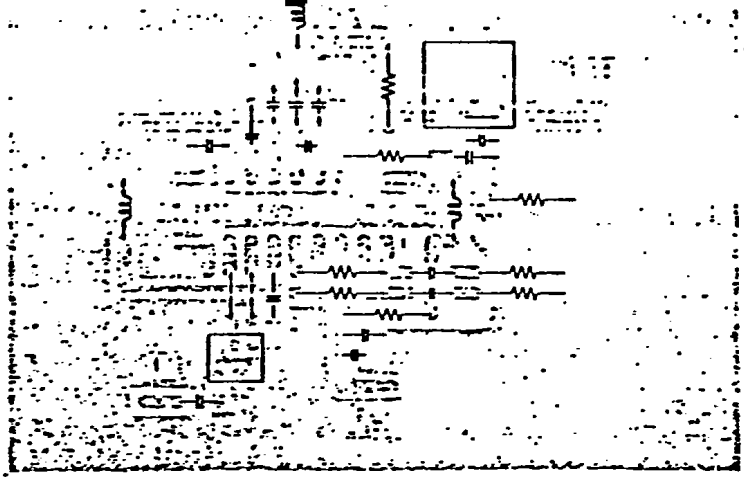




Figure 15 Printed Board for Typical Application Circuit

Table 1 uPC1477C Electrical Characteristics

| Item | Symbol | MIN. | TYP. | MAX. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Circuit Current | $I_{CC}$ | 55 | 65 | 75 | mA | with no signal applied |
| Capture Range | | ±15 | ±20 | | MHz | $f_0$=400 MHz, $P_{in}$=−10 dBm |
| Lock Range | | ±20 | ±25 | | MHz | |
| Differential Gain | DG | | 2.0 | 3.5 | % | $P_{in}$=−10 dBm, $f_0$=400 MHz |
| Differential Phase | DP | | 2.0 | 3.5 | deg | $\Delta f_m$=17 $MHz_{p-p}$, Stair Signal |
| Video S/N | S/N | 55 | 60 | | dB | $f_0$=400 MHz, $P_{in}$=−10 dBm, White Signal |
| VCO Sensitivity | | 8 | 10 | | MHz/V | $f_0$=400 MHz |
| VCO Drift | $\Delta f_{OSC}$ | | ±1.0 | ±2.0 | MHz | $f_0$=400 MHz, 12 V±10 % |

Figure 14 shows a typical application circuit for the uPC1477C and the printed board shown in Figure 15. Electrical characteristics of the uPC1477C are shown in Table 1.

Although not shown in application circuit, de-emphasis must be incerted after demodulation. In this case, the de-emphasis circuit should be incerted to output terminal (16pin), and should be connected to the next stage through an emitter follower circuit.

A typical de-emphasis circuit is shown in Figure 16 for reference.

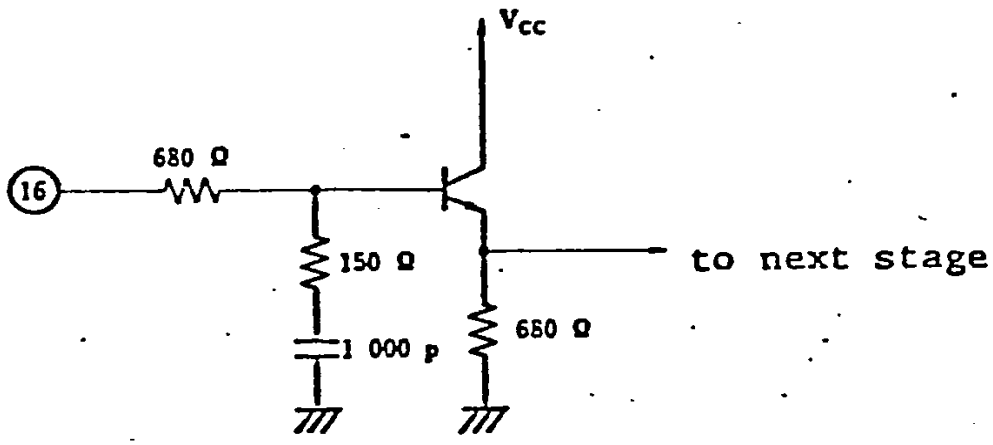



Figure 16 Typical De-emphasis Circuit

The characteristics of the application circuit are listed in Table 1.

All characteristics obtained here meet actual requirements for the DBS receiver. Especially DG, DP values are excellent such as 2%, 2° respectively.

Test results at 400MHz are introduced above. In addition frequency responce of the uPC1477C is quite good so it operates both at 130MHz and 612MHz with slight modification of circuits.

ABSOLUTE MAXIMUM RATINGS (Ta=25 °C)

| | | | |
|---|---|---|---|
| Supply Voltage | Vcc | 14.5 | V |
| Power Dissipation | $P_T$ (Ta=75°C) | 910 | mW |
| Operating Temperature | Topr | -20 to +75 | °C |
| Storage Temperature | Tstg | -40 to +125 | °C |

RECOMMENDED OPERATING CONDITIONS

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | 10.8 | 12.0 | 13.2 | V |
| Input Level | Pin | -13 | | -5 | dBm |

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=12V)

| CHARACTERISTICS | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Total Supply Current | Icc | 55 | 65 | 75 | mA | Zero Carrier |
| PLL Capture Range | | ±15 | ±20 | | MHz | $f_0$=400MHz, Pin=-10dBm |
| PLL Lock Range | | ±20 | ±25 | | MHz | " |
| Differential Gain | DG | | 2.0 | 3.5 | % | $f_0$=400MHz, Pin=-10dBm |
| Differential Phase | DP | | 2.0 | 3.5 | deg | fm=17MHz, Stair Step |
| Signal to Noise Ratio | S/N | 55 | 60 | | dB | $f_0$=400MHz, Pin=-10dBm<br>fm=17MHz, White Signal |
| VCO Sensitivity | | 8 | 10 | | MHz/V | $f_0$=400MHz |
| VCO Freq. Drift | | ±1.0 | ±2.0 | | MHz | $f_0$=400MHz, Vcc±10% |