BIPOLAR ANALOG INTEGRATED CIRCUITS

T-74-07-01

μPC1663, μPC1664

ULTRA-WIDEBAND DIFFERENTIAL VIDEO AMPLIFIERS

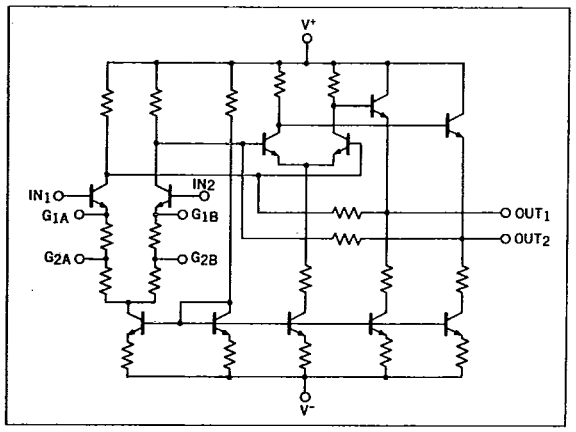
DESCRIPTION

The μPC1663 and μPC1664 are video amplifiers with differential input and output stages. An ultrahigh-frequency process (f_T = 6 GHz) improves AC performance compared with industry-standard type 733 video amplifiers. The μPC1663 and μPC1664 are excellent as sense amplifiers for high-density CCDs, as video or pulse amplifiers in high-resolution displays, and in communications equipment.

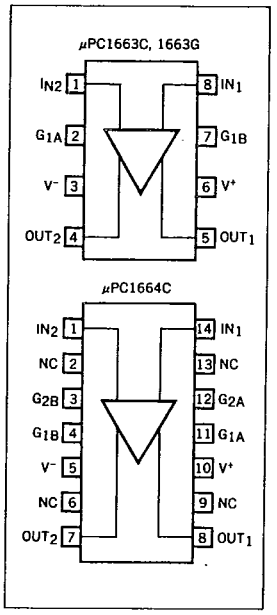
FEATURES

- Bandwidth and typical gain
  120 MHz at A_{VOL} = 300
  170 MHz at A_{VOL} = 100
  700 MHz at A_{VOL} = 10
- Very small phase delay
- Gain adjustable from 10 to 300
- No frequency compensation required

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM (Top View)



ORDERING INFORMATION

Part Number	Package
μPC1663C	8 PIN PLASTIC DIP (300 mil)
μPC1663G	8 PIN PLASTIC SOP (225 mil)
μPC1664C	14 PIN PLASTIC DIP (300 mil)

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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	μPC1663C	μPC1663G	μPC1664C	UNIT
Voltage between V^+ and V^-	$V^{\pm}$	±8	±7	±8	V
Power Dissipation	P_T	500	*280 (T_a = 75 °C)	570	mW
Differential Input Voltage	V_{ID}	±5	±5	±5	V
Input Voltage	V_{ICM}	±6	±6	±6	V
Output Current	I_O	35	35	35	mA
Operating Temperature Range	T_{opt}	−45 to +85	−45 to +75	−45 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	−55 to +150	−55 to +150	°C

*Mounted on 5 cm x 5 cm x 0.16 mm glass epoxy PWB

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V^{\pm}$ (1663C, 1664C)	±2	±6	±7	V
Supply Voltage	$V^{\pm}$ (1663G)	±2	±6	±6.5	V
Source Current	I_O source			20	mA
Sink Current	I_O sink			2.5	mA
Frequency Range		DC		200	MHz

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, $V^{\pm}$ = ±6V)

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Differential Voltage Gain	Gain 1	A_{Vd}	200	320	500		(Note 1)
	Gain 2		80	100	120		(Note 2)
	Gain 3		8	10	12		(Note 3)
Bandwidth	Gain 1	BW		120		MHz	R_S = 50 Ω (3 dB down point)
	Gain 2			170			
	Gain 3			700			
Rise Time	Gain 1	t_r		2.9		ns	R_S = 50 Ω, V_{out} = 1 V_{p-p}
	Gain 2			2.7			
	Gain 3			2.7			
Propagation Delay	Gain 1	t_{pd}		2		ns	R_S = 50 Ω, V_{out} = 1 V_{p-p}
	Gain 2			1.6			
	Gain 3			1.2			
Input Impedance	Gain 1	R_{in}		4.0		kΩ	
	Gain 2		6.7	13			
	Gain 3		50	180			
Input Capacitance		C_{in}		2		pF	
Input Offset Current		I_{IO}		0.4	5.0	μA	
Input Bias Current		I_B		20	40	μA	
Input Noise Voltage		V_n		3		$\mu V_{r.m.s.}$	R_S = 50 Ω, 10 k to 10 MHz
Input Voltage Range		V_I	±1.0			V	
Common Mode Rejection Ratio		CMR	55	70		dB	V_{cm} = ±1 V, f ≦ 100 kHz
			53	60			V_{cm} = ±1 V, f = 5 MHz
Supply Voltage Rejection Ratio		SVR	50	70		dB	ΔV = ±0.5 V
Output Offset Voltage	Gain 1	$V_{O(off)}$		0.3	1.5	V	$V_{O(off)} = \lvert OUT_1 - OUT_2 \rvert$
	Gain 2, 3			0.1	1.0		
Output Common Mode Voltage		$V_{O(CM)}$	2.4	2.9	3.4	V	
Output Voltage Swing		V_{Op-p}	3.0	4.0		V_{p-p}	
Output Sink Current		I_{sink}	2.5	3.6		mA	
Power Supply Current		I_{CC}		13	20	mA	

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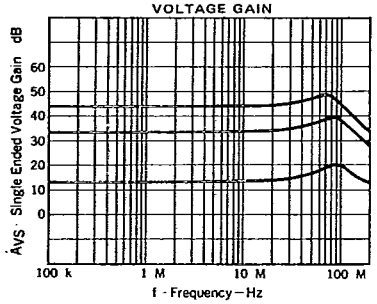
Notes: 1. Gain select pins G1A and G1B are connected.
2. Gain select pins G2A and G2B are connected.
3. All gain select pins are open.
4. Insert adjustment resistor (0 to 10 kΩ) between G1A and G1B when variable gain is necessary.

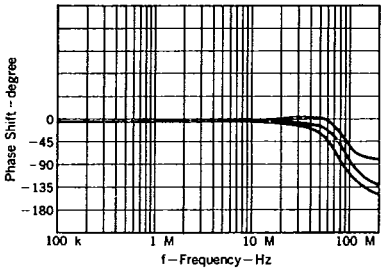
Attention: Due to ultrahigh-frequency characteristics, the physical circuit layout is very critical. Supply voltage line bypass, double-sided printed-circuit board, and wide-area ground line layout are necessary for stable operation. Two signal resistors connected to both inputs and two load resistors connected to both outputs should be balanced for stable operation.

TYPICAL PERFORMANCE CHARACTERISTICS (T_a = 25 °C)

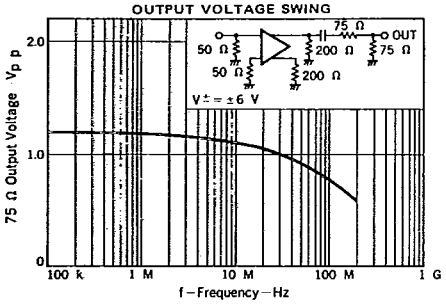
SINGLE ENDED VOLTAGE GAIN



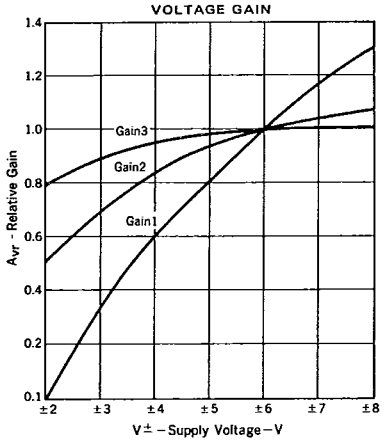
PHASE SHIFT



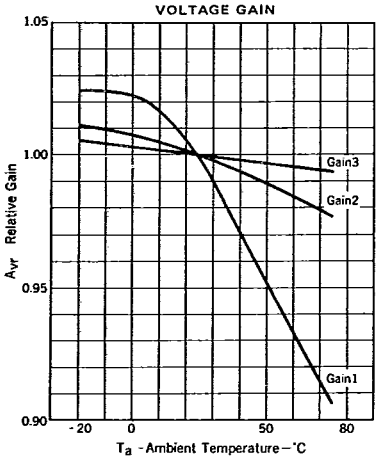
VIDEO LINE SINGLE ENDED OUTPUT VOLTAGE SWING



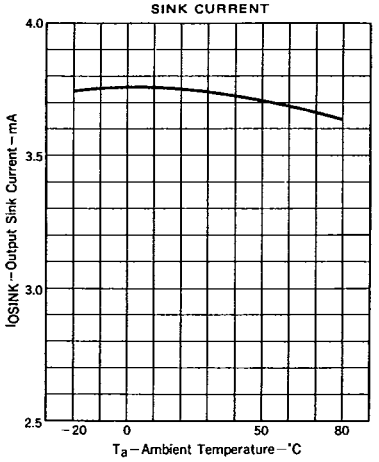
VOLTAGE GAIN



VOLTAGE GAIN



SINK CURRENT



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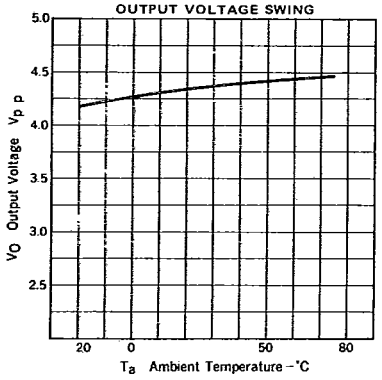
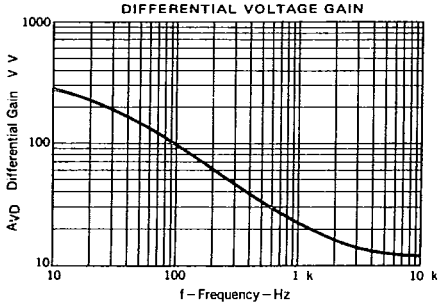
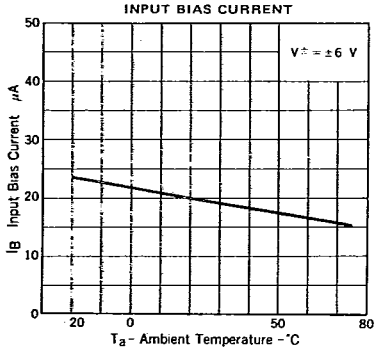
SINGLE ENDED
OUTPUT VOLTAGE SWING



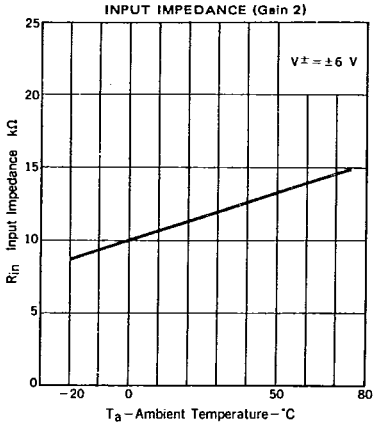
DIFFERENTIAL VOLTAGE GAIN



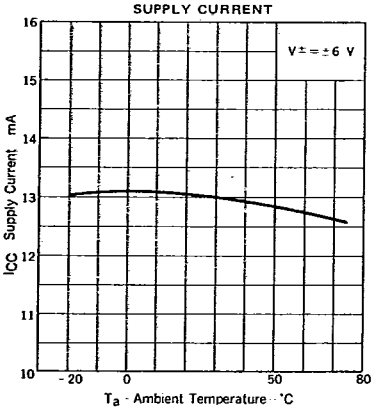
INPUT BIAS CURRENT



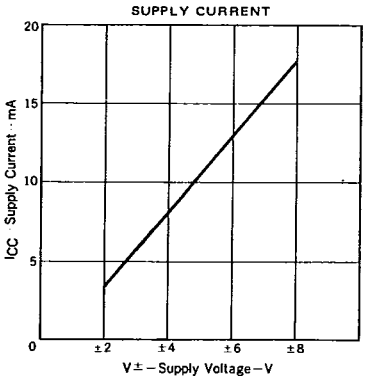
INPUT IMPEDANCE (Gain 2)



SUPPLY CURRENT

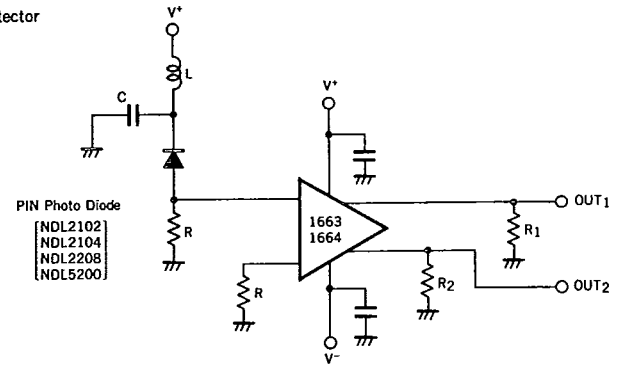


SUPPLY CURRENT



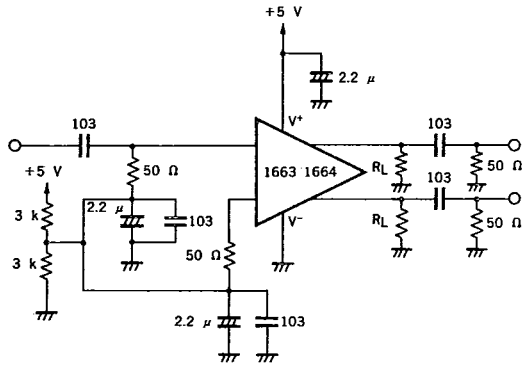
TYPICAL APPLICATIONS

● Photo Signal Detector



FET source follower buffer is necessary, when input impedance of μPC1663/1664 is critical.

● Application for +5 V Single Supply



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PERFORMANCE UNDER +5 V OPERATION

PARAMETER		CONDITIONS	PERFORMANCE	UNIT
Differential Gain	Gain 1	15 MHz	35	dB
	Gain 3		11	
Bandwidth	Gain 1	3 dB down point	106	MHz
	Gain 3		115	
Rise Time	Gain 1	R_S = 50 Ω, V_{OUT} = 80 mV_{p-p}	2.2	ns
Propagation Delay	Gain 1	R_S = 50 Ω, V_{OUT} = 80 mV_{p-p}	2.8	ns
	Gain 3	R_S = 50 Ω, V_{OUT} = 60 mV_{p-p}	1.8	
Phase Shift	Gain 1	100 MHz	−123	degree
	Gain 3		−93	
Output Power	R_L = 240 Ω	Z_L = 50 Ω 15 MHz	5.0	dBm
	R_L = 910 Ω		0	
	R_L = 80 Ω		−11.5	

μPC1163, μPC1164

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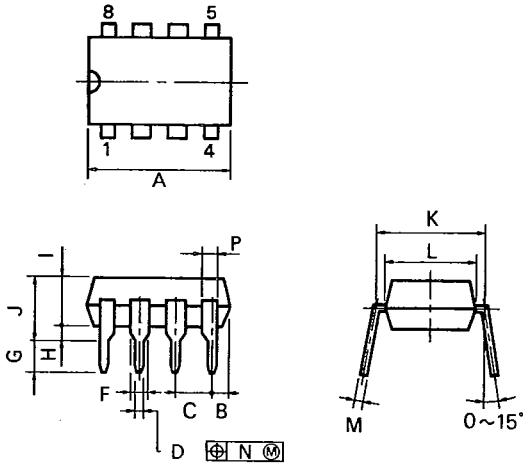
8 PIN PLASTIC DIP (300 mil)



P8C-100-300B,C

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.4 MIN.	0.055 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

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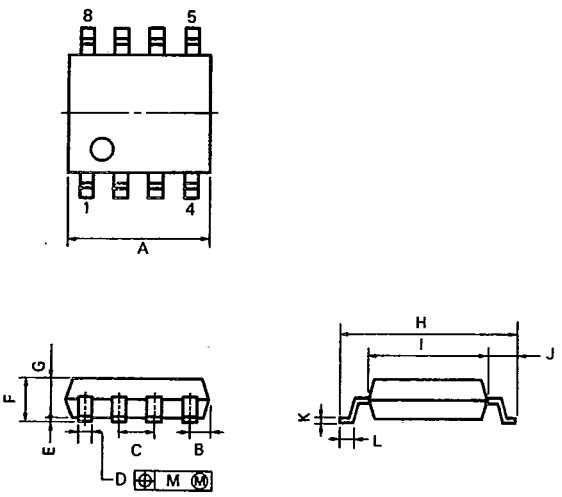
8 PIN PLASTIC SOP (225 mil)



S8GM-50-225B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	5.70 MAX.	0.225 MAX.
B	0.94 MAX.	0.037 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.49	0.059
H	6.5 ± 0.3	0.256 ± 0.012
I	4.4	0.173
J	1.1	0.043
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

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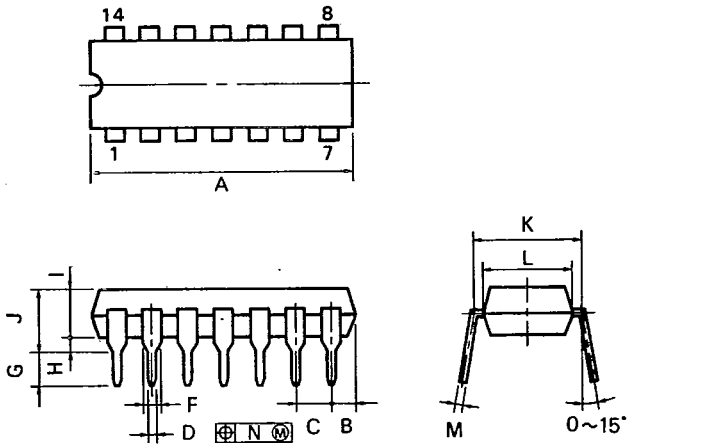
14 Pin Plastic DIP (300 mil)



P14C-100-300B1

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.6^{\pm0.3}$	$0.142^{\pm0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01